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A new architecture of Thermometer to Binary code encoder for 4 - bit FLASH ADC in 45nm CMOS process

Abstract. *In this work, a new architecture of Thermometer to Binary Encoder is designed in 45nm CMOS Technology for 4-bit FLASH ADC. The Thermometer code is converted to intermediate gray code and then to binary code in the proposed encoder. The 4-bit FLASH ADC is integrated with the proposed low –power encoder, Double-tail Dynamic Comparator and resistive ladder networks. Simulation results show that the proposed encoder consumes 119μW power with 1V supply voltage. The 4-bit FLASH ADC consumes less power when compared with the conventional ADCs.*

Streszczenie. *W tej pracy zaprojektowano nową architekturę termometru do kodera binarnego w technologii 45nm CMOS dla 4-bitowego FLASH ADC. Kod termometru jest konwertowany na pośredni kod Graya, a następnie na kod binarny w proponowanym enkoderze. 4-bitowy FLASH ADC jest zintegrowany z proponowanym koderem małej mocy, dwustronnym komparatorem dynamicznym i rezystancyjnymi sieciami drabinkowymi. Wyniki symulacji pokazują, że proponowany enkoder pobiera moc 119μW przy napięciu zasilania 1V. 4-bitowy FLASH ADC zużywa mniej energii w porównaniu z konwencjonalnymi przetwornikami ADC. (* ***Nowa architektura termometru do enkodera kodu binarnego dla 4-bitowego FLASH ADC w procesie 45nm CMOS***)

Keywords: Thermometer-code Encoder, Comparator, Flash ADC, low power
Słowa kluczowe: Termometr-kod Enkoder, komparator, Flash ADC, mała moc

Introduction

Most electronic systems require analog data from the real world to be processed using digital logic, which demands the use of analog and digital converters. Portable devices and high-end instruments are becoming increasingly complex in this electronic age, and they can now execute a wide range of tasks with high precision. Even as the capability of these gadgets improves, their size continues to shrink. The majority of these appliances are powered by batteries therefore power consumption is a crucial consideration in their design [1-3]. ADCs are used to convert analog signals into digital that may be processed by digital systems. ADCs with high speed and low power consumption are required in today's VLSI design for signal processing systems [4-6].

Input signal bandwidth, resolution, quantization error, SNR, differential non-linearity, and integration non-linearity are some of the basic factors that affect ADC performance[7-8].However, resolution is always inversely proportional to the device's conversion rate [9-11]. Almost every practical application.

Design Methodology

An encoder is a combinational circuit that reverses the Decoder's operation. There are a maximum of 2n input lines and 'n' output lines on this device. As a result, it encodes data from 2^n inputs into an n-bit code. It will generate a binary code that is equivalent to the active high input. As an outcome, the encoder encodes 2^n input lines to 'n' bits.In the design of Flash ADCs, the thermometer to binary code conversion circuits are considered the bottleneck [7-8]. Because the entire circuit's speed is affected by this overall architecture, picking the right encoder block design is critical. The outputs from the comparator array in Flash ADC will be in thermometer code format due to the parallel topology. As a mercury column in a thermometer, this is the number of logic 'high' bits that will be organized according to the strength of the signal. Because there are 2^n-1 comparators in a flash ADC, each comparator delivers one output comparison. The number of bits in the thermometer code at involves the conversion of an analog signal to a digital signal for more exact output, hence the ADC is critical in a variety of applications such as wireless communication and digital signal processing.

ADC designs are classified according to their speed, resolution, and power consumption. Low-power, high-speed, medium-resolution data converters should use the Flash ADC architecture. There are several blocks in the Flash ADC itself like Comparator array, resistor ladder, Encoder, etc. Even the encoder portion of the ADC consumes a significant amount of power. As a result, the low-power design of a Thermometer to binary code Converter helps in enhancing the whole system's performance.

The objective of this work is to create a low-power 4-bit flash ADC. This work proposes a one-of-a-kind framework for translating thermometer data to binary code. An encoder with 16 inputs is required for a 4-bit ADC.

Thermometer to binary intermediate Gray Encoder

In this architecture, the thermometer code is directly transformed to its corresponding gray code, which is subsequently converted to binary. Fig.1 shows the Intermediate to Gray code-based encoder. This technique saves a burst of power. Converting the thermometer to grey coding will help to reduce bubble errors in addition to saving power. The equations shown below demonstrate the conversion of gray code to binary code using the basic logic gates [AND, OR, and INVERTER].

(1) G4=T8

(2) G3=T4T12’

(3) G2=T2T6’+T10T14’

(4) G1=T1T3’+T5T7’+T9T11’+T13T15’

Finally, these gray codes are converted to binary codes using XOR gates and general gray to binary code conversion equations.

(5) B4=G4
(6) B3=G3^B4
(7) B2=G2^B3
(8) B1=G1^B2

From all of the above equations, the circuit is designed using logic gates.

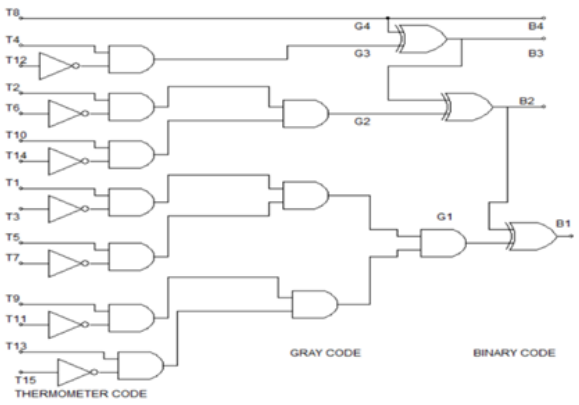

Fig. 1 Proposed Intermediate Gray code-based encoder architecture

The Intermediate Gray code encoder is designed using cadence software in the 45nm CMOS process.

Comparator

In analog to digital converters with high speed, the comparator is crucial. A comparator compares two analog signals or voltages and provides a digital output based on the comparison results[12-14]. Comparators, also known as 1-bit analog to digital converters, are a type of A/D converter that is widely employed. Many high-speed ADCs, such as flash ADCs, require small chip regions and high-speed, low-power comparators[15-21].A high-speed comparator with minimal power consumption is utilized in the design of ADCs. Assume that Vin is smaller than the DC voltage level at Vref in the op-amp comparator circuit shown in Fig.3. The comparator's output will be Low because the non-inverting (positive) input is less than the inverting (negative) input, resulting in a negative saturation of the output at the negative supply voltage, -Vcc. When there is an increase in the input voltage (Vin), over the inverting input's reference value (Vref), the output voltage rapidly rises HIGH towards the positive supply voltage, +Vcc, resulting in positive output saturation. The op-output amps are somewhat smaller than the reference voltage if the input voltage Vin is decreased again.

Double tail dynamic comparator

Two tail transistors are used in the double tail architecture. For low-power applications, a double tail comparator is utilized. Increase the voltage differential between the output nodes in this technique to speed up latch regeneration. Two control transistors, in parallel with M3 and M4 transistors but cross-coupled, were added to the first stage for this purpose. The reset and decision-making phases are the two operation modes of the double tail comparator. The operation modes are determined by the clock input. CLK = VDD is the assessment phase, while CLK = 0 is the reset phase. The NMOS transistor is turned off and the PMOS transistor is turned on when CLK = 0. NMOS and PMOS are both active when CLK = VDD. The comparator is designed as shown in Fig.2.

When CLK = 0 during the reset phase, both the tail transistors Mtail1 and Mtail2 are turned off to avoid static power. The M3 and M4 transistors are both operational. M3 and M4 connect both the fn and fp nodes to VDD, turning off the MC1 and MC2 transistors. In the circuit, MR1 and MR2 are two intermediate stage transistors. These transistors reset both latch outputs to ground. Throughout the decision-making process, both tail transistors are on while M3 and M4 transistors are off when CLK = VDD. The control transistors MC1, MC2 are still off at the start of this phase (since fn and fp are about VDD). As a result, depending on the input voltages, fn and fp continue to drop at various rates. Assume VINP > VINN, which means fn is falling faster than fp (since M2 provides more current than M1). As long as fn continues to fall, the corresponding pMOS control transistor (MC1) begins to switch on, bringing the fp node back to the VDD and allowing fn to be fully discharged.

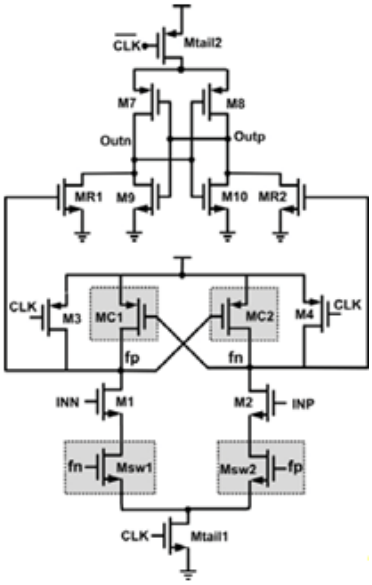

Fig.2 Circuit Diagram of Double Tail Dynamic Comparator [15]

A current from VDD is pulled to the ground via input and tail transistors (ie, M1, MC1, and Mtail1) when one of the control transistors is turned on, resulting in static power consumption. Two nMOS switches, Msw1 and Msw2, are utilised below the input transistors to get around this constraint. Both switches are closed at the start of the decision-making phase because both fn and fp nodes were pre-charged to VDD (during the reset phase), and fn and fp begin to discharge at different speeds. The voltage difference between the control transistors will develop when the comparator detects that one of the fn or fp nodes is discharging quicker. When fp approaches VDD and fn must be fully discharged, the switch in fp's charging path is opened, but the switch connected to fn is closed, allowing the fn node to be fully discharged. In other words, the operation of the control transistors with the switches simulates the operation of the latch.

Flash ADC Design

The propsed encoder designed is integrated with comparators for 4-bit Flash ADC. There are 16 resistors and 15 comparators for 4-bit Flash ADC. The outputs of comparators are given to 15 inputs of the encoder and the last input is given to the ground. Then the flash ADC is given with input voltage and reference voltage.To generate 15 different reference voltages, 16 resistors are used. When estimating the resistance value, the effects of power consumption, settling time, and mismatch are taken into account.The voltage will then be divided and sent to comparators based on the values of the resistors, and the output of the comparators will be in binary format, i.e. a high '1' or a low '0' will suffice. The inputs will next be processed, and the output will be created in binary form, as seen above in the encoder.

Results and Discussion

The proposed thermometer code encoder is simulated in 45nm CMOS process and all the sub blocks including comparator and resistive ladder network is integrated to form 4-bit FLASH ADC. Table1 shows the power consumption of the proposed Encoder for the various supply voltages. The Flash ADC consumes 119.1uW of power as shown in Fig.3.

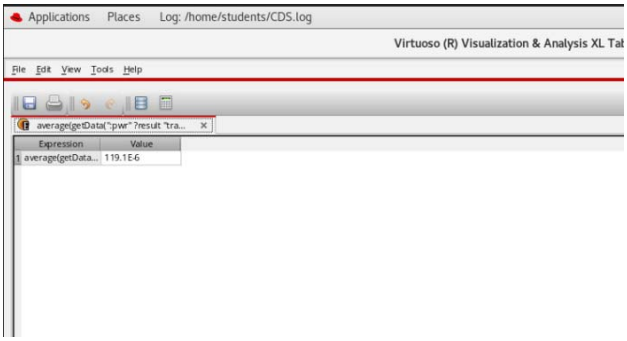

Fig.3 Flash ADC's power consumption

Table 1 Comparison of different types of an encoder with the proposed encoder

Title	Type of encoder	Power Dissipation	Delay
An efficient priority encoder and decoder using 45nm FinFET technology.	priority encoder	362858.23µW	24.4s
Design of a 4-bit Flash ADC	Thermometer to Binary Code Converter	1.943mW	6.182ns
Proposed encoder	Thermometer-Gray-Binary encoder	316.8nW	11.06ns

Table 2 Comparison of different types of the comparators with the proposed comparator

Type of Comparator	CMOS Process	Power
A low power dynamic comparator for low offset applications	180 nm	347µW
MSB and LSB comparators	45nm	2.95mW
Double tail dual-rail dynamic latched comparator	180nm	10.2µW
Low power time domain rail to rail comparator	560nm	19µW
Proposed Comparator	45nm	1.41µW

Table 3 Comparison of different types of the ADCs with the proposed Flash ADC

Name of ADC	Encoders and Comparators used	CMOS Technology	Power consumption
A high-speed flash ADC	Encoder designed with Pseudo dynamic CMOS logic	180nm	0.68mW
ADC	Using operational amplifiers	45nm	9mW
Proposed Flash ADC	Thermometer encoder, double tail dynamic comparator	45nm	119µW

Table 2 shows the comparison of different types of comparators and Table 3 shows the comparison of different types of ADCs with the designed 4-bit FLASH ADC.

Conclusion

Bbinary code encoder architecture is used for Flash ADC. The thermometer code sequence is transformed to intermediate grey code, which is subsequently converted to the appropriate Binary code. The suggested architecture's core building elements are two input XOR gates and logical gates. Using 45nm CMOS technology, the circuit is simulated in cadence and results are compared to the performance of earlier layouts. Based on the simulation findings, the proposed 4-bit Flash ADC consumes an average of 119uW at 1V with all possible combinations of logic inputs, which is the lowest power consumption among the accessible architectures.

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