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Quasi-Z-Source Three-Phase Voltage Source Inverter with Virtual Space Vector Modulation to Increase the Voltage Gain and for the Reduction of Common Mode Voltage

Research paper

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Abstract: A quasi-Z-source network is used to boost the DC bus voltage of a voltage source two-level H-bridge inverter to increase the voltage gain. With the increase in the DC bus voltage, the common mode voltage (CMV) also increases. The CMV is reduced using virtual space vector pulse width modulation (SVPWM). Due to the presence of a quasi-Z-source network, the expression of the CMV changes significantly with respect to the conventional voltage source two-level H-bridge inverter fed from a pure DC supply. In this paper, a detailed analysis of the origin of the CMV for the quasi-Z-source two-level H-bridge inverter is presented. Additionally, it is shown how the CMV is affected for a DC input supply taken from a three-phase diode bridge rectifier. The work also details the scheme for suitable placement of shoot-through time intervals required for boosting within the non-active time intervals in virtual SVPWM. The simulation and experimental results show the scheme is effective in increasing the voltage gain and reducing the CMV arising at the third harmonic of the desired output frequency by at least 33.33%.

Keywords: *common mode voltage • quasi-Z-source inverter • virtual space vector modulation • voltage source inverter • voltage gain*

1. Introduction

The space vector pulse width modulation (SVPWM) is used in a conventional H-bridge voltage source inverter (VSI) to achieve voltage gain more than the gain achieved through sinusoidal pulse width modulation (SPWM). However, even with SVPWM, the output line to line root mean square (RMS) voltage is less than the input AC line to line RMS voltage applied to the input of the three-phase diode bridge rectifier. To overcome this, the impedance network commonly known as the Z-network (Peng, 2003**)** is placed in such a way in between the rectifier output and the DC input of the H-bridge of the VSI, which creates a significant increase in the overall gain of the system with suitable shoot-through duration (Peng, 2003; Peng et al., 2005a). The Z-network with the VSI can perform the buck and boost (Peng, 2003; Peng et al., 2003). A simple Z-network made of inductors and capacitors cannot maintain continuous DC input current. A quasi-Z-source inverter (Q-ZSI) is used to obtain continuous current from the input DC supply. The different configurations for quasi-Z-network applicable in a VSI consisting of inductors, capacitors and a diode can be found in Anderson and Peng (2008). Application of back-to-back connected Q-ZSI in DSTATCOM is described in Sabat et al. (2022). The use of two-cascaded Q-ZSI to achieve large boosting capability is described in Gajanayake et al. (2010). The use of the switched inductor Q-ZSI configuration for enhanced boosting and suppression of current inrush is discussed in Nguyen et al. (2011). An application of Q-ZSI VSI to boost up the DC voltage in distributed power-generation systems is described in Vinnikov and Roasto (2011). The SVPWM can be used in ZSI as well as in Q-ZSI with some modifications for enhanced DC bus utilisation (Liu et al., 2014;

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Loh et al., 2005; Nanda et al., 2019). Here, the part of the duration of the zero-states is used to create shoot-through states in boosting the voltage. At least two semiconductor switches in a leg are switched on simultaneously to create shoot-through states. The amount of boosting depends on the selection of shoot-through duty ratio. Higher the shoot-through duty ratio, more is the boosting. However, the maximum value of this shoot-through duty ratio is restricted by the available duty ratio for the zero-states (Peng et al., 2005b).

The power circuit schematic of the arrangement is shown in Figure 1. The input AC three-phase lines are connected to a three-phase diode bridge rectifier. A capacitor (C_{in}) acts as a DC filter capacitor. The rectifier DC output (v_{dc}) is having a small ripple voltage. To find the mid-point potential of the DC voltage, two conceptual equal voltage sources of value $\frac{v_{dc}}{2}$ connected in series are shown. The quasi-Z network consists of two inductors (L1,L2), two capacitors (C1,C2) and a diode (D7). The DC bus voltage of the VSI is marked as v_{dcbus} in Figure 1. This voltage is not a steady voltage, but fluctuates between the boosted DC voltage and the zero voltage during the active state and the shoot-through state, respectively. To find the mid-point potential of this voltage, two conceptual DC voltage sources are connected in series. In Figure 1, the common mode voltage (CMV) is defined as the voltage of the quasi-Z-source inverter's (Q-ZSI) load star point (n) with respect to the grid side neutral point (g) (Ünand Hava, 2009) and is expressed in Eq. (1),

$$\begin{aligned} v_{cmv} &= v_{ng} \\ &= (v_{Ag} + v_{Bg} + v_{Cg})/3 \\ &= (v_{Ao} + v_{og} + v_{Bo} + v_{og} + v_{Co} + v_{og})/3 \\ &= (v_{Ak} + v_{ko} + v_{og} + v_{Bk} + v_{ko} + v_{og} + v_{Ck} + v_{ko} + v_{og})/3 \\ &= (v_{Ak} + v_{Bk} + v_{Ck})/3 + v_{ko} + v_{og}) \\ &= v_{nk} + v_{ko} + v_{og}. \end{aligned} \tag{1}$$

From Eq. (1), it can be said that the expression of the instantaneous common mode (CMD) voltage for Q-ZSI fed from a diode bridge rectifier is different from the expression of the CMD voltage containing a pure DC source and without any quasi-Z network. In the case of a conventional two-level H-bridge VSI, the voltage of the load neutral terminal (n) with respect to the DC bus voltage mid-point terminal (k), i.e. (v_{nk}) is the CMV. The mid-point terminal potential is taken as the zero reference potential. In the case of a Q-ZSI, the potential difference (v_{nk}) refers to the CMV with respect to the virtual mid-point of the DC bus voltage of the VSI. The virtual mid-point potential is not taken as the reference voltage as it is a fluctuating voltage. The term (v_{ko}) refers to the voltage of the virtual mid-point of the DC bus voltage of the VSI with respect to the conceptual mid-point of the DC input voltage to the quasi-Z network. As this potential is fluctuating, so it cannot be considered as a reference potential. The term (v_{og}) refers to the voltage of the virtual mid-point of the DC input voltage to the quasi-Z network with respect to the grid neutral. The potential at the grid neutral terminal is considered as a reference potential.

The presence of the CMV causes electromagnetic interferences (EMIs), bearing currents, insulation failure and earth leakage current (Havaand Un, 2011; Laiand Shyu, 2004; Ünand Hava, 2009). The CMV appears due to many reasons (Cavalcanti et al., 2010; Lai and Shyu, 2004; Ünand Hava, 2009). The introduction of shoot-through states invites additional higher-order harmonics in CMV and results in common mode leakage current for a transformer-less PV system (Noroozi and Zolghadri, 2018). The reduction of the common mode circulating current in a grid-tied PV system using a Q-ZSI is discussed comprehensively in Noroozi et al. (2019). Different modulation techniques and filter circuits are available for reduction of the CMV at the output of the conventional H-bridge VSI

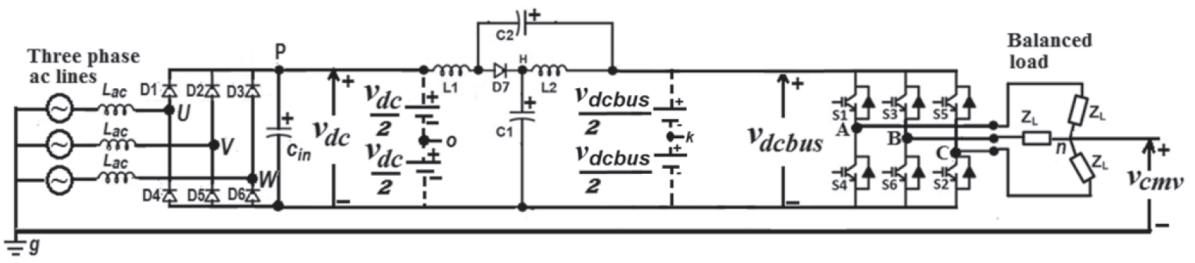

Figure 1. Power circuit schematic of the three-phase bridge rectifier fed Q-ZSI.

(Akagi and Doumoto, 2004; Akagi and Tamura, 2006; Cacciato et al., 1999, 2009; Fan et al., 2023; Hava and Un, 2011; Hedayati et al., 2013; Hou et al., 2013; Roomi, 2019; Tian et al., 2016; Yuen et al., 2012; Zhao et al., 2012; Zhu et al., 2012). The reduction of the CMV using different modulation techniques for a three-phase two-level H-bridge VSI is reviewed in Chen and Zhao (2016). Many aspects of the Q-ZSI with SVPWM such as voltage stress on the capacitors and devices, utilisation of DC bus voltage, overall efficiency, input current ripples and CMV are considered in the various published literature. A paper, recently published, considered the combination of Q-ZSI with 'Odd Pulse Width Modulation' to reduce the CMV and switching losses for a pure input DC supply source (Jiang et al., 2023). However, a detailed discussion on the origin of the CMV particularly for a Q-ZSI fed from a three-phase bridge rectifier is not available.

In this paper, a detailed discussion on the origin of this CMV is presented; to reduce the CMV, the virtual space vector modulation (VSVM) technique is implemented in the place of the SVPWM. The VSVM reduces the CMV but it decreases the voltage gain (Tian et al., 2016). The simple boost control (SBC) technique is used to boost the DC bus voltage so that the overall gain is the same with respect to a Q-ZSI with SVPWM. A fixed portion of the zero-state time duration of the switching cycle time period is utilised for conversion to shoot-through time duration. This shoot-through time duration remains fixed to get a constant boosting. The criticality in the placement of the shoot-through time duration in the case of the VSVM is discussed. A three-phase diode bridge rectifier is the DC source for the quasi-Z-source inverter in this paper. The effect of this rectifier on the CMV is also discussed.

The proposed method is theoretically analysed, and then the simulation results are presented. The simulation of the entire scheme is carried out in the MATLAB/Simulink simulation platform made by MathWorks. The VSVM pulse-generation scheme with the shoot-through states for the semiconductor switches in the H-bridge VSI is implemented in a Field Programmable Gate Arrays (FPGA Cyclone EPIC12Q240C8)-based development board. The pulses are fed to the semiconductor switches made of IGBTs through the gate driver ICs in the experimental set-up developed in the laboratory to carry out the experiments at different desired output frequencies. The analysis of the experimental results is included in this paper.

The experimental results obtained with the application of SVPWM and with the application of VSVM are compared to show the improvements achieved in reducing the CMV. For both the cases, the RMS magnitudes of the input AC grid voltage and the RMS magnitude of the fundamental component of the output AC voltage at the desired output frequency are kept the same by adjusting the shoot-through time duration and modulation index separately for SVPWM and VSVM.

2. Boosting by Shoot-Through States in a Q-ZSI with SVPWM

The arrangement of the two inductors (L1 and L2), two capacitors (C1 and C2) and a diode in a quasi-Z-network inverter (Q-ZSI) draws continuous DC current from the DC source (Anderson and Peng, 2008; Peng et al., 2003). As shown in Figure 1, the input DC voltage to the inverter is provided from a three-phase diode bridge rectifier, which is connected to the grid. The equivalent circuit of Q-ZSI, for analysis purposes, is shown in Figure 2 where input to the quasi-Z-network is (V_{in}) and the DC-link voltage v_{dcbus} after the quasi-Z-network, is input to the H-bridge VSI.

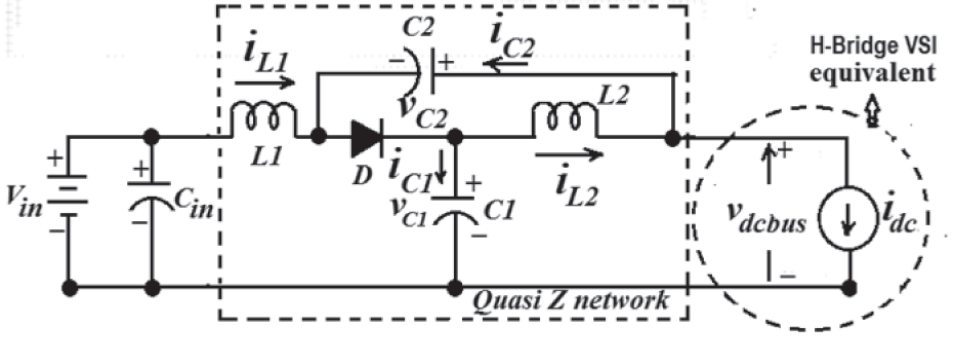

Figure 2. Equivalent electrical circuit for a Q-ZSI. VSI, voltage source inverter.

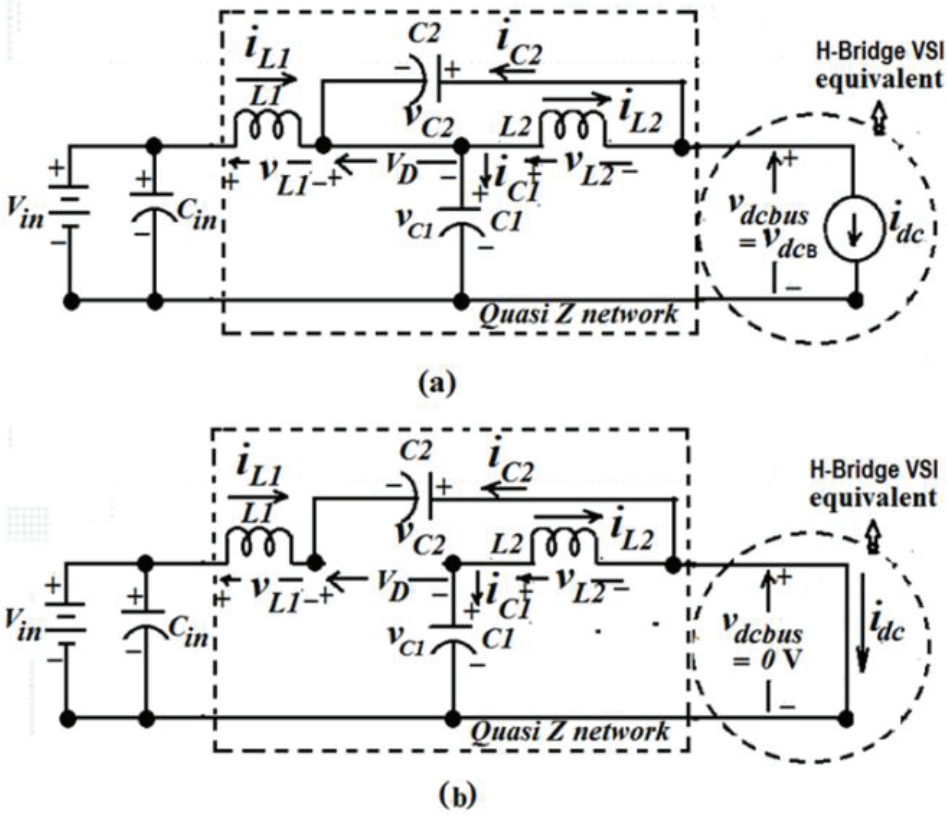

Figure 3. (a) Equivalent electrical circuit schematic for non-shoot-through state, (b) Equivalent electrical circuit schematic for shoot-through state. VSI, voltage source inverter.

The shoot-through duty cycle decides the boost-factor of the Q-ZSI. Two modes of operation are in a Q-ZSI: (a) shoot-through state and (b) non-shoot-through state. Figure 3 shows the equivalent electrical circuits for the two modes. To obtain a constant boost-factor, a fixed shoot-through duty ratio is considered. This mode is called 'simple boost control' (SBC) (Peng et al., 2005b).

Considering a fixed shoot-through duty ratio (d_{st}), the boosted DC (v_{dcB}) voltage during the non-shoot-through state can be expressed as:

$$v_{dcB} = \frac{1}{1-2d_{st}} \times V_{in} \tag{2}$$

The boost-factor '*B*' is defined as:

$$B = \frac{1}{1-2d_{st}} \tag{3}$$

Considering the output AC peak, the line-to-line voltage for SVPWM can be expressed as:

$$V_{ac(peak)} = m \times V_{dcB} \tag{4}$$

Where '*m*' is the modulation index. Therefore,

$$V_{ac(peak)} = m \times \frac{1}{1-2d_{st}} \times V_{in} \tag{5}$$

In SBC (Peng et al., 2005b), the relation between the maximum shoot-through duty ratio ($d_{st\max}$) and the modulation index (m) is:

$$d_{st\max} = 1 - m \tag{6}$$

The desired output line-to-line voltages of the Q-ZSI are defined in Eqs. (7)–(9),

$$v_{AB}(t) = V_m \cos(2\pi f_o t) \tag{7}$$

$$v_{BC}(t) = V_m \cos\left(2\pi f_o t - \frac{2\pi}{3}\right) \tag{8}$$

$$v_{CA}(t) = V_m \cos\left(2\pi f_o t - \frac{4\pi}{3}\right) \tag{9}$$

In space vector form, the expression of the output line-to-line voltage is given in Eq. (10).

$$\vec{v}_o(t) = V_m e^{j2\pi f_o t} \tag{10}$$

In space vector form, the expression of the desired output phase voltage rotating space vector is given in Eq. (11).

$$\vec{v}_{oPh} = \frac{V_m}{\sqrt{3}} e^{j\left(2\pi f_o t - \frac{\pi}{6}\right)} \tag{11}$$

3. VSVM

The VSVM technique is a modified version of the SVPWM (Tian et al., 2016). Here, all the virtual stationary space vectors are defined in terms of output three-phase voltages. Those virtual stationary space vectors are created only from conventional active stationary phase voltage space vectors. This is illustrated in Figure 4. The active virtual space vectors are $\vec{V}_{12}$, $\vec{V}_{23}$, $\vec{V}_{34}$, $\vec{V}_{45}$, $\vec{V}_{56}$ and $\vec{V}_{61}$. Each active virtual space vector is obtained by the vectorial summation of half of the two adjacent conventional active phase voltage space vectors. For example, $\vec{V}_{12}$ is composed of the

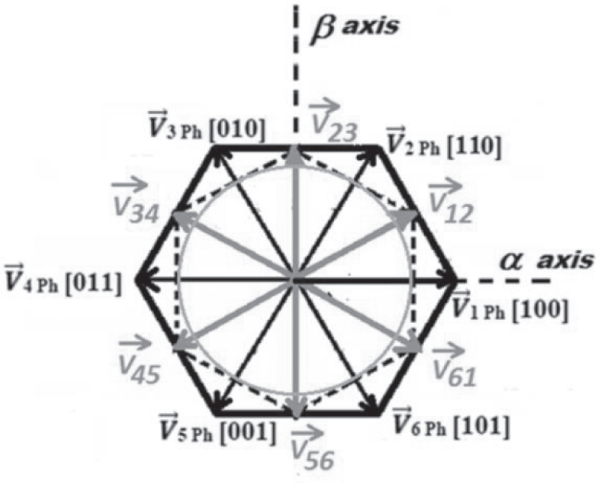

Figure 4. Construction of active virtual stationary space vectors from the stationary phase voltage space vectors. Virtual stationary space vectors are coloured in blue.

Table 1. Different switching state active and non-active (zero) stationary phase voltage space vectors.

Switching states $\begin{bmatrix} S1 & S3 & S5 \\ S4 & S6 & S2 \end{bmatrix}$	Magnitude(volt)	Angle(radian)	Assigned name
$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix}$	$\frac{2}{3}V_{dcB}$	0	$\vec{V}_{1Ph}$
$\begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$\frac{2}{3}V_{dcB}$	$\frac{\pi}{3}$	$\vec{V}_{2Ph}$
$\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix}$	$\frac{2}{3}V_{dcB}$	$\frac{2\pi}{3}$	$\vec{V}_{3Ph}$
$\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \end{bmatrix}$	$\frac{2}{3}V_{dcB}$	$-\pi$	$\vec{V}_{4Ph}$
$\begin{bmatrix} 0 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix}$	$\frac{2}{3}V_{dcB}$	$-\frac{2\pi}{3}$	$\vec{V}_{5Ph}$
$\begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}$	$\frac{2}{3}V_{dcB}$	$-\frac{\pi}{3}$	$\vec{V}_{6Ph}$
$\begin{bmatrix} 0 & 0 & 0 \\ 1 & 1 & 1 \end{bmatrix}$	0	--	$\vec{V}_{0Ph}$
$\begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 0 \end{bmatrix}$	0	--	$\vec{V}_{7Ph}$

stationary phase voltage space vectors $\vec{V}_{Ph1}$ and $\vec{V}_{Ph2}$.The non-active virtual space vector is created by combining vectorially half of the two opposite active stationary phase voltage space vectors. There are three such non-active virtual space vectors as $\vec{V}_{14}$, $\vec{V}_{36}$ and $\vec{V}_{25}$. The solid black lines with arrow-head indicate the active stationary phase voltage space vectors and the blue solid lines with arrow-head indicate the six active virtual space vectors in Figure 4.

Table 1 shows the six active stationary phase voltage space vectors out of the different permissible switching combinations of the switches of the inverter.

Considering,

$$\vec{V}_1 = \frac{2 \times V_{dcB}}{3} \times e^{j0} \tag{12}$$

and,

$$\vec{V}_2 = \frac{2 \times V_{dcB}}{3} \times e^{j\frac{\pi}{3}} \tag{13}$$

The virtual stationary voltage space vector can be expressed as,

$$\vec{V}_{12} = \frac{\vec{V}_1}{2} + \frac{\vec{V}_2}{2} = \frac{V_{dcB}}{\sqrt{3}} \times e^{j\frac{\pi}{6}} \tag{14}$$

Table 2 shows the six active and non-active virtual stationary phase voltage space vectors and the relationship with stationary phase voltage space vectors.

Table 3 shows the instantaneous CMV with respect to the conceptual mid-point potential of the boosted DC voltage, i.e. 'v_{nk}' for different active and non-active (zero) stationary phase voltage space vectors. For a conventional

Table 2. Six active and non-active virtual stationary voltage space vectors and the relationship with the stationary phase voltage space vectors.

Relationship with Stationary phase voltage space vectors	Magnitude(volt)	Angle(radian)	Assigned name
$(\vec{V}_{1Ph}+\vec{V}_{2Ph})/2$	$\frac{1}{\sqrt{3}}V_{dcB}$	$\frac{\pi}{6}$	$\vec{V}_{12}$
$(\vec{V}_{2Ph}+\vec{V}_{3Ph})/2$	$\frac{1}{\sqrt{3}}V_{dcB}$	$\frac{\pi}{2}$	$\vec{V}_{23}$
$(\vec{V}_{3Ph}+\vec{V}_{4Ph})/2$	$\frac{1}{\sqrt{3}}V_{dcB}$	$\frac{5\pi}{6}$	$\vec{V}_{34}$
$(\vec{V}_{4Ph}+\vec{V}_{5Ph})/2$	$\frac{1}{\sqrt{3}}V_{dcB}$	$-\frac{5\pi}{6}$	$\vec{V}_{45}$
$(\vec{V}_{5Ph}+\vec{V}_{6Ph})/2$	$\frac{1}{\sqrt{3}}V_{dcB}$	$-\frac{\pi}{2}$	$\vec{V}_{56}$
$(\vec{V}_{6Ph}+\vec{V}_{1Ph})/2$	$\frac{1}{\sqrt{3}}V_{dcB}$	$-\frac{\pi}{6}$	$\vec{V}_{61}$
$(\vec{V}_{1Ph}+\vec{V}_{4Ph})/2$	0	--	$\vec{V}_{14}$
$(\vec{V}_{2Ph}+\vec{V}_{5Ph})/2$	0	--	$\vec{V}_{25}$
$(\vec{V}_{3Ph}+\vec{V}_{6Ph})/2$	0	--	$\vec{V}_{36}$

two-level H-bridge VSI, the mid-point potential of the DC bus voltage is taken as the reference potential. The average value of this instantaneous voltage for the active stationary phase voltage space vectors over a switching cycle time period is not zero. This results in the generation of the frequency component at the third harmonic of desired output voltage frequency in the CMV for a conventional two-level H-bridge VSI (Tian et al., 2016). This is predominantly true for a Q-ZSI. The DC bus voltage is not constant here and the potential of the mid-point of the DC bus is fluctuating. The peak variation of the voltage 'v_{np}' is determined by the peak values of the non-active (zero) stationary phase voltage space vectors that stay within (+ $\frac{1}{2}V_{dcB}$,$-\frac{1}{2}V_{dcB}$). Therefore, the fluctuation of the mid-point potential with respect to grid neutral potential introduces a harmonic component at thrice the grid frequency.

Table 4 shows the instantaneous CMV with respect to the conceptual mid-point potential of the boosted DC voltage, i.e. 'v_{nk}' for different active and non-active virtual stationary phase voltage space vectors. For a conventional two-level H-bridge VSI fed from a pure DC supply, the average value of this instantaneous voltage over a switching cycle period is zero (Tian et al., 2016). In the case of Q-ZSI, this is also predominantly true. Here, DC bus voltage fluctuates due to active and shoot-through states. The mid-point potential of the DC bus cannot be considered as the reference potential. Therefore, the frequency component at the third harmonic of the desired output voltage frequency in the 'v_{nk}' is significantly reduced for a Q-ZSI. The peak variation of the voltage 'v_{nk}' is determined by the peak values of the non-active stationary phase voltage space vectors, which stay within (+ $\frac{1}{6}V_{dcB}$,$-\frac{1}{6}V_{dcB}$). An overall improvement compared to the SVPWM is thus achieved with respect to the CMV both in reducing the peak variations and reducing the third harmonic component for a Q-ZSI. However, it reduces simultaneously the voltage gain, which is the critical disadvantage of VSVM.

As shown in Figure 4, the inner circle (in yellow colour) touching the hexagon (in dashed black line) constituted by the tips of the virtual stationary phase voltage space vector (in blue colour) limits the maximum magnitude of the output phase voltage space vector. The radius of the inner circle is of the value $\frac{V_{dcB}}{2}$. Therefore, for VSVM, the maximum value of the output phase voltage space vector is:

$$V_{oph\max VSVM} = \frac{V_{dcB}}{2} = \frac{V_{dc}\times B}{2} \tag{15}$$

Where '*B*' is the boost-factor as defined in Eq. (3).

Table 3. Instantaneous CMV with respect to the conceptual mid-point potential of the boosted DC bus voltage for the active stationary phase voltage space vector.

Stationary phase voltage space vectors	Magnitude of v_{np} (volt)
$\vec{V}_{1Ph}$	$-\frac{1}{6}V_{dcB}$
$\vec{V}_{2Ph}$	$\frac{1}{6}V_{dcB}$
$\vec{V}_{3Ph}$	$-\frac{1}{6}V_{dcB}$
$\vec{V}_{4Ph}$	$\frac{1}{6}V_{dcB}$
$\vec{V}_{5Ph}$	$-\frac{1}{6}V_{dcB}$
$\vec{V}_{6Ph}$	$\frac{1}{6}V_{dcB}$
$\vec{V}_{0Ph}$	$-\frac{1}{2}V_{dcB}$
$\vec{V}_{7Ph}$	$+\frac{1}{2}V_{dcB}$

CMV, common mode voltage.

Table 4. Switching cycle average CMV with respect to the conceptual mid-point potential of the boosted DC bus voltage for virtual stationary active voltage space vector.

Virtual stationary Space vectors	Construction	Two extremes of Instantaneous value	Switching cycle average
$\vec{V}_{12}$	$(\vec{V}_{1Ph}+\vec{V}_{2Ph})/2$	$-\frac{1}{6}V_{dcB}$, $+\frac{1}{6}V_{dcB}$	$\left(-\frac{1}{6}V_{dcB}+\frac{1}{6}V_{dcB}\right)\Big/2=0$
$\vec{V}_{23}$	$(\vec{V}_{2Ph}+\vec{V}_{3Ph})/2$	$+\frac{1}{6}V_{dcB}$, $-\frac{1}{6}V_{dcB}$	$\left(+\frac{1}{6}V_{dcB}-\frac{1}{6}V_{dcB}\right)\Big/2=0$
$\vec{V}_{34}$	$(\vec{V}_{3Ph}+\vec{V}_{4Ph})/2$	$-\frac{1}{6}V_{dcB}$, $+\frac{1}{6}V_{dcB}$	$\left(-\frac{1}{6}V_{dcB}+\frac{1}{6}V_{dcB}\right)\Big/2=0$
$\vec{V}_{45}$	$(\vec{V}_{4Ph}+\vec{V}_{5Ph})/2$	$+\frac{1}{6}V_{dcB}$, $-\frac{1}{6}V_{dcB}$	$\left(+\frac{1}{6}V_{dcB}-\frac{1}{6}V_{dcB}\right)\Big/2=0$
$\vec{V}_{56}$	$(\vec{V}_{5Ph}+\vec{V}_{6Ph})/2$	$-\frac{1}{6}V_{dcB}$, $+\frac{1}{6}V_{dcB}$	$\left(-\frac{1}{6}V_{dcB}+\frac{1}{6}V_{dcB}\right)\Big/2=0$
$\vec{V}_{61}$	$(\vec{V}_{6Ph}+\vec{V}_{1Ph})/2$	$+\frac{1}{6}V_{dcB}$, $-\frac{1}{6}V_{dcB}$	$\left(+\frac{1}{6}V_{dcB}-\frac{1}{6}V_{dcB}\right)\Big/2=0$
$\vec{V}_{14}$	$(\vec{V}_{1Ph}+\vec{V}_{4Ph})/2$	$-\frac{1}{6}V_{dcB}$, $+\frac{1}{6}V_{dcB}$	$\left(-\frac{1}{6}V_{dcB}+\frac{1}{6}V_{dcB}\right)\Big/2=0$
$\vec{V}_{25}$	$(\vec{V}_{2Ph}+\vec{V}_{5Ph})/2$	$+\frac{1}{6}V_{dcB}$, $-\frac{1}{6}V_{dcB}$	$\left(+\frac{1}{6}V_{dcB}-\frac{1}{6}V_{dcB}\right)\Big/2=0$
$\vec{V}_{36}$	$(\vec{V}_{3Ph}+\vec{V}_{6Ph})/2$	$-\frac{1}{6}V_{dcB}$, $+\frac{1}{6}V_{dcB}$	$\left(-\frac{1}{6}V_{dcB}+\frac{1}{6}V_{dcB}\right)\Big/2=0$

CMV, common mode voltage.

For SVPWM, the peak value of the output sinusoidal phase voltage without Q-ZSI:

$$V_{oph\max SVPWM}=\frac{V_{dc}}{\sqrt{3}} \tag{16}$$

The maximum overall voltage gain of the converter is defined as:

$$G = \frac{V_{oph\max}}{V_{dc}} \tag{17}$$

Therefore, for VSVM with Q-ZSI,

$$G_{VSVM} = \frac{V_{oph\max vsvm}}{V_{dc}} = \frac{B}{2} \tag{18}$$

And for SVPWM without Q-ZSI,

$$G_{SVPWM} = \frac{1}{\sqrt{3}} \tag{19}$$

Therefore, by adjusting the boost-factor '*B*,' the overall maximum gain of Q-ZSI with VSVM can be made higher than the maximum overall gain for a conventional two-level H-bridge VSI. This facilitates the wide variation of the overall gain by varying the boost factor and the modulation index appropriately.

For a practical purpose, the boost factor and the modulation index are suitably adjusted to get the overall voltage gain using Eqs. (5) and (6).

4. Implementation of VSVM in Q-ZSI

The VSVM scheme in a conventional two-level H-bridge VSI is nearly similar to the SVPWM scheme, if the virtual stationary phase voltage space vectors are considered instead of stationary phase voltage space vectors for constructing the reference rotating output phase voltage space vector. This is illustrated in Figure 5. The six active virtual phase voltage stationary space vectors (coloured in blue) divide the space into six sectors. The sectors are identified with different numbers. The desired rotating output voltage space vector $\vec{V}_{ref}$ (coloured in red) at any instant lies in any of the sectors. Depending on the sector, it finds two adjacent virtual active stationary phase voltage space vectors; one ahead of it and one behind of it. These two virtual stationary active phase voltage space vectors are used to construct the rotating phase voltage space vector by taking an appropriate proportion from them. The

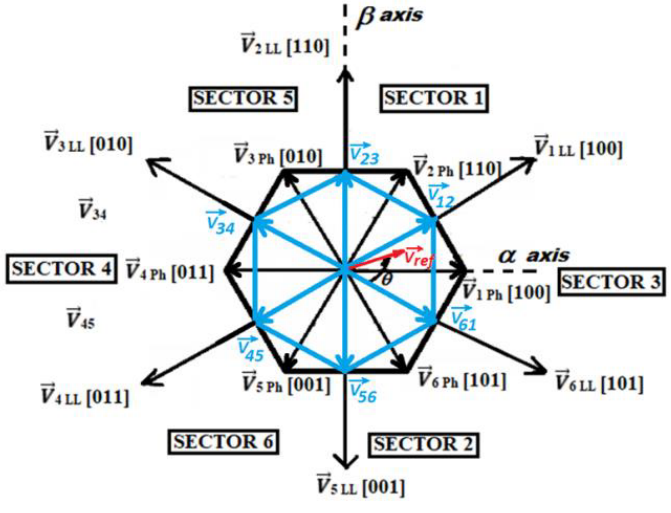

Figure 5. Relation between virtual space vectors, phase voltage stationary space vectors and line-to-line stationary voltage space vectors.

appropriate proportion corresponds to the duty ratio of the particular switching combination corresponding to the virtual stationary phase voltage space vector. In Figure 5, for the position of the reference rotating space vector, the stationary virtual space vectors $\vec{V}_{61}$ and $\vec{V}_{12}$ are to be considered.

Considering d_α to be the duty ratio for the virtual space vector $\vec{V}_{61}$,

$$d_\alpha = m_v.\sin\left(\frac{\pi}{3} - \theta\right) \tag{20}$$

Where,

$$m_v = \frac{\vec{V}_{ref}}{\frac{V_{dc}}{2}} \tag{21}$$

and, considering d_β to be the duty ratio for the virtual space vector $\vec{V}_{12}$,

$$d_\beta = m_v.\sin(\theta) \tag{22}$$

The non-active duty ratio d_{ov},

$$d_{ov} = 1 - d_\alpha - d_\beta \tag{23}$$

Non-active-duty ratio can be distributed between two 180° opposing stationary active space vectors ($\vec{V}_{3Ph}$, $\vec{V}_{6Ph}$). The duty cycle of each of the non-virtual active stationary phase voltage space vectors creating the participating virtual stationary space vectors can be obtained as follows:

For the space vector $\vec{V}_{6Ph}$ (as it will be engaged in half of the dwelling duration of the virtual space vector $\vec{V}_{61}$ and in half of the dwelling duration of the virtual space vector $\vec{V}_{36}$),

$$d_6 = \frac{d_\alpha}{2} + \frac{d_{ov}}{2} \tag{24}$$

For the space vector $\vec{V}_{1Ph}$ (as it will be engaged in half of the dwelling duration of the virtual space vector $\vec{V}_{61}$ and in half of the dwelling duration of the virtual space vector $\vec{V}_{12}$),

$$d_1 = \frac{d_\alpha}{2} + \frac{d_\beta}{2} \tag{25}$$

For the space vector $\vec{V}_{2Ph}$ (as it will be engaged in half of the dwelling duration of the virtual space vector $\vec{V}_{12}$),

$$d_2 = \frac{d_\beta}{2} \tag{26}$$

For the space vector $\vec{V}_{3Ph}$ (as it will be engaged in half of the dwelling duration of the virtual space vector $\vec{V}_{36}$),

$$d_3 = \frac{d_{ov}}{2} \tag{27}$$

Four duty cycles can be generalised as,

$$d_{o\alpha} = \frac{d_{ov}}{2} + \frac{d_\alpha}{2} \tag{28}$$

$$d_{\alpha\beta} = \frac{d_{\alpha v}}{2} + \frac{d_\beta}{2} \tag{29}$$

$$d_{\beta s} = \frac{d_{\beta}}{2} \tag{30}$$

$$d_{os} = \frac{d_{ov}}{2} \tag{31}$$

The active stationary phase voltage space vector operating for the duty ratio $d_{o\alpha}$ must be 180° opposite of the active stationary phase voltage space vector operating for the duty ratio d_{os}.

For getting the shoot-through operation, a part of the dwelling interval for d_{os} and an equal part from the dwelling interval of $d_{o\alpha}$ are taken so that their average contribution to the output voltage over a switching cycle becomes zero.

The shoot-through duration cannot be greater than the non-active duration. Hence,

$$d_{st} \le d_{ov} \tag{32}$$

For the SBC operation, the relation between the modulation index and the non-active duty ratio is (Peng et al., 2005b),

$$d_{ov}\big|_{\min} = 1 - m_v \tag{33}$$

Hence, the expression of the maximum d_{st} for a particular m_v,

$$d_{st}\big|_{\max} = 1 - m_v \tag{34}$$

So, from Eqs. (21) and (34), the range of d_{st} for VSVM is,

$$0 \le d_{st} \le (1 - m_v) \tag{35}$$

A few intermediate variables are defined to segregate dwelling durations corresponding to different duty ratios in a switching cycle interval and are given below.

$$m_1 = d_{o\alpha} \tag{36}$$

$$m_2 = d_{o\alpha} + d_{\alpha\beta} \tag{37}$$

$$m_3 = d_{o\alpha} + d_{\alpha\beta} + d_{\beta s} \tag{38}$$

$$mst = d_{st} \tag{39}$$

These values are compared with a triangular timing signal to segregate the different dwelling time intervals as shown in Figure 6. These values (m_1, m_2, m_3, mst) are compared with the triangular waveform to get different time intervals including the time intervals for the shoot-through. These shoot-through time intervals must be less than the interval for $\frac{d_{o\alpha}}{2}$. This is illustrated in Figure 6.

5. Simulation and Experimental Results Analysis

The simulation study is done in MATLAB/Simulink made by MathWorks with the circuit parameters as given in Table 5. The rating of the semiconductor devices and passive components used in the experiment are mentioned. The switches are considered having zero turn-on time and turn-off time in the simulation. The shoot-through duty ratio is considered as 0.16 and modulation index is considered as 0.8.

Figure 7 shows the plots of the CMV and its different constituents obtained through simulation.

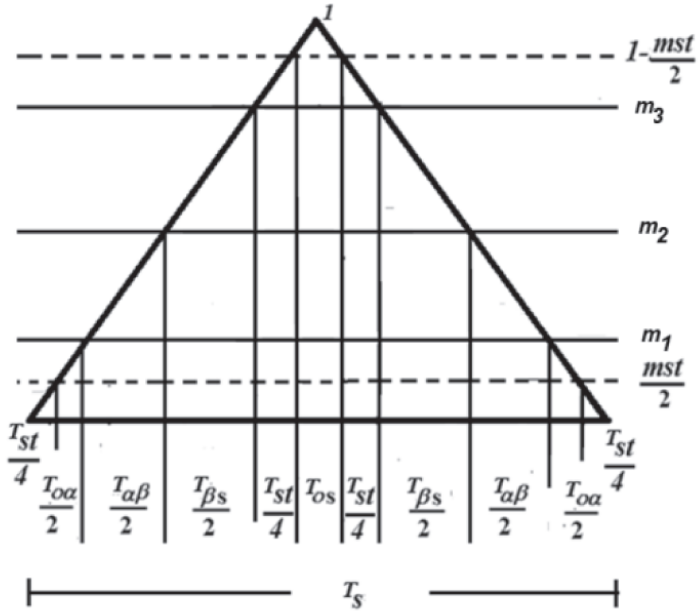

Figure 6. Generation of different dwelling durations corresponding to the different duty ratios including shoot-through duty ratio.

Table 5. Electrical circuit parameters considered for simulation study and experimental verification.

Circuit components and semiconductor devices	Rating
Grid	Three-phase 100 V, 50 Hz
Rectified DC	135 V
DC filter capacitor (C_{in})	2,000 microF, 450 V
Z-network inductor (L_1)	20 mH, 20 A DC
Z-network inductor (L_2)	20 mH, 20 A DC
Capacitance of Z-network capacitor (C_1)	140 microF, 1,800 VDC
Capacitance of Z-network capacitor (C_2)	140 microF, 1,800 V DC
Inductor of the per phase load (Z_L)	20 mH, 5 A
Resistor of the per phase load (Z_L)	29 ohms, 6 A
Bridge rectifier diode	80 A, 1,600 V
Z-network diode	150 A, 1,200 V
IGBT in the H-bridge inverter	100 A, 1,200 V

The plot for the CMV in Figure 7(a) shows that its maximum positive values and minimum negative values are modulated by time-varying waveforms. This is because the time-varying component v_{og} in the expression of CMV in Eq. (1) is a third harmonic component with respect to the grid frequency arising out of the three-phase diode bridge rectifier. The plot of v_{og} is shown in Figure 7(d). Therefore, the presence of a third harmonic component at thrice the grid frequency is inevitable. It is not clear from the waveform shown in Figure 7(a) whether any third harmonic component at thrice the output frequency is present. Even in Figure 7(b) for v_{nk}, we cannot identify the third harmonic component at thrice the output frequency by looking at the envelopes for positive maximum value and negative minimum value in the plot of the load-neutral potential with respect to the conceptual mid-point potential of the DC bus voltage of the VSI. The reason is that the third harmonic component at thrice the output frequency depends on the pulse width modulation technique utilised for a VSI fed from a pure DC supply when the DC bus voltage remains constant (Tian et al., 2016). Therefore, harmonic analysis is used to determine the third harmonic component at thrice the output frequency. The plot of v_{ko} in Figure 7(c) shows that the conceptual mid-point potential of the DC bus voltage of the VSI is not a constant value with respect to the conceptual mid-point potential of the

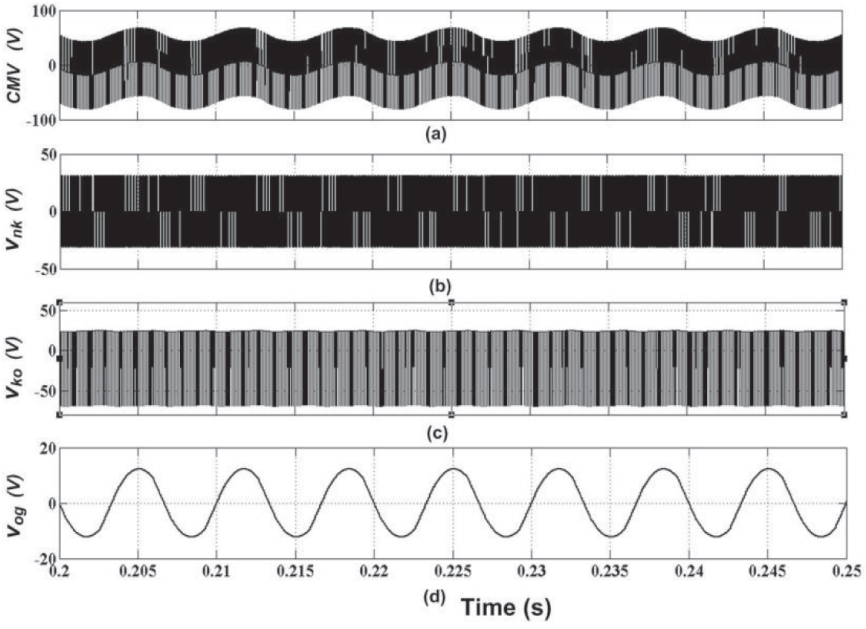

Figure 7. The plot of the CMV and its different components obtained through simulation: (a) The plot of CMV (v_{ng}), (b) the plot of the load neutral potential with respect to the conceptual mid-point terminal of the DC bus voltage of the VSI (v_{nk}), (c) the plot of the conceptual mid-point potential of the DC bus voltage of the VSI with respect to the conceptual mid-point terminal of the DC bus voltage after the rectifier (v_{ko}), (d) the plot of the conceptual mid-point potential of the DC bus voltage after the rectifier with respect to the grid neutral (v_{og}). Grid voltage: three-phase line-to-line 100V, 50 Hz, shoot-through duty ratio: 0.16, modulation index: 0.8 and desired output voltage frequency: 80 Hz. CMV, common mode voltage; VSI, voltage source inverter.

rectified DC voltage. The harmonic analysis in the low-frequency range of the CMD waveform shows that the RMS magnitude of the third harmonic component with respect to the grid frequency is around 9 V and the magnitude of the third harmonic component with respect to the desired output frequency is 0.7 V as shown in Figure 8(a). The VSVM reduces the third harmonic component with respect to the desired output frequency. The reduction is not as much for a VSI fed from a pure DC source without a quasi-Znetwork. This is due to the fact that the Q-ZSI does not provide a pure DC source with a constant mid-point potential of the DC bus voltage. The shoot-through states change the mid-point potential to the potential of the negative DC bus with respect to the grid neutral. Therefore, the complete reduction of CMV is not possible. However, this cannot reduce the contribution due to the three-phase bridge rectifier that appears at the third harmonic component with respect to the grid frequency. The third harmonic component at thrice the desired output frequency appears in Figure 8(b) for v_{nk} as expected. However, the third harmonic component at thrice the input grid frequency is absent in Figure 8(b) as expected. The harmonic spectrum of v_{ko} in Figure 8(c) shows the DC value as well as a few harmonic components due to the shoot-through states in Q-ZSI. The harmonic spectrum v_{og} in Figure 8(d) shows the third harmonic component at thrice the input grid frequency as expected. The harmonic spectrum of the CMV in Figure 8(a) reflects all the frequency components present in its constituents.

5.1. Experimental analysis

Experimental analysis was carried out in the laboratory with a quasi-Z-source inverter stack built in the laboratory consisting of a three-phase diode bridge rectifier feeding a Q-ZSI as in Figure 9. In Figure 9, the whole experimental set-up consists of the Q-ZSI stack, an R–L load and an field programmable gates array (FPGA) (Cyclone EPIC12Q240C8) development board. The experimental waveforms are captured in a digital-storage oscilloscope and the components at different frequencies are computed and displayed through a wide-band power analyser (Norma D6200) manufactured by LEM NORMA GmbH. The power circuit schematic of the Q-ZSI stack is closely similar to that given in Figure 1 with the difference that two diodes in series are used in the experimental set-up instead of one diode marked as ‘D7’ in the power schematic. The ratings of the electrical circuit components are given in Table 5. For the experimental results given in this paper, the modulation index is set at 0.8 and the value 0.16 is set for the shoot-through duty ratio.

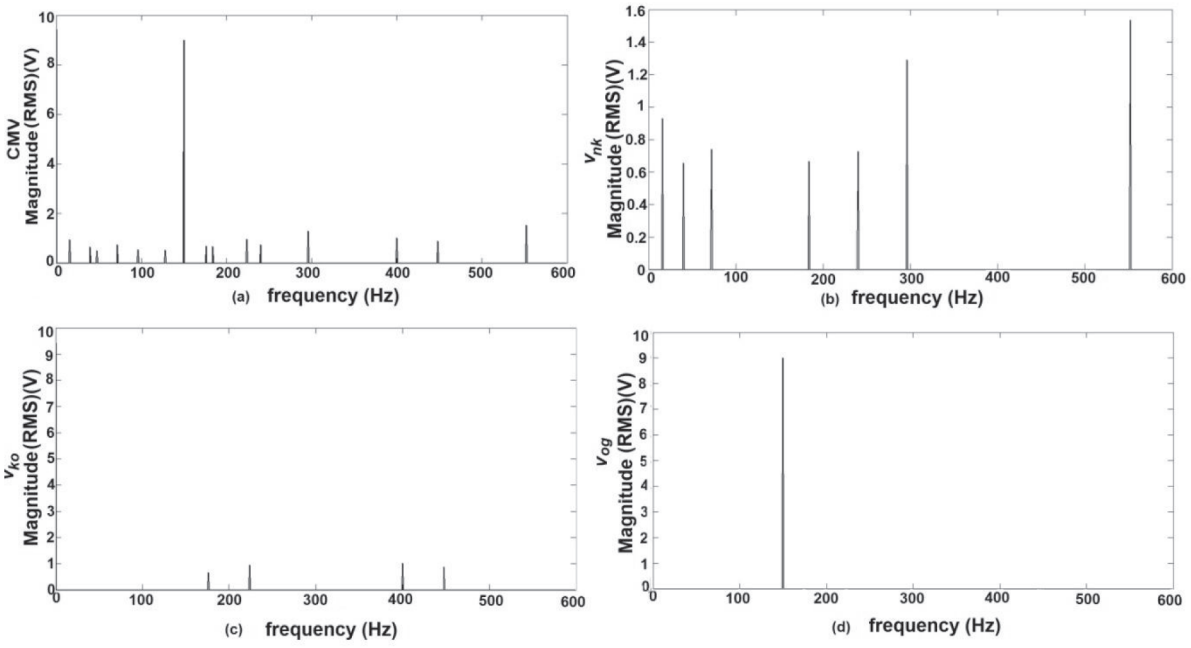

Figure 8. Harmonic analysis of the CMV and its different components. (a) Low frequency components in CMV. (b) Low frequency components in the potential of load neutral with respect to conceptual mid-point terminal of the DC bus of the VSI. (c) Low frequency components in the potential of conceptual mid-point terminal of the DC bus of VSI with respect to potential of the conceptual mid-point terminal of the DC bus voltage after rectifier. (d) Low frequency components of the potential of the conceptual mid-point potential of the DC bus voltage after the rectifier with respect to the potential of the grid neutral. Grid voltage: Three-phase line-to-line 100V, 50 Hz, shoot-through duty ratio: 0.16, modulation index: 0.8 and desired output voltage frequency: 80 Hz. CMV, common mode voltage; RMS, root mean square.

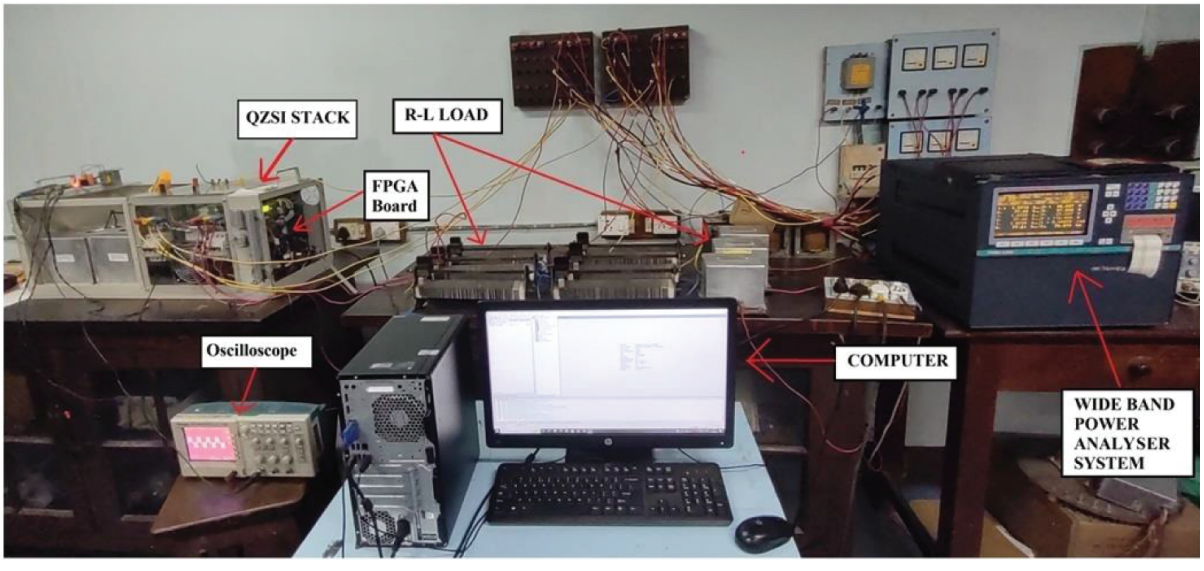

Figure 9. Experimental set-up.

In Figure 10, the rectified DC voltage waveform at the input of the Q-ZSI and the boosted DC voltage waveform obtained experimentally are shown. The AC line-to-line voltage is maintained at 100V (L–L), 50 Hz and the shoot-through duty ratio is set at 0.16 by programming through a real-time field programmable gates array (FPGA)-based controller. The VSVM switching frequency is 5 kHz. As recorded in Trace-1, the output of the voltage sensor for rectified DC voltage is 0.95V. Considering the gain of the voltage sensor as 7.125 mV/V, the rectified

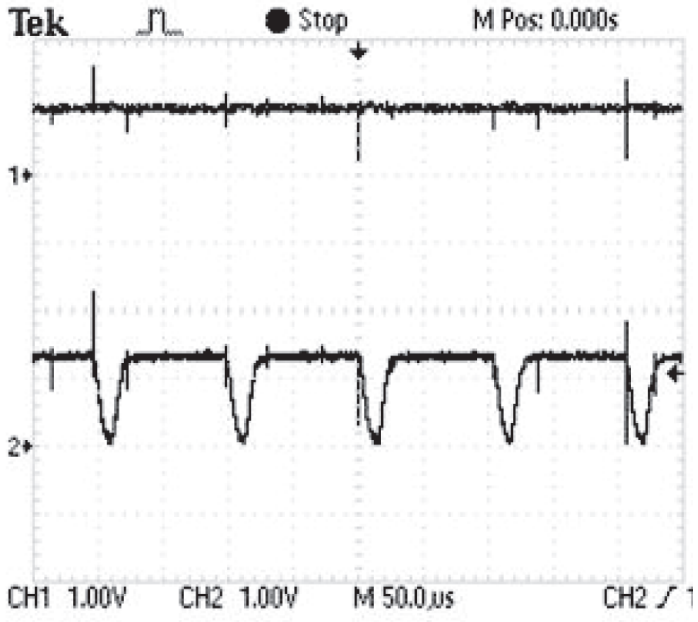

Figure 10. Experimental waveforms: Trace-1: Voltage sensor output for the rectified DC voltage, Trace-2: Voltage sensor output for the boosted DC voltage with the shoot-through duty ratio 0.16. Voltage sensor gain: 7.125 mV/V. Three-phase AC voltage at the input of the diode bridge rectifier: 100 V(line-to-line), 50Hz.

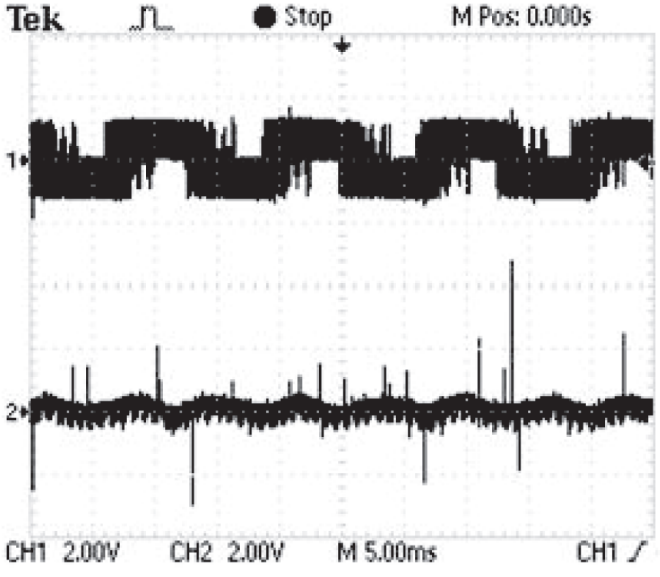

Figure 11. Experimental waveforms: Trace-1: Voltage sensor output for the output line-to-line voltage, Trace-2: Voltage sensor output for CMV. Voltage sensor gain: 7.125 mV/V. Shoot-through duty ratio: 0.16. Desired output frequency:80 Hz. Modulation index, m = 0.8. Three-phase AC voltage at the input of the diode bridge rectifier: 100 V (line-to-line), 50 Hz. CMV, common mode voltage.

voltage is 133 V, which is close to the theoretical value of 135 V for a three-phase bridge rectifier. As recorded in Trace-2, the output of the voltage sensor for the boosted DC voltage during the non-shoot-through time interval is 1.36V. Considering the gain of the LEM voltage sensor as 7.125 mV/V, the boosted DC voltage is 190.8 V. Theoretically, the boosted DC voltage should be 195.5 V with a shoot-through duty ratio 0.16 and a bridge rectifier

Figure 12. Experimental result: Low-frequency harmonic spectrum of the output line-to-line voltage analysed through the Norma D6200 Power Analyser manufactured by LEM NORMA GmbH. Shoot-through duty ratio: 0.16. Desired output frequency: 80 Hz. Modulation index, m = 0.8. Three-phase AC voltage at the input of the diode bridge rectifier: 100 V (line-to-line), 50 Hz.

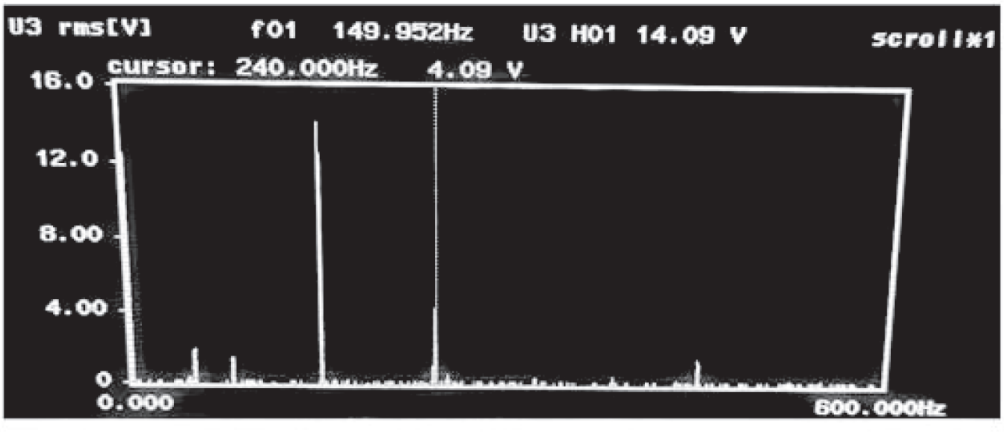

Figure 13. Experimental result: Low-frequency harmonic spectrum of the CMV analysed through the Norma D6200 Power Analyser. Shoot-through duty ratio: 0.16. Desired output frequency: 80 Hz. Modulation index, m = 0.8. Three-phase AC voltage at the input of the diode bridge rectifier: 100 V (line-to-line), 50 Hz. CMV, common mode voltage.

output of 133 V. However, due to the DC voltage drop in the equivalent series resistance of the inductors and across the diode of quasi-Znetwork, the ideal boosting is not obtained.

The CMV voltage waveform along with the output line-to-line voltage waveform as sensed by the voltage sensors are shown in Figure 11.

The low-frequency harmonic spectrum of the output line-to-line voltage is shown in Figure 12. The RMS magnitude of the desired frequency of 80 Hz is nearly equal to 76 V. The low-frequency harmonic spectrum of the CMV is shown in Figure 13. The dominant low-frequency components are of frequencies at the third harmonic of the grid frequency and at the third harmonic of the desired frequency.

Several experiments are carried out for different output frequencies of 40 Hz, 50 Hz and 80 Hz. The shoot-through duty ratios at 0.16 and the modulation index at 0.8 are maintained for all the cases. The results are tabulated in Table 6. The values of the rectified DC voltage, the boosted DC voltage, the RMS magnitude of the output line-

Table 6. Experimental results.

Output frequency (Hz)	Rectified DC voltage (V)	Shoot-through duty ratio	Boosted DC voltage (V)	Output voltage (L–L) Magnitude (RMS) (V)	Low-frequency Components in the CMV	
					Frequency (Hz)	Magnitude (V)
40	133	0.16	190	80	120	2.25
					150	14.35
50	133	0.16	190	80	150	11.86
					150	11.86
80	133	0.16	190	76	240	4.09
					150	14

CMV, common mode voltage; RMS, root mean square.

Table 7. Comparison between the SVPWM and the VSVM performances.

Output frequency (Hz)	Rectified DC voltage (V)	Output voltage (L–L) Magnitude (RMS) (V)	Low-frequencyComponents in the CMV		
			Frequency (Hz)	Magnitude (RMS)	
				SVPWM (V)	VSVM (V)
40	133	80	120	8	2
			150	14	14
50	133	80	150	13	12
			150	13	12
80	133	76	240	6	4
			150	14	14

CMV, common mode voltage; RMS, root mean square; SVPWM, space vector pulse width modulation; VSVM, virtual space vector modulation.

to-line voltages and the RMS magnitudes of the different dominant low-frequency components in the CMV are tabulated. In all the cases, the 100V, 50 Hz three-phase voltages are applied at the input of the diode bridge rectifier.

The boosted DC voltages are nearly equal to the theoretical values. For example, considering a 40 Hz output frequency and a 0.16 shoot-through duty ratio, from Eqs. (2) and (3), the boosted DC voltage should be 195.5 V. The value obtained from the experiment is 190 V. The small drop in the value can be attributed to the voltage drop in the resistance of the inductor and the voltage drop across the two diodes in the Z-network where 'D7' is realised with two series diodes.

Theoretically, for ideal switches, the RMS magnitude of the output line-to-line voltage with a boosted DC voltage of 190 V and a 0.8 modulation index is 93.00 V. However, the voltage obtained in the experiment is 76 V. The drop in voltage can be attributed to the voltage drop across the IGBTs and to the loss of voltage during switching state transitions between the IGBTs in a leg (Chatterjee et al., 2023a,b; Jeong and Park, 1991).

The corresponding RMS magnitudes of the low-frequency components at the third harmonic of the AC grid frequency are nearly equal for all the desired frequencies of values 40 Hz and 80 Hz. But for the desired output frequency of 50 Hz, the RMS magnitude is different. This is due to the merging of two low-frequency components of the CMV; one component due to the inverter and the other component due to the bridge rectifier. The frequencies of these two components become equal in this case.

A comparison between the SVPWM and the VSVM in the reduction of the dominant low-frequency components in the CMV is provided in Table 7. The values are rounded to the nearest integer values. The input three-phase AC grid voltage is 100 V, 50 Hz. The rectified DC voltage is 133 V. Three different desired output frequencies are considered. The modulation index and the shoot-through duty ratios for the SVPWM and the VSVM are adjusted separately so that the output AC voltage RMS values are nearly the same for both modulation schemes. For the SVPWM, the modulation index was 0.8 and the shoot-through duty ratio was 0.1, which gave an overall voltage gain(G) equal to 1 following the relation $G = m \times B = 1.25 \times 0.8$. For the VSVM, the modulation index was 0.8 and the shoot-through duty ratio was 0.16, which gave an overall voltage gain 1.01 following the relation $G = \frac{\sqrt{3}}{2} \times m \times B = \frac{\sqrt{3}}{2} \times 1.47 \times 0.8$. Other than the desired output frequency of 50 Hz, the reduction of the third harmonic component at thrice the desired output frequency is significant. The minimum reduction is 33.33%. The reduction in the percentage was

measured by first subtracting the value obtained using the VSVM from the value obtained using the SVPWM. Then, the result of the subtraction was divided by the value obtained using the SVPWM. After that, the ratio was multiplied by 100 to get the result. For the 50 Hz desired output frequency, the third harmonic component at thrice the grid frequency merges with the third harmonic component at thrice the desired output frequency. Hence, the VSVM cannot reduce the third harmonic component at thrice the desired output frequency. The reduction is not uniform for the other desired frequency because the switching state transition of the semiconductor switches gives rise to additional different low-frequency harmonics in the CMV (Chatterjee et al., 2023b).

6. Conclusion

The analysis shows that using the VSVM instead of the SVPWM in a Q-ZSI significantly reduces the third harmonic component in the CMV with respect to desired output frequency without sacrificing the voltage gain. The scheme reduces the peak amplitude of the CMV. The simulation results and the experimental results confirm the analytical findings reasonably. One of the reasons for not getting the complete elimination of the third harmonic component in the CMV with respect to the desired output frequency is the fluctuation of the mid-point potential of the rectifier output due to the shoot-through states. Further study in this area is required to identify other causes. It shows why this scheme cannot suppress the third harmonic component with respect to the grid frequency. When the desired output frequency becomes equal to the grid frequency, then the third harmonic component with respect to the grid frequency and the third harmonic component with respect to the desired frequency combine. The combined magnitude depends on the phase angle difference between those two same-frequency components. Then, the scheme fails to suppress the third harmonic component in the CMV with respect to desired output frequency. The switching state transition between two IGBTs in a leg affects the reduction of the expected output voltage magnitude due to the devices' finite turn-on and turn-off time. It influences the magnitudes of the low-frequency components in the CMV in practical situations. Very fast turn-on and turn-off devices can overcome these. Further work on calculating the overall efficiency of the proposed scheme is being undertaken.

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