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Evaluation of SVC-Coupled Hybrid DSTATCOM using JLMS Algorithm for Enhancement of Power Quality

Research paper

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Abstract: This research study explains the design and performance of a Static VAR Compensator (SVC) coupled Hybrid Distribution Static Compensator (DSTATCOM) for low voltage power distribution system (PDS). A comparative analysisis done between Voltage Source Inverter (VSI)-based DSTATCOM and SVC Hybrid DSTATCOM using Jordan Least Mean Square (JLMS) algorithm to alleviate the shunt-related power quality (PQ) glitches. The specific design is obtained as compared to the existing neural network toolbox algorithm to improve the estimation speed and accuracy. The main objective is to extract the tuned weighted values of fundamental active and reactive power components of distorted load currents for the switching signal generation using an adaptive JLMS algorithm.Several functions of DSTATCOM and hybrid DSTATCOM using this JLMS controller are showcased for harmonics curtailment, power factor (p.f.) improvement, load balancing, voltage regulation, etc. Simulation results on an SVC Hybrid DSTATCOM have shown an acceptable level of performance under unbalanced loading situations. Finally, some comparative results are provided to validate the feasibility and effectiveness of the suggested topology.

Keywords: *DSTATCOM • Hybrid DSTATCOM • JLMS • PQ*

1. Introduction

Research studies on various types of topology for distribution static compensator (DSTATCOM) are gaining more and more attention due to its attractive features in the power distribution system (PDS) application. So, the design of an improved version of DSTATCOM for the power quality (PQ) control is forecasted to obtain reduced inverter capacity and cost. Also, this discussion is accompanied by consideringthe new evolution of current systems due to growing capacity and service-aware demand, etc.(Bayu, 2020; Chilipi et al., 2017; Mangaraj, 2021; Mangaraj et al., 2022a). Though, active filtering using DSTATCOM or D-STATCOM is normally adopted to work out grid harmonic pollution. Still, various types of designs, such as I-DSTATCOM, D-SVC-DSTATCOM and I-SVC-DSTATCOM are considered for the betterment of power delivery,which is deemed highly essential (Sabat et al., 2021; et al., 2016; Zhao et al., 2017). Due to the high effectiveness, accuracy, superiority and feasibility, an improved version of DSTATCOM, I-SVC-DSTATCOM has been carried out as a proposed approach to investigate the performance by extensive research. Hence, the research is going on for analysis of the design of new topology to survive under different loading situationsto maintain healthy PDS with PQ indices as per IEEE-519-2014 guidelines (Lu et al., 2018; Wang et al., 2019). Therefore, the robustness of theproposed DSTATCOM is regarded as a new challenge.

In this research work, using Static VAR Compensator (SVC) and DSTATCOM by coupling each other with the coupling transformer provides better PQ by mitigating the Total Harmonic Distortion (THD) in the distribution system. To improve PQ with better voltage regulation, unit power factor (p.f.), harmonic reduction, high consistency, reduced cost, low loss, and better performance, it is pertinent to choose the SVC-Coupled DSTATCOM; as a result,

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coupling of SVC and DSTATCOM has been raised as a research point for the researchers (Sabat et al., 2022a; Wang et al., 2017a).Based on the above analysis, this paper aims to investigate the stability of SVC-supported DSTATCOM under different loading conditions.

By providing some triggering pulses to the SVC the current flowing to the anti-parallel thyristors shown in the SVC part will not be controlled dynamically,and so some inductors are connected to each anti-parallel thyristor part to control the system (Sabat et al., 2022b; Wang et al., 2017b). The SVC part can relentlessly provide reactive power to maintain the stability of the transmission. All the electrical loads will produce the reactive power and they will absorb too. The reactive power balance in the grid will vary slowly because the transmitted load varies significantly from hour to hour. So, to dampen the power oscillations, the SVC in the transmission system plays a very significant role. The load currents are mainly collected or extracted from the PCC (Mangaraj, 2021; Mangaraj et al., 2022b; Mangaraj et al., 2022c; Puhan et al., 2021; Sabat et al., 2021; Wang et al., 2017c; ZangenehBighash et al., 2018).So, here Voltage Source Inverter (VSI) or DSTATCOM is the main custom power device that can be used for the mitigation of the harmonics and other PQ issues to get a reliable power supply from the power system. The foremost objective of DSTATCOM is to control the flow of the reactive power. Furthermore, the conventional DSTATCOM and SVC coupled Hybrid DSTACOM using Jordan Least Mean Square (JLMS) control technique is tested under unbalanced loading with a response time from 0.6 s to 0.7 s and compared based on PQ issues and DC-link voltage reduction. The mathematical expressions that are included in this topology are very important and play a crucial role in the mitigation of PQ issues. So, by implementingthe JLMS Algorithm, we can enhance the PQ of PDS.

The organisation of this paper is as follows: Section 2 describes the distribution systems including the controllers. In Section 3, the JLMS control algorithm is discussed. Section 4 presents the shunt-related PQ issues and Simulink results of topologies are presented. In Section 5, the conclusions are presented.

2. Circuit Description of SVC Coupled Hybrid DSTATCOM

The shunt harmonic current compensation in 3-phase 3-wire PDS using SVC-Coupled Hybrid DSTATCOM is illustrated in Figure 1. In Figure 1, the SVC coupled with the conventional DSTATCOM is used for the elimination of the THD.The signals for the switching devices of the inverters are produced by the JLMS control techniques, and the detailed control strategy is described below in Section-3.

3. Design of Control Strategy

The proposed JLMS uses a supervised neural network structure but has trained the data by using the recurrent learning principle. The JLMS uses the product of the sum of input components having the linear summation of a single hidden layer and the product of processing units at the output layer, instead of the sum of the product of inputs as in other networks. The three-phase current i_{la}, i_{lb}, i_{lc} and in-phase unit voltage template u_{pa}, $u_{pb,}u_{pc}$ which are considered as the nth input to the input layer. Here, $\alpha\&\gamma$ are chosen as feedback gains. The notation w_o and $w_{pa}(n-1)$ are used for initial and previous weight respectively (Makkar et al., 2018; Nayak et al., 2014; Şen et al., 2020). Finally, w_{pa}, w_{pb}, w_{pc} are considered as the updated weight. The generalisation of updated weight can be trained by using the aforementioned input factor using a suitable learning principle which is presented below and depicted in Figure 2. The JLMS control technique is deployed to enhance the PQ of PDS and reduce the computational complexities which generally occur in the conventional system. The significant harmonics reduction and p.f.improvement are achieved using the proposed system.

$$w_{pa}(n) = w_o + w_{pa}(n-1)u_{pa}(n) + \alpha\gamma\left\{i_{la}(n)w_{pa}(n-1)u_{pa}(n)\right\}u_{pa}(n) \quad (1)$$

$$w_{pb}(n) = w_o + w_{pb}(n-1)u_{pb}(n) + \alpha\gamma\left\{i_{lb}(n) - w_{pb}(n-1)u_{pb}(n)\right\}u_{pb}(n) \quad (2)$$

$$w_{pc}(n) = w_o + w_{pc}(n-1)u_{pc}(n) + \alpha\gamma\left\{i_{lc}(n) - w_{pc}(n-1)u_{pc}(n)\right\}u_{pc}(n) \quad (3)$$

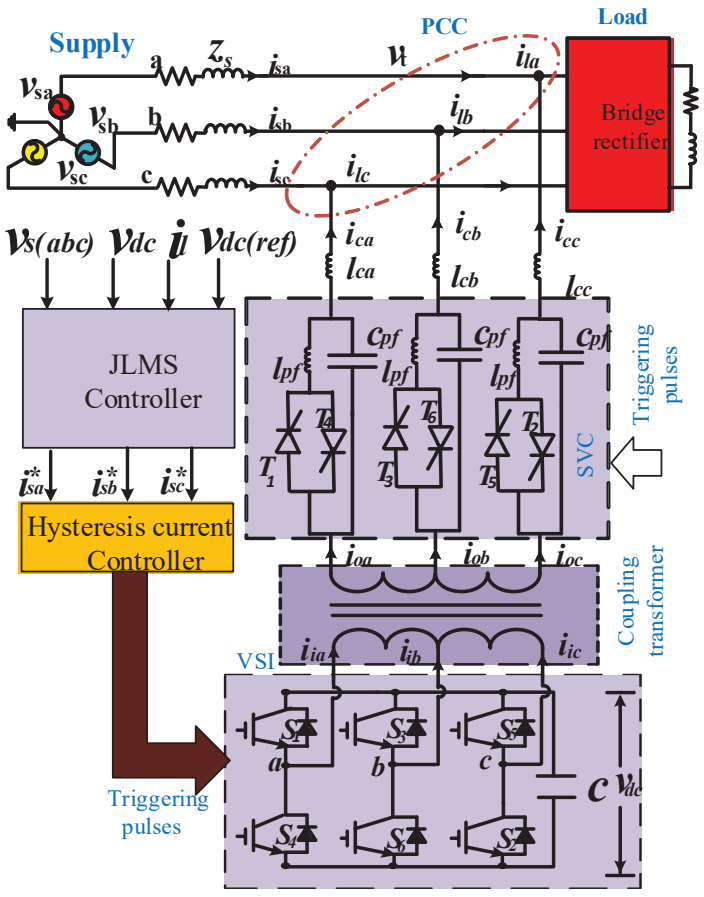

Fig. 1. Circuit Configuration of PDS with SVC coupled Hybrid DSTATCOM.DSTATCOM, distribution static compensator; JLMS, Jordan least mean square; PDS, power distribution system; SVC, static VAR compensator; VSI, voltage source inverter.

Similarly, the extraction of weighting values of fundamental reactive component of load current (w_{qa}, w_{qb}, w_{qc}) can be calculated as:

$$w_{qa}(n) = w_o + w_{qa}(n-1)u_{qa}(n) + \alpha\gamma\left\{i_{la}(n) - w_{qa}(n-1)u_{qa}(n)\right\}u_{qa}(n) \tag{4}$$

$$w_{qb}(n) = w_o + w_{qb}(n-1)u_{qb}(n) + \alpha\gamma\left\{i_{lb}(n) - w_{qb}(n-1)u_{qb}(n)\right\}u_{qb}(n) \tag{5}$$

$$w_{qc}(n) = w_o + w_{qc}(n-1)u_{qc}(n) + \alpha\gamma\left\{i_{lc}(n) - w_{qc}(n-1)u_{qc}(n)\right\}u_{qc}(n) \tag{6}$$

The mean values of weighting values (w_a) of phase 'a', 'b' and 'c' active component is calculated as follows:

$$w_a = \frac{w_{pa} + w_{pb} + w_{pc}}{3} \tag{7}$$

Similarly, the mean value of weighting values (w_r) of phase 'a', 'b' and 'c' reactive components is calculated as follows:

$$w_r = \frac{w_{qa} + w_{qb} + w_{qc}}{3} \tag{8}$$

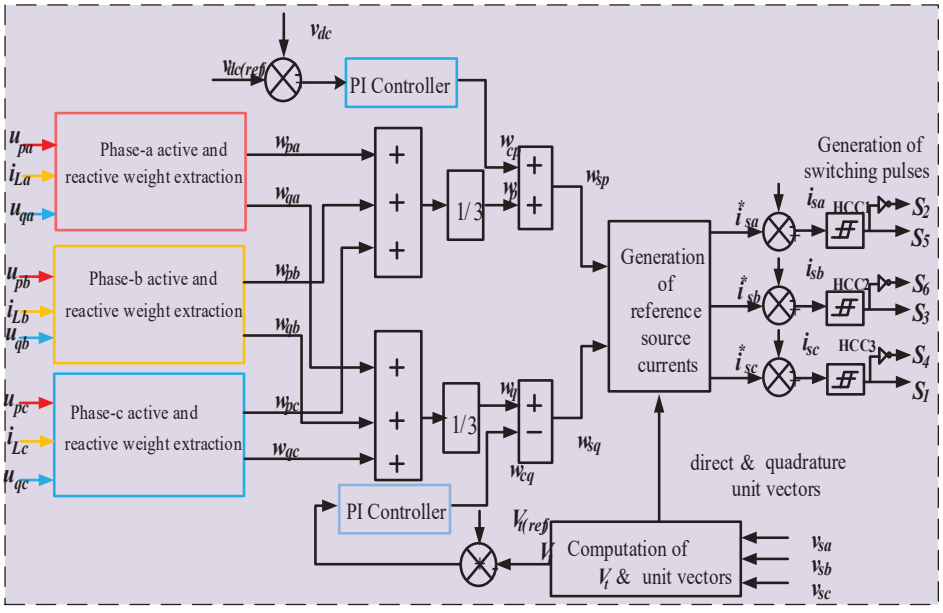

Fig. 2. JLMS control for VSI switching. JLMS, Jordan least mean square; PI, proportional-integral; VSI, voltage source inverter.

The in-phase unit voltage templates (u_{pa}, u_{pb}, u_{pc}) are the relation of phase voltages & amplitude of PCC voltage (v_t) estimated as follows:

$$u_{pa} = \frac{v_{sa}}{v_t}, u_{pb} = \frac{v_{sb}}{v_t}, u_{pc} = \frac{v_{sc}}{v_t} \tag{9}$$

The quadrature unit voltage templates (u_{qa}, u_{qb}, u_{qc}) are the relation of phase voltages as follows:

$$u_{qa} = \frac{u_{pb} + u_{pc}}{\sqrt{3}}, u_{qb} = \frac{3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}, u_{qc} = \frac{-3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}} \tag{10}$$

Where v_t can be expressed as

$$v_t = \sqrt{\frac{2\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2\right)}{3}} \tag{11}$$

The difference between reference DC voltage and sensed DC voltage is the error in DC voltage (v_{de}) can be expressed as

$$v_{de} = v_{dc(ref)} - v_{dc} \tag{12}$$

This difference is processed through the proportional-integral (PI) controller to control the constant DC bus voltage. The output of the PI controller can be expressed as

$$w_{cp} = k_{pa} v_{de} + k_{ia} \int v_{de} dt \tag{13}$$

The sum of the output of the PI controller and the average magnitude of the active component of load currents is the total active components of the reference source current can be expressed as

$$w_{sp} = w_a + w_{cp} \tag{14}$$

The difference between reference ac voltage and sensed amplitude of ac bus voltage is the error in ac voltage (v_{te}) can be expressed as

$$v_{te} = v_{t(ref)} - v_t \tag{15}$$

This difference is processed through the PI controller to maintain the constant ac bus voltage. The output of the PI controller can be expressed as

$$w_{cq} = k_{pr} v_{te} + k_{ir} \int v_{te} dt \tag{16}$$

The difference between the output of the PI controller and the average magnitude of the reactive component of load currents is the total reactive components of the reference source current can be expressed as;

$$w_{sq} = w_r - w_{cq} \tag{17}$$

Three-phase instantaneous reference source active components are estimated by multiplying in phase unit voltage template and active power current component and these are obtained as

$$i_{aa} = w_{sp} u_{pa}, i_{ab} = w_{sp} u_{pb}, i_{ac} = w_{sp} u_{pc} \tag{18}$$

Similarly, three-phase instantaneous reference source reactive components are estimated as

$$i_{ra} = w_{sq} u_{qa}, i_{rb} = w_{sq} u_{qb}, i_{rc} = w_{sq} u_{qc} \tag{19}$$

The summation of active and reactive components of current is called reference source currents and these are obtained as

$$i_{sa}^* = i_{aa} + i_{ra}, i_{sb}^* = i_{ab} + i_{rb}, i_{sc}^* = i_{ac} + i_{rc} \tag{20}$$

Both actual source currents (i_{sa}, i_{sb}, i_{sc}) and the reference source currents $\left(i_{sa}^*, i_{sb}^*, i_{sc}^*\right)$ of the respective phases are compared then current error signals are fed to a Hysteresis current controller (HCC). Their outputs are used to feed the insulated-gate bipolar transistors (IGBTs) s_1 to s_6 of the VSI (Voltage Source Inverter) served as a DSTATCOM.

4. Results Discussion

In this section, using the MATLAB/Simulink tool, the performance of VSI-based DSTATCOM and SVC Coupled Hybrid DSTATCOM are examined. The system's parameters are shown in Table 1. Unbalanced loading conditions are used for operating the DSTATCOM and SVC-supported Hybrid DSTATCOM. Through efficient reactive power compensations and harmonic current compensation, the Hybrid DSTATCOM raises PQ. Unbalanced loads are connected to the PCC of PDS to show the techniques' resiliency. All the simulation waveforms are captured with the simulation step size 1s using discrete simulation type where atustin type solver is used for 50 μs sample time.

4.1. Performance of DSTATCOM under an unbalanced condition

The performance of the traditional DSTATCOM is verified under an unbalanced load using the JLMS controller in this subsection. The system is initially run at 230V without Coupling DSTATCOM at PCC (Point of Common Coupling) and it is noticed that the load side THD is 19.45%. Before compensation, the load side distortion and source side are identical. The source side THD is measured at 4.55%when the DSTATCOM is switched ON. The performance of the compensator observed during unbalanced load from 0.6 s to 0.7 s, is presented in Figure 3. The FFT (Fast Fourier Transform) analysis of source current and load current are presented in Figure 4(i) and 4(ii).

Parameters	Magnitude
AC Proportional controller (K_{pr})	0.2
3-phase voltage (v_s)	230 V
DC link capacitor (C_{dc})	2,000 μF
DC Proportional controller (K_{pa})	0.01
DC link voltage (v_{dc} (ref))	700 V
DC Integral controller (K_{ia})	0.05
Fundamental frequency (f_s)	50 Hz
Resistance (R_c)	0.25 Ω
Inductance (L_s)	2 mH
Resistance (R_s)	0.5 Ω
Inductance (L_c)	1.5 mH
Inductance (L_l)	20 mH
Resistance (R_l)	10 Ω
Switching frequency	15 kHz
IGBT dead time	2 μs
Transformer	3 KVA, 415 V
SVC inductor value	5 mH

IGBT, insulated-gate bipolar transistor; SVC, Static VAR Compensator.

Table 1. Parameters magnitude for testing the proposed system.

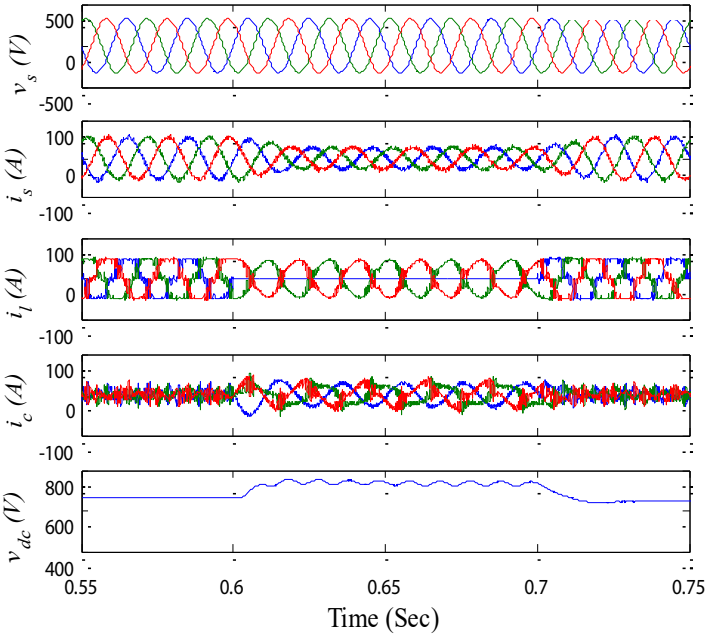

Fig. 3. Analysis of DSTATCOM under unbalanced loading using JLMS control technique from top to bottom; Supply voltage, Source current, Load current, Compensator current and DC-link voltage.DSTATCOM, distribution static compensator; JLMS, Jordan least mean square.

The maximum DC link voltage is observed at 680V from the simulation results. The characteristics of source voltage, source current, load current, compensator current, and DC-link voltage utilising JLMS controller with RL (Resistance and Inductance) load are shown in Figure 3. Here, the traditional DSTATCOM is tested with an RL load using the JLMS controller.

4.2. FFT Analysis

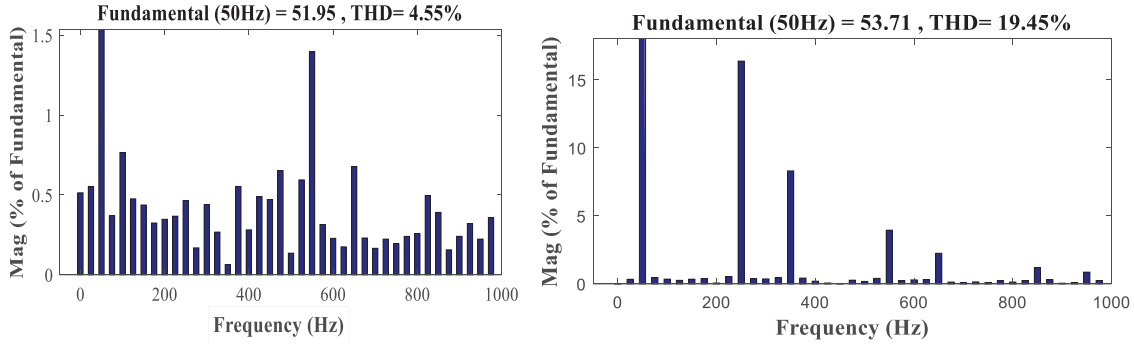

Fig. 4. (i) FFT analysis of DSTATCOM Source current THD. (ii). FFT analysis of DSTATCOM Load current THD.DSTATCOM, distribution static compensator; THD, total harmonic distortion.

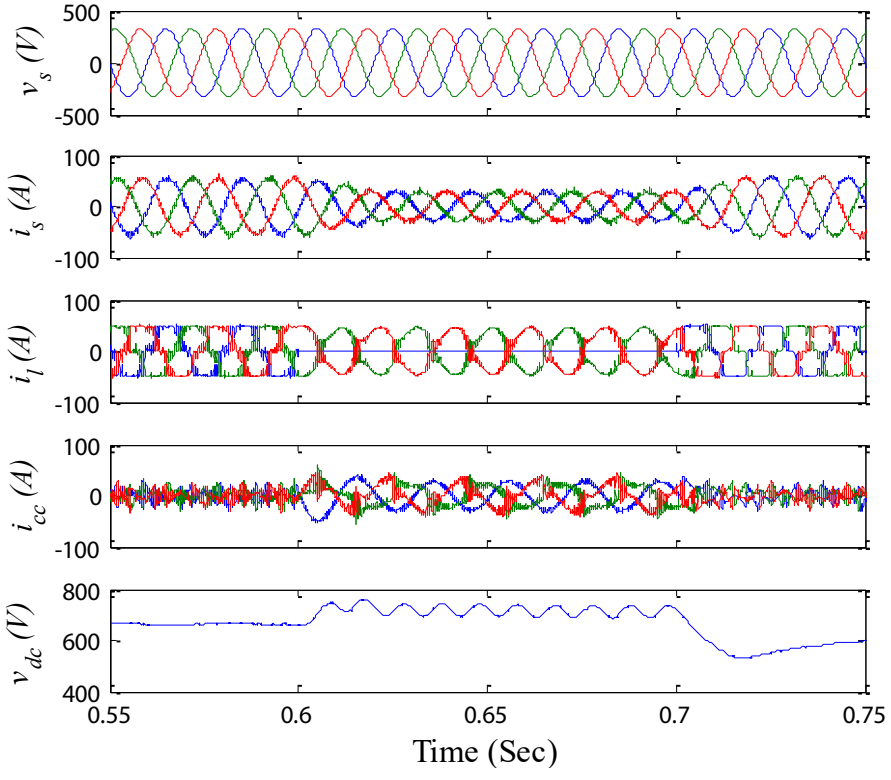

Fig. 5. Analysis of SVC coupled Hybrid DSTATCOM under unbalanced loading using JLMS control technique from top to bottom; Supply voltage, Source current, Load current, Compensator current and DC-link voltage.DSTATCOM, distribution static compensator; JLMS, Jordan least mean square; SVC, static VAR compensator.

4.3. Performance of SVC coupling Hybrid DSTATCOM under an unbalanced condition

The performance of the suggested Hybrid SVC coupling DSTATCOM is verified under an unbalanced load using the JLMS controller in this subsection. The system is initially run at 230V without Coupling DSTATCOM at PCC and it is noticed that the load side THD is 19.76%.

Before compensation, the load side distortion and source side are identical. The source side THD is measured at 3.25%when the DSTATCOM is switched ON. The performance of the Hybrid compensator observed during unbalanced load from 0.6 s to 0.7 s, is presented in Figure 5. The FFT analysis of source current and load current

are presented in Figure 6(i) and 6(ii). The maximum DC link voltage is observed at 620V from the simulation results. The characteristics of source voltage, source current, load current, compensator current, and DC-link voltage utilising JLMS controller with RL load are shown in Figure 5. The bar chart analysis is shown in Figure 7 and the comparative analysis among different parametersof both topologies are arranged in Table 2. Here, the proposed Hybrid DSTATCOM is tested with an RL load using the JLMS controller and shows its effectiveness better compared to the traditional one.

4.4. FFT Analysis

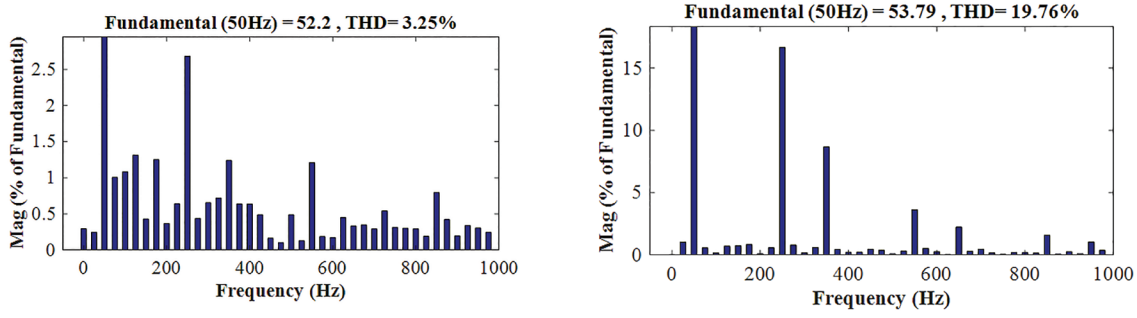

Fig. 6. (i) FFT analysis of Hybrid DSTATCOM Source current THD. (ii) FFT analysis of Hybrid DSTATCOM Load current THD.DSTATCOM, distribution static compensator; THD, total harmonic distortion.

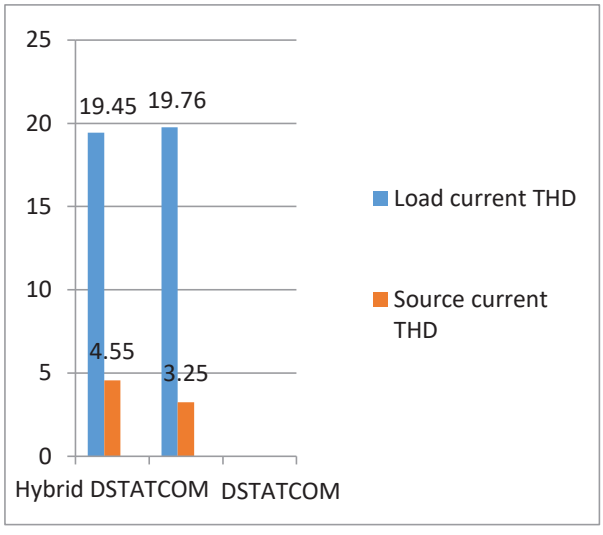

Fig. 7. THDAnalysis of the suggested Hybrid DSTATCOM and traditional DSTATCOM using a bar chart.DSTATCOM, distribution static compensator; THD, total harmonic distortion.

Topology	THD%(supply current)	DC-link voltage	Power factor
Hybrid DSTATCOM	3.25%	620V	0.875
DSTATCOM	4.55%	680V	0.891

DSTATCOM, Distribution Static Compensator; THD, Total Harmonic Distortion.

Table 2. Performance parameter.

5. Conclusion

This study successfully examined the performance of HybridDSTATCOM under PQ improvement. The inference from the simulation results of Hybrid DSTATCOM satisfiesthe benchmark value of the IEEE-519-2014standard. From the above analysis, it is observed that the proposed Hybrid DSTATCOM has superior and robust control ability for providing a better PQ solution over traditional DSTATCOM.Also, it can be expected that the JLMS controller will be a suitable measure for providing a better PQ solution in the PDS for various choices of loading conditions. Hence, the presented results can be considered as the promising performance of SVC coupled Hybrid DSTATCOM usingthe JLMS control technique for future distributed demand-side management and distributed generation systems. To achieve better PQ control, the proposed JLMS can be also modified, which is further applied to other applications.

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