sciendo
Power Electronics and Drives
Volume 8(43), 2023 DOI: 10.2478/pead-2023-0007

Current-zero-crossing Shift for Compensation of Dead-time Distortion in Pulse-width-modulated Voltage Source Inverter

Research paper

Dipankar Chatterjee[1,*], Chandan Chakraborty[2], Kaushik Mukherjee[1], Suvarun Dalapati[1]

[1]*Electrical Engineering Department, Indian Institute of Engineering Science and Technology, Shibpur, Howrah, India*
[2]*Electrical Engineering Department, Indian Institute of Technology Kharagpur, Kharagpur, India*

Received: December 22, 2022; Accepted: February 24, 2023

Abstract: Accurate current polarity detection is a major issue for successful compensation of dead-time distortion in pulse-width-modulated (PWM) voltage source inverter. The present study is concerned with the concept of shift in current-zero-crossing due to dead-time distortion compensation that results in error in current polarity detection and thus causes a problem with regard to the successful continuation of compensation. The phenomenon is analysed in detail, along with its dependence on different factors. The proposed concept is validated in digital simulation and also through experimental verification. The study also recommends the possible correction to be incorporated in view of such zero-crossing shift for achieving proper compensation, especially in case of current-sensor-less compensation techniques.

Keywords: *compensation • current polarity • current-zero-crossing shift • dead-time distortion • PWM VSI*

1. Introduction

Pulse-widthmodulated (PWM) voltage source inverters (VSI) constitute the core of most power electronic systems in which DC/AC conversion is required. Numerous examples of such systems are available, such as grid-connected solar inverters, battery-driven vehicles, uninterruptible power supplies (UPS) etc. The PWM technique overcomes the major hurdles for generating a low THD sinusoidal voltage and current at the output. Over the past few decades, research in this area has resulted in different types of inverter topologies. At the same time, modulation and control techniques have been developed to improve the performance of the inverter. This is equally applicable to single-phase and multi-phase inverters or two-level and multilevel inverters. Rąbkowski and Kopacz (2018) propose an extended T-type inverter, a combination of a three-level DC–DC converter and a three-phase inverter. Here, the input inductor and the DC bus capacitors are reduced, but the neutral point potential remains balanced in spite of the low capacitance. With the use of SiC MOSFETs and Schottky diodes, the proposed inverter exhibits a better performance as compared to a system consisting of a boost converter and a T-type inverter. Different topologies associated with Z-source inverter (ZSI) and various modulation strategies that are used to obtain the voltage boosting property of ZSI have been discussed in Roomi's study (2019). This work also focuses on the neutral point formation, which is important in multilevel ZSIs and the limitation of the different modulation methods. In Beniak and Rogowski (2016), an implementation of space vector based pulse-width modulation (SVPWM) algorithm, with reduced number of state changes in power transistors, is presented. It uses a prediction algorithm for analysing transistors' state sequences and for applying those sequences that reduce the number of switches. This causes around 20% decrease in the number of state changes and decreases switching losses of multilevel inverter-fed drive considerably. Bhowmick et al. (2021) proposes an improved DC bus voltage balancing of a SVPWM based three-phase three-level neutral point clamped (NPC)

* *Email: dipankar.rs2018@ee.iiests.ac.in*

photovoltaic (PV) inverter. Here, two strategies have been discussed. The first one is comprised of two stages, namely a three-phase three-level NPC inverter and a three-level boost converter, and the second one has a single stage consisting of only a three-phase three-level NPC inverter. The grid-tied PV system involving single-stage power conversion seems to have a 91.72% maximum efficiency at 20°C, with minimum converter loss of 284.74 W at 45°C, whereas the system involving two-stage conversion has an 89.41% maximum efficiency and a minimum converter loss of 503.23 W at 20°C. The centralised inverter can work as a static synchronous compensator (STATCOM) using the proposed strategy. A novel switched capacitor (SC)-based three-phase seven-level inverter, consisting of a single DC source, which includes eight switches, two capacitors, and one diode per phase leg, has been presented in Jena et al. (2022). This provides self-balancing of the SCs and also the advantages of lower switch voltage stress, inherent voltage gain, and a reduction in the number of switching components.

Dead-time distortion is a regular problem for almost all PWM VSIs, feeding lagging loads (including motor loads), and other linear and nonlinear loads fed through L-C or L-C-L low-pass filters. These include all grid-connected inverters, and inverters used for motion control, as well as for UPS and different industrial applications. It results in a nonlinear relationship between the reference and the actual voltage, causes current distortion, torque pulsation, and additional losses. To eliminate such problems, several strategies and techniques for dead-time distortion compensation have been proposed by researchers over the last few decades. These techniques can broadly be divided into two categories, namely average compensaton technique (Ben-Brahim, 1998) and pulse-by-pulse compensation technique (Leggate and Kerkman, 1997). In both these techniques, accurate current polarity detection is a major requirement for achieving successful compensation.

Yu et al. (2021) present numerical and analytical models of the H-bridge inverter's output spectrum to precisely find the effects of dead-time on the power amplifier switching mode voltage. In Wu et al.'s study (1999), analysis of the output harmonics of the H-Bridge inverter with dead-time has been presented in two ways: the first one represents the PWM signal without dead-time and the second one involves a correction part that represents the effects of the dead-time using double Fourier analysis in the 3-D mode. Monotonically decreasing odd harmonics are obtained from the analytical results, but these are not always correct in practice. In harmonic characteristic analysis methods, mainly double Fourier series is involved (Kumar, 2018). However, it did not take into account the impact of dead-time effects. For switching frequency formulation, if high switching frequencies are considered, then within switching intervals, linear error i.e. constant slope and constant reference current can be assumed. This inaccurate assumption causes errors, due to which the existing formulations are not suitable for precise determination of the switching instants. Chierchie et al. (2014) extended the results of the double Fourier series of PWM waveform, proposed by Black (1953), to take into account the dead-time associated with arbitrary band-limited modulating signals. However, all these methods are applicable to switching function model and are not suitable for application to a time average model (TAM). Also, here the switching transients are neglected. Seyyedzadeh and Shoulaie (2019) propose a more accurate measurement method in offline mode, where the voltage disturbance is measured through Kirchhoff's voltage law under different current amplitudes, considering the nonlinear parameters. However, to fit the current-disturbance curve, massive data are required. In Bedetti et al. (2015), for matching the nonlinear relationship, a piecewise compensation method was proposed. Here, the inverter non-idealities were compensated using the lookup table in a feed-forward manner. This is because the compensation of the complete lookup table having nonlinear equations against temperature effects becomes a very difficult task. In the studies mentioned, some parasitic parameters of inverters are involved, which vary with circuit state and are often approximated. It results in a reduction of compensation accuracy in offline methods. Now, for the low and high currents, the inverter nonlinearity is different and it may result in the errors in nonlinearity estimation for very low currents as explained in Seyyedzadeh et al. (2019), wherein is also proposed a numerical solution to the equation. It is worth mentioning that in the trapezoidal and lookup table methods, the effects of parasitic capacitors, dead-time etc. are considered simultaneously. However, with the variation of the temperature of the inverter, detuning of the stored values of the compensation voltage takes place, which is the main drawback of these techniques. A dead-time compensation scheme, robust to current measurement errors, and using the support vector regression theory, has been presented in Choi et al. (2007). However, precise knowledge of the inverter model and its parameters is required here, and this also involves

high computational efforts. Chierchie et al. (2014) effectively use the analysis of the oscillation issues due to nonlinearities in the half-bridge converter using the describing-function (DF)-based approach. Berg and Roinila (2020) developed a simple model, which cannot be applied for a complex grid-connected PMSG system having cascaded control structures, such as inner current control loop, outer DC voltage control loop, and PLL. The dead-time is distributed in all fundamental cycles in asymmetric manner (Lin, 2002), and accurate calculation of PWM transmission, switching on or off delay time, cannot be executed. Thus, it is unable to provide a very good compensation performance. A number of studies in the literature have discussed the different switching modes associated with the inductor current ripple. If the switch-node voltage is assumed to be the half of the DC bus voltage, when the inductor current is clamped to zero, it involves oversimplified linear approximation of voltage error and gives rise to inaccurate results. In Herran et al. (2013), the control system robustness against parameter variations has been increased using the predictive controller, where adaptive tuning of the parameters within the observer can be achieved. However, the feedback information of the output voltage is required. In Shen and Jiang (2019), real-time current ripple is considered and a dead-time compensation, based on a model-based predictor for current ripple prediction, is proposed. It results in increase in system order, and heavy computational load, which requires a large memory size. If there is a current measurement error, then the dead-time elimination method using current polarity will fail due to the wrong information given by the measured phase currents. A compensation strategy, based on a repetitive controller and finite impulse response (FIR) filters, has been presented in the study of Tang and Akin (2017). The elimination or reduction of dead-time is difficult even with use of a digital-feedback control loop. Anti-alias filters are required for the high-frequency content of the PWM signal. This in turn, imposes a limitation on the feedback gain, which can be used to reject the dead-time perturbation. However, in the inverter mode, the amplitude of the modulation wave is incremented in all the aforementioned dead-time compensation methods. Using the disturbance observer, effective estimation of the disturbance voltage is expected for a wide operating range (Hwang and Kim, 2010). Thus, the operating conditions actually limit the performance of the observer. Moreover, in the sensor-less control system, the rotor angle, which is important for the observer design, can have an inaccuracy. Some existing dead-time compensation approaches fundamentally involve the observer theory (Kim et al., 2003), and usually have good performance in the identification of the disturbance voltage term. However, these suffer several drawbacks such as determining accurate parameter values of the PMSM, tracking of time-varying disturbances by the observer, and time consuming tuning of observer gains. In the methods using current harmonic filtering (Zhao et al., 2004), the 6th harmonic of current in d-q-axes synchronous rotating reference frame is filtered, and compensation voltage is determined therefrom. Although this method never relies on properties of VSI and motor model, it has trouble with the convergence. The voltage distortion due to dead-time can be compensated using the reference voltage waveform, when added with a predetermined compensation signal. However, this introduces an extra hardware detection circuit, which increases the cost and circuit complexity. In Kim and Park (2007), the 6^{th} harmonic is subtracted from d-q-axes reference currents. It involves complicated calculation and also may be affected by outside interferences resulting from the operation of the system. These solutions become ineffective near current-zero-crossing points in grid-tie converters, where high ripples exist. This results in phase currents having a zero current clamp (ZCC) distortion. In the study of Munoz and Lipo (1999), using the low-pass and notch filters, detected current is decomposed into magnitude and phase angle. Thereafter, the current waveform having no ZCC is reconstructed. This method seems to have a decent performance for V/f motor drives. The performance of this method relies on adequate design of the fillers. However, reconstructing phase current in the transient state is difficult and inapplicable to high-performance drives. In Liu et al.'s study (2017), current-zero-crossing points are detected by the inverter terminal voltage sampling in two Dead-time (DT) regions in a sampling cycle. This is done by adding a high-speed AD sampling circuit. However, the switching noise produced by high-frequency switches greatly affects the detection accuracy. This may require complicated signal processing algorithms or extra hardware.

Accurate current-zero-crossing detection is an important issue for successful implementation of the compensation algorithm. The current-zero-crossing points get shifted after implementing compensation. If it is not taken care of, then continuing accurate compensation is not possible, as it involves incorrect current polarity. This phenomenon has not been addressed in the analysis and compensation techniques discussed above. This paper focuses on a detailed analysis of shift in current-zero-crossing due to dead-time distortion compensation and also recommends

the possible correction to be incorporated for achieving proper compensation, especially in case of current-sensor-less compensation techniques.

This article is divided into six sections. Section 2 presents and explains the dead-time effect and its compensation. The shift in current-zero-crossing due to compensation is analysed in Section 3. Application of the proposed concept for achieving successful compensation is discussed in Section 4. Sections 5 and 6 present the results from simulations and experiments, respectively, to validate the above analysis. Section 7 draws the conclusion.

2. Dead-time Effect and its Compensation

A single-phase two-level VSI is shown in Figure 1, where IGBTs T1–T4 are used as switching devices and D1–D4 are the anti-parallel diodes of the corresponding switching devices. The gate pulses for T1–T4 are denoted by g1–g4, respectively. The PWM gate pulses are generated by comparing a sinusoidal modulating wave with a triangular carrier wave. Under ideal conditions, the turning on of one switch and the turning off of the other switch in the same inverter-leg occur at the same instant. In a practical inverter, due to the finite turn-on and turn-off time of switches, a small delay is mandatorily introduced between turning off a switch and turning on the other switch in the same inverter-leg, to avoid the 'shoot-through' phenomenon. This 'delay' is commonly known as 'dead-time' or 'blanking-time'. Figure 1 represents a case-in-point for such a phenomenon, where the dead-time is denoted by 'T_d'. For a heavily inductive load, the presence of this dead-time causes changes in the pulse-widths of the pole voltage (measured w.r.t. negative DC bus), based on current polarity (Figure 2). One such pole voltage v_{AO} is represented in Figure 2 for two different cases of inverter output current i_L. Here, T_{sw} is the switching frequency, which is same as carrier wave frequency T_c. As evident, the pole voltage pulse-widths are reduced due to dead-time when the pole current is positive (i.e. outward) and increased when the pole current is negative (i.e. inward). Such deviation of pulse-width from the ideal value results in considerable distortion in the load voltage waveform, as shown in Figure 3. This distortion, called 'dead-time distortion', introduces low-frequency harmonics in the output voltage, and the actual output voltage will deviate from the desired voltage profile. The average load voltage deviation within each period of load current i_L for a carrier-waveform frequency f_c, DC bus voltage V_{DC}, and dead-time T_d is given by

$$\Delta v_{dt} = -2 f_c T_d V_{DC} sign(i_L) \tag{1}$$

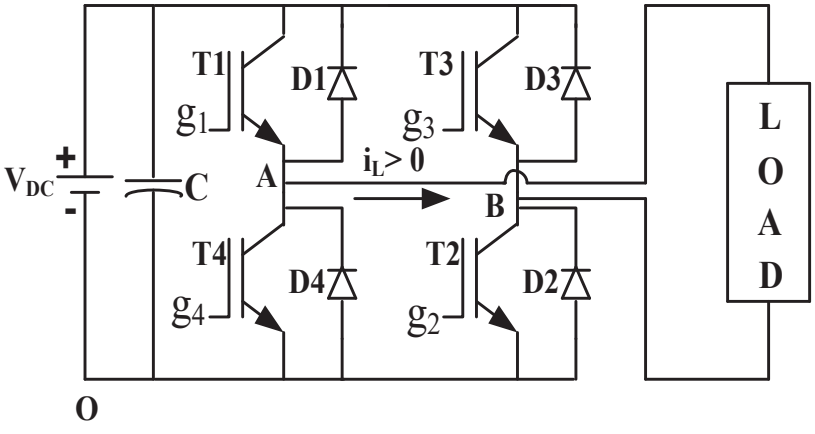

Fig. 1. Single-phase two-level inverter.

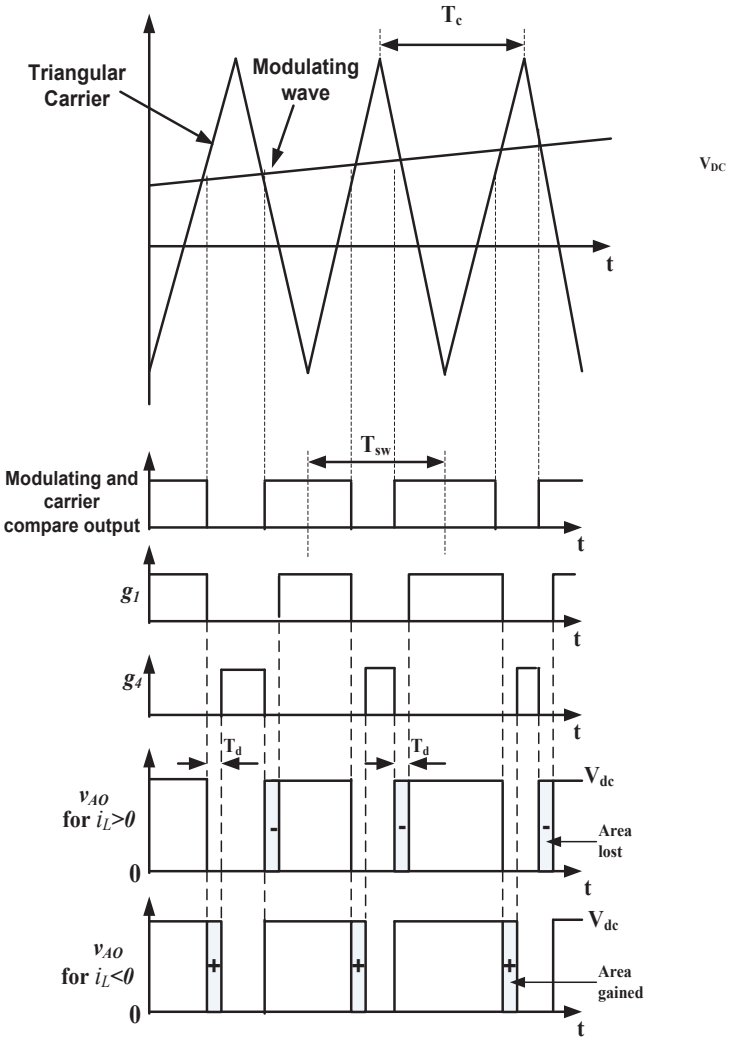

Fig. 2. Dead-time effect on pole voltage measured w.r.t. negative DC bus.

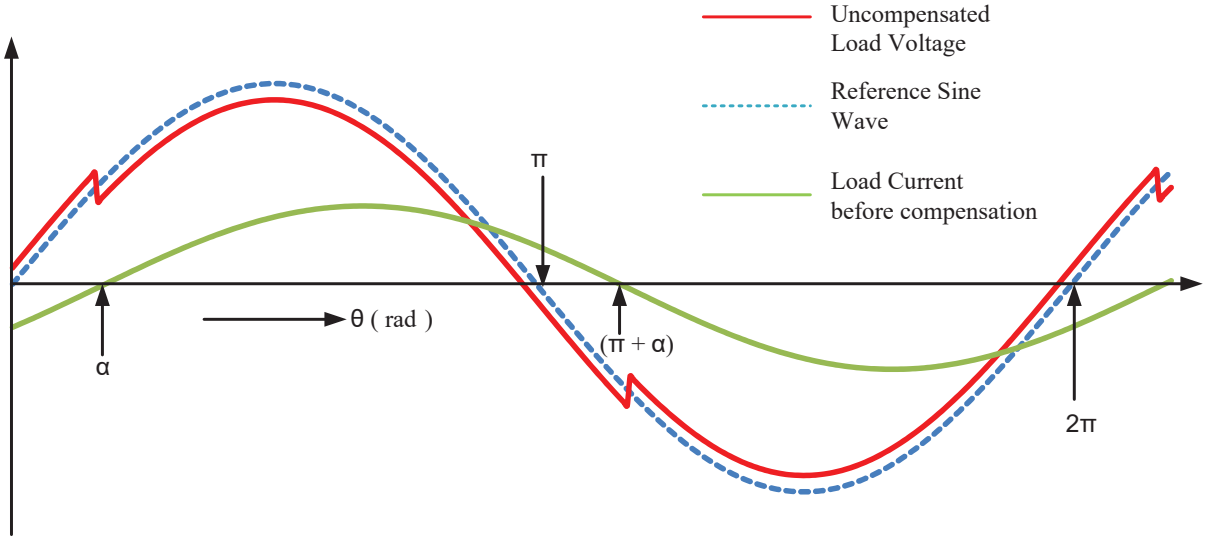

Fig. 3. Illustrating a dead-time distorted load voltage (neglecting high-frequency components) from a PWM inverter; the reference voltage and load current waveforms are also shown.

The effect of this deviation on both the half cycles of the filtered load voltage is shown in Figure 3, where notches exist at positive and negative zero-crossing instants of load current i_L.

There are number of dead-time distortion compensation techniques available. These techniques can be divided into two major categories. The first one is based on averaging theory, where the cumulative effect of dead-time is evaluated over half-cycle of load current and is a comparatively slow process. The modulating wave is adjusted accordingly and can be expressed as

$$v_{rc} = v_r + \left(2n_p f T_d V_{DC}\right) sign\left(i_L\right) \tag{2}$$

where v_r is the original sinusoidal modulating waveform, v_{rc} is the modified modulating waveform to achieve the desired compensation, n_p is the number of voltage deviation pulses per period of load voltage due to dead-time, and f is the fundamental frequency of load voltage.

The second method is pulse-by-pulse compensation, which is faster and more accurate. Here the original modulating waveform is modified based on both current polarity and carrier-waveform slope '*m*', as follows:

$$\begin{aligned} v_{rc} &= v_r + \varepsilon, if\ sgn\left(i_L\right) > 0\ \&m < 0 \\ &= v_r - \varepsilon, if\ sgn\left(i_L\right) < 0\ \&m > 0 \\ &= v_r, otherwise \end{aligned} \tag{3}$$

In both these techniques, the compensating action is achieved either by increasing or decreasing the gate pulse-width of the switches depending on current polarity. Thus, knowledge of the current polarity is mandatory for such dead-time distortion compensation techniques. Continuous research is also being undertaken in relation to current-sensor-less dead-time distortion compensation e.g. using time feedback or terminal voltage A/D conversion of PWM VSI etc.

3. Shift in Current-zero-crossing due to Dead-time Distortion Compensation

As discussed in the preceding section, the PWM voltage across the load undergoes distortion due to the presence of dead-time. Upon passing this load voltage through a suitable low-pass filter, the switching frequency and higher harmonics are attenuated, leaving behind the low-frequency profile of the distorted voltage. This filtered load voltage is presented in Figure 3, and it has notches at current positive and negative zero-crossing instants. Thus, the load voltage now has low-frequency harmonics, which can be analysed using Fourier series expansion. The distorted load voltage can be represented as the difference of a sine wave and a square wave in phase with the load current, as shown in Figure 3. The sine wave may be represented as

$$v_1(\theta) = V_m \sin\theta \tag{4}$$

where $V_m = m_a V_{DC}$, m_a being the amplitude modulation index, and $\theta = \omega t$, where $\omega = 2\pi f$ is the angular frequency of the sine wave in rad/s and t is the time in seconds.

Using Fourier series expansion, the square wave can be represented as

$$v_2(\theta) = \left(4V_2 \big/ \pi\right) \sum_{n=1,3,5,..}^{\infty} \frac{1}{n} \sin n(\alpha - \theta) \tag{5}$$

where $V_2 = 2 f_c T_d V_{DC}$ is the magnitude of square wave, n being the order of harmonics and α being the angular position of the current positive zero-crossing w.r.t. the reference sine wave as indicated in Figure 3.

Now, let $\left(\frac{4V_2}{\pi}\right) / V_m = \left(\frac{8}{\pi}\right)(f_c T_d / m_a) = A$, where A is a constant.

Using Eqs (4) and (5), load voltage can be expressed as

$$v_L(\theta) = V_m \sin\theta - AV_m \sum_{n=1,3,5,..}^{\infty} \frac{1}{n} \sin n(\theta - \alpha) \tag{6}$$

Due to the presence of harmonics in the load voltage, the load-current waveform also undergoes distortion. The contribution of the low-frequency voltage-harmonics is more dominant in this regard. This distortion also affects the amount of time-lag between the original sinusoidal modulating waveform zero-crossing instant and the corresponding load-current zero-crossing instant. Evidently, the value of this time-lag before the dead-time distortion compensation of the load voltage waveform is not same as that after the compensation. This is illustrated in Figure 4. Now, dead-time distortion compensation is itself dependent on the load-current-polarity, which can be derived if load-current zero-crossing instants are known. Thus, dead-time distortion compensation can be successfully achieved if load-current zero-crossing instants are correctly detected. Hence, prior to starting the compensation, the current-zero-crossing instants are first determined. However, if the compensation is continued based on this information, it becomes erroneous, as the time-lag between the voltage- and current-zero-crossing instants changes after dead-time distortion compensation.

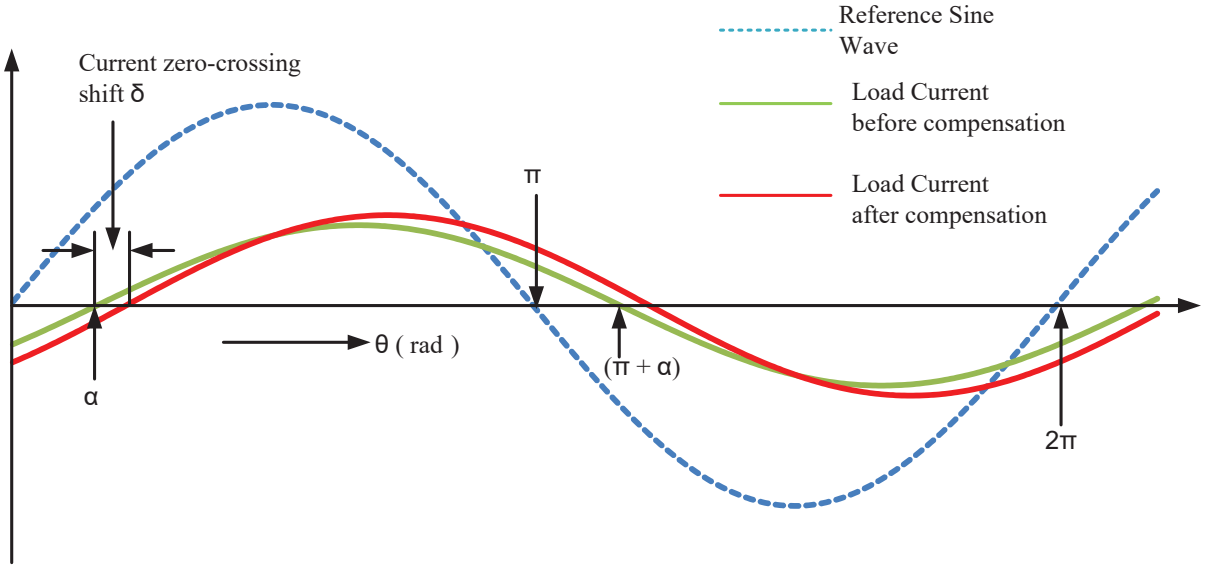

Fig. 4. Illustrating the current-zero-crossing shift after dead-time distortion.

The shift in current-zero-crossing instant can be calculated as follows. Here, R-L load is taken for analysis. Using Eq. (6), load current can be expressed as

$$i_L(\theta) = \frac{V_m \sin(\theta - \tan^{-1} p)}{R\sqrt{1+p^2}} - \frac{AV_m}{R} \sum_{n=1,3,5,..}^{\infty} \frac{1}{n\sqrt{1+n^2p^2}} \sin\{n(\theta-\alpha) - \tan^{-1} np\} \tag{7}$$

where R is load resistance, L is load inductance, $\varphi = \tan^{-1}\frac{\omega L}{R}$ is load impedance angle, and $p = \omega L/R$.

At $\theta = \alpha$, $i_L(\theta) = 0$.

$$\delta = \varphi - \alpha = \sin^{-1}\left[Ap\sqrt{1+p^2} \sum_{n=1,3,5,..}^{\infty} \frac{1}{1+n^2p^2} \right] \tag{8}$$

Thus, Eq. (8) represents the shift in current-zero-crossing δ due to dead-time distortion compensation. Here, φ and α indicate the instants of load-current zero-crossing w.r.t. sine modulating waveform after and before dead-time distortion compensation, respectively, measured in equivalent radians.

Spread-sheet based calculation has been carried out to evaluate the magnitude of δ using Eq. (8). The results are shown in Figure 5 over load impedance angle values ranging from 20° to 80°. Here, f_c 10 kHz, T_d = 4 µs, and m_a = 0.7, so that A = 0.1456. It may be stated that the magnitude of this shift increases as load impedance angle increases.

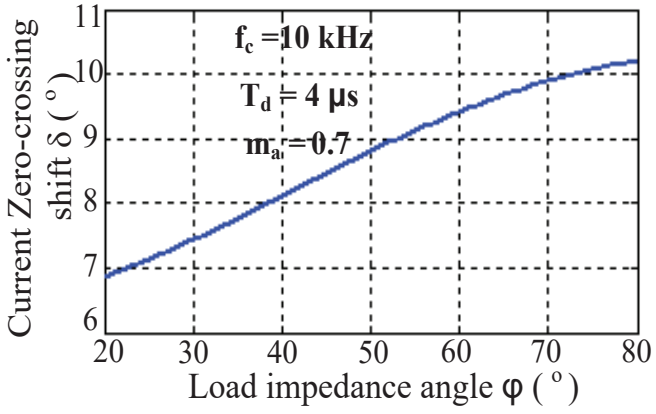

Fig. 5. Variation of current-zero-crossing shift δ (°) with load impedance angle φ (°).

At φ = 90°, δ is maximum and its value is given by

$$\delta = \lim_{p\to\infty} \sin^{-1}\left[A \sum_{n=1,3,5,..}^{\infty} \frac{\sqrt{\left(1+\frac{1}{p^2}\right)}}{\left(\frac{1}{p^2}+n^2\right)} \right] = \sin^{-1}\left(\frac{\pi^2 A}{8}\right) \tag{9}$$

From Eq. (9), it is observed that δ also depends on A, which can be changed with variation of f_c, T_d, and m_a. Here, f_c, T_d, and V_{DC} are assumed to remain constant and variation of current-zero-crossing shift due to variation in m_a has been studied using spread-sheet based calculation. The variation of current-zero-crossing shift w.r.t. m_a and φ is shown in Figure 6.

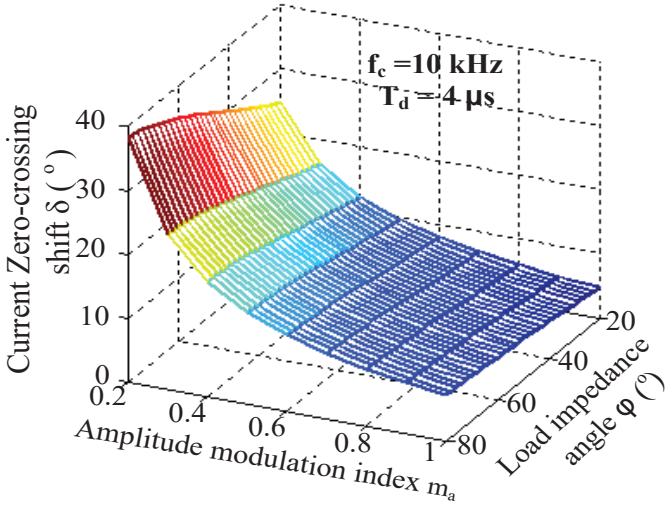

Fig. 6. Variation of current-zero-crossing shift δ (°) w.r.t. load impedance angle ϕ (°) and amplitude modulation index m_a.

It can be observed from Figure 5 that δ decreases with decrease in φ and with increase in m_a. But as m_a increases, the decrease in δ is much larger. Thus, δ is more sensitive to changes in m_a than in φ. The dead-time distortion effect is represented by a square wave and can be mathematically represented using Fourier series expansion as in Eq. (5). As the number of harmonics used for such representation is reduced, the deviation of this representation from square wave is increased. Hence, error in the calculation of δ also increases. The error in calculation w.r.t. both the order of harmonics, taken into consideration, and load impedance angle is shown in Figure 7, whereas Figure 8 shows the corresponding result w.r.t. the order of harmonics n taken for calculation, and m_a. From Figure 7, it can be observed that error increases with decrease of φ but it increases at a much higher rate with decrease of n. From Figure 8, it can be seen that variation in error is much smaller over a wide range of m_a. This shows a predominant effect of low-frequency harmonics on δ. Thus, error in calculation may be reduced to an acceptable limit for all values of m_a and φ, if higher number of harmonics are also taken into consideration.

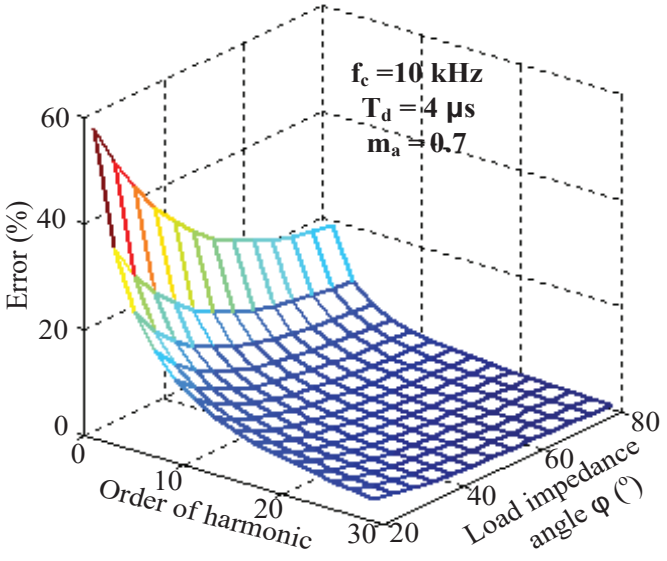

Fig. 7. Error (%) in current-zero-crossing shift calculation with variation in load impedance angle, ϕ (°), and order of harmonics taken, n, for calculation.

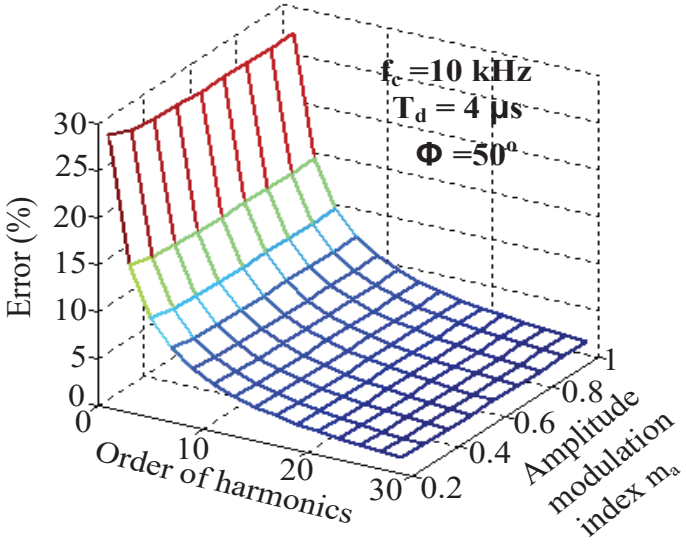

Fig. 8. Error (%) in current-zero-crossing shift calculation with variation order of harmonics, n, taken for calculation and amplitude modulation index m_a.

4. Application of Proposed Concept in Dead-time Distortion Compensation

Thus, from above discussion it is observed that there is a shift of the current-zero-crossing instant w.r.t. the reference waveform, prior to and after dead-time distortion compensation. In case current sensors are used to sense the pole current, such shift is automatically detected. However, for current-sensor-less dead-time distortion compensation, the accurate detection or estimation of current-zero-crossing shift may be very important for proper current polarity detection. If, for example, current-zero-crossing position and corresponding current polarity are determined by detecting notch positions of dead-time distorted inverter output voltage waveform prior to dead-time distortion compensation, and used for compensating the dead-time distortion, then incorrect compensation will result due to current-zero-crossing shift post compensation. It is observed that the current-zero-crossing shift depends on the load impedance angle and also on the amplitude modulation index of the inverter. Thus, the shift may be computed corresponding to a load impedance angle for a given inverter output amplitude. A family of look up tables may be formed for the variation in δ w.r.t. the variation in ϕ. In each look up table, the value of m_a may be taken as a constant parameter, while the dead-time value and switching frequency are constant for all the plots. The correction may then be applied by adding this shift, obtained from the look up table, with the detected current-zero-crossing position (based on notch positions in the uncompensated voltage waveform) to determine the actual current-zero-crossing position after starting the compensation.

5. Simulation Results

Numerical simulation has been carried out to verify the proposed current-zero-crossing shift calculation. The block-diagrammatic representations of the simulation model with and without dead-time distortion compensation is presented in Figure 9. In this paper, current sensor has been used in the experimentation-process to obtain

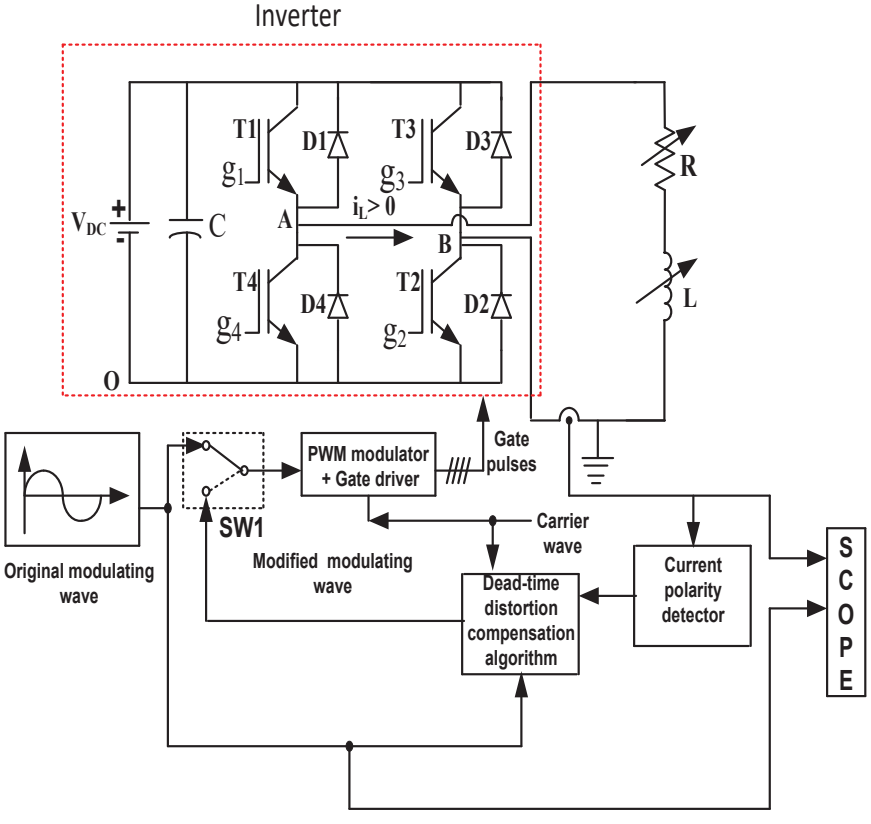

Fig. 9. Simulation block diagram of single-phase inverter with and without dead-time distortion compensation.

the current-zero-crossing positions before and after compensation and the corresponding shifts for different load impedance angles, which has been used in the dead-time distortion compensation block. The other two inputs to this compensation block are carrier wave and original sinusoidal modulating wave, which is generated internally within the controller. Using these three inputs, the compensation block sets up the modified modulating waveform for correct compensation by suitable addition or subtraction of the compensating component. The PWM modulator obtains the original modulating wave or its modified form for compensation through a single pole-selector switch, and gate pulses are generated for the inverter accordingly. The current waveform along with the reference sine modulating waveform are observed on the oscilloscope. This helps to determine the shift in current-zero-crossing. Some sample results are presented here to validate the discussions and analysis as presented in the previous sections.

The parameters for simulation of inverter with R-L load are given in Table 1. Figures 10 and 11 show two sample results for load impedance angles of 30° and 60°, respectively. It is clearly observed that dead-time distortion compensation has been applied at $t = 0.1$ s, due to which there is a shift in current-zero-crossing that has been measured w.r.t. the original sine modulating waveform. The theoretical calculation of current-zero-crossing shift has been carried out by taking up to the 99th harmonic for representing the square wave discussed in Section 2. The calculated values of current-zero-crossing shift for different load impedance angles are compared with the corresponding values in simulation and are shown in Figure 12.

Simulation parameters	Values
V_{DC}	220 V
Load impedance magnitude	5.1 Ω
Load impedance angle (φ)	Varying between 20° and 80°
m_a	0.7
Carrier wave amplitude	1 p.u.
Reference wave amplitude	0.7 p.u.

Table 1. Simulation parameters.

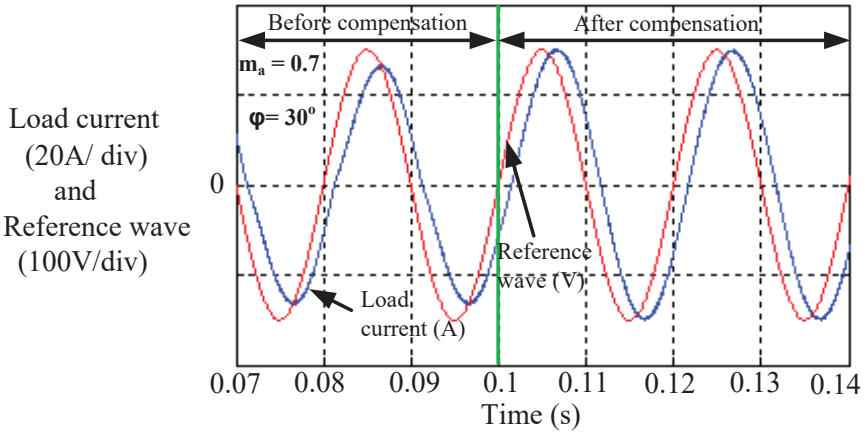

Fig. 10. Illustrating current-zero-crossing shift after compensation: load current (A) (blue) and reference waveform (red) for load impedance angle 30° before and after compensation for R-L load.

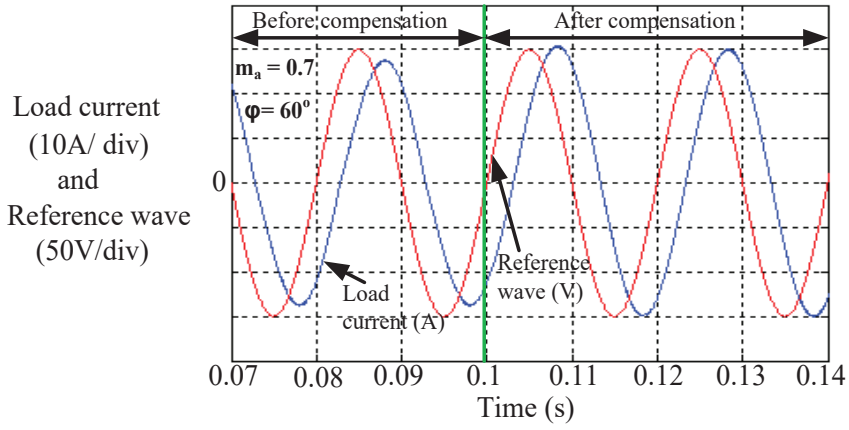

Fig. 11. Illustrating current-zero-crossing shift after compensation: load current (A) (blue) and reference waveform (red) for load impedance angle 60° before and after compensation for R-L load.

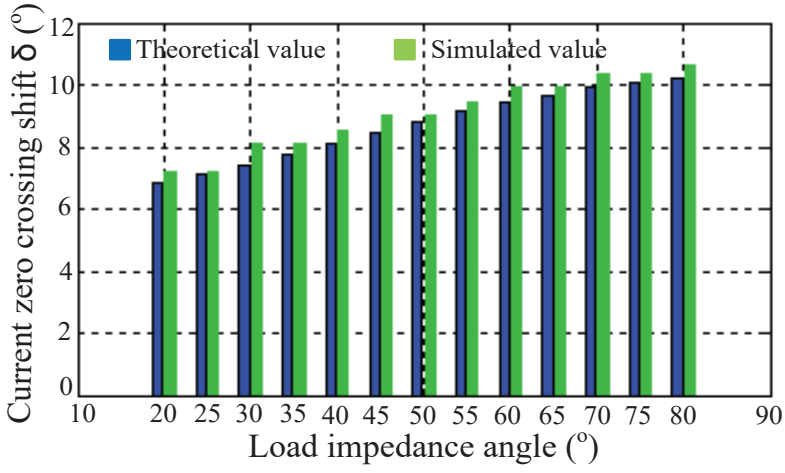

Fig. 12. Comparison of theoretical and simulated current-zero-crossing shift after compensation for different load impedance angles for R-L load.

6. Experimental Results

To validate the proposed concept, the hardware implementation of a pulse-by-pulse compensation of dead-time distortion has been carried out in the laboratory using a controller-card, based on an 8-bit mid-level digital controller, Microchip make PIC18F4431. Semikron-make IGBT-based inverter stack has been used as PWM VSI with 220 V DC bus voltage. The experiment has been performed with R-L load using resistances and inductances available in the laboratory. The different parameters used in the experimental model are given in Table 2.

Experimental parameters	Values
V_{DC}	220 V
Load resistance and inductance	Combining different values as available in the laboratory
Load impedance angle (φ)	Varying between 20° and 80°
m_a	0.7
Carrier wave amplitude	1 p.u.
Reference wave amplitude	0.7 p.u.

Table 2. Experimental parameters.

Experimental data have been taken for a range of load impedance angles as indicated in Table 3. The resistance of the inductor coil and change of resistance value due to heating effect during the experiment have also been considered for load impedance angle calculation. Figure 13 shows the experimental arrangement. The load current and the reference sine wave are shown in Figure 14 before compensation and in Figure 15 after compensation. Here, the current-zero-crossing position has been determined w.r.t. sine modulating wave. The current-zero-crossing position w.r.t. the corresponding zero-crossing position of the original sinusoidal modulating waveform has been clearly indicated before and after compensation by Δt_1 and Δt_2 in Figure 14 and Figure 15, respectively. It can be observed that before compensation, Δt_1 = 750 μs, and after compensation, Δt_2 = 1,200 μs. Hence, in this case, the 'shift' in current-zero-crossing turns out to be $\Delta t_2 - \Delta t_1$ = 450 μs, which is equivalent to 8.1° for a 50 Hz waveform. The shift in current-zero-crossing obtained experimentally for different load impedance angles are compared with theoretical and simulation results and given in Table 3. From this table, it can be stated that experimental values of current-zero-crossing shift are near to that obtained theoretically.

Load impedance angle (°)	Theoretical angle shift (°)	Angle shift from simulation (°)	Angle shift from experiment (°)
21	6.91	7.2	7.2
23	7.02	7.2	7.2
28	7.31	8.1	7.2
32	7.57	8.1	8.1
34	7.7	8.1	8
36	7.84	8.1	8
38	8	8.5	8.1
46	8.54	9	9
49	8.74	9	9
58	9.3	9.9	9.9
64	9.63	9.9	10.1
70	9.9	10.35	10.1
76	10.1	10.35	10.6

Table 3. Shift in current-zero crossing due to dead-time distortion compensation.

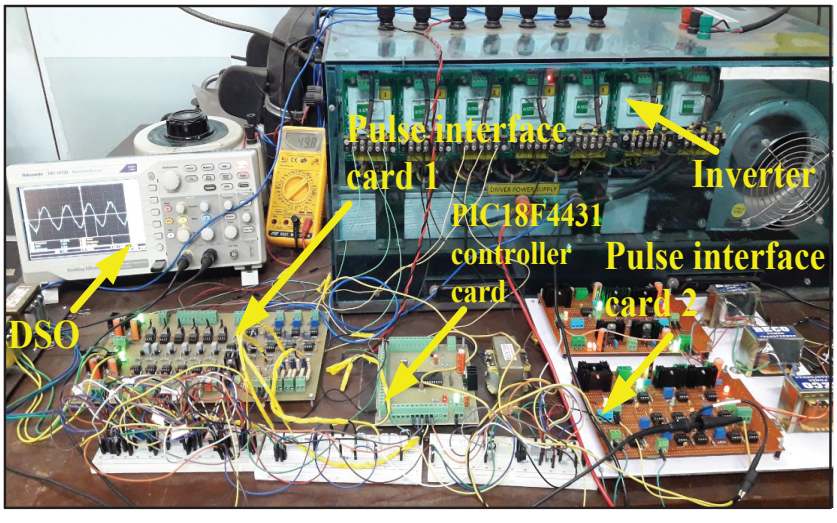

Fig. 13. Experimental set-up.

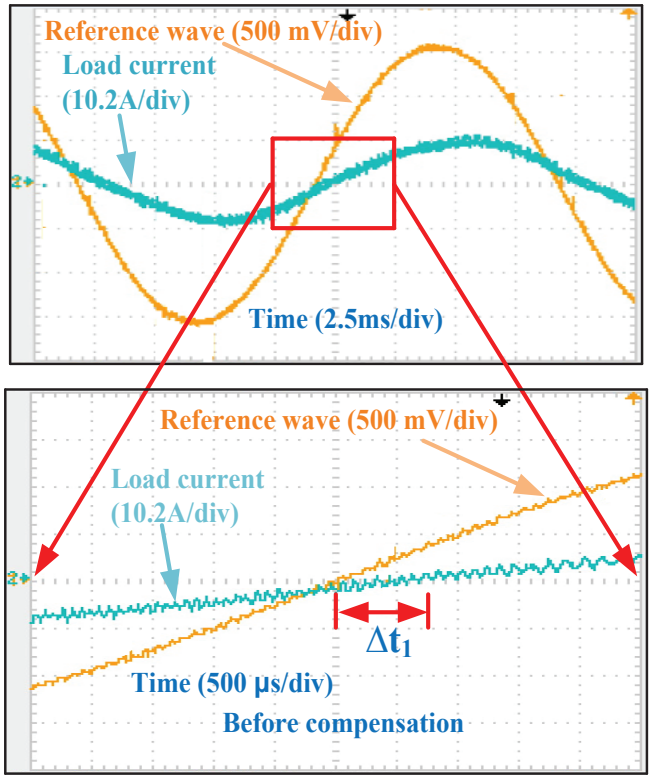

Fig. 14. Load current (blue) (10.2 A/div) and reference waveform (yellow) (500 mV/div) for load series impedance angle 32° before compensation for R-L load.

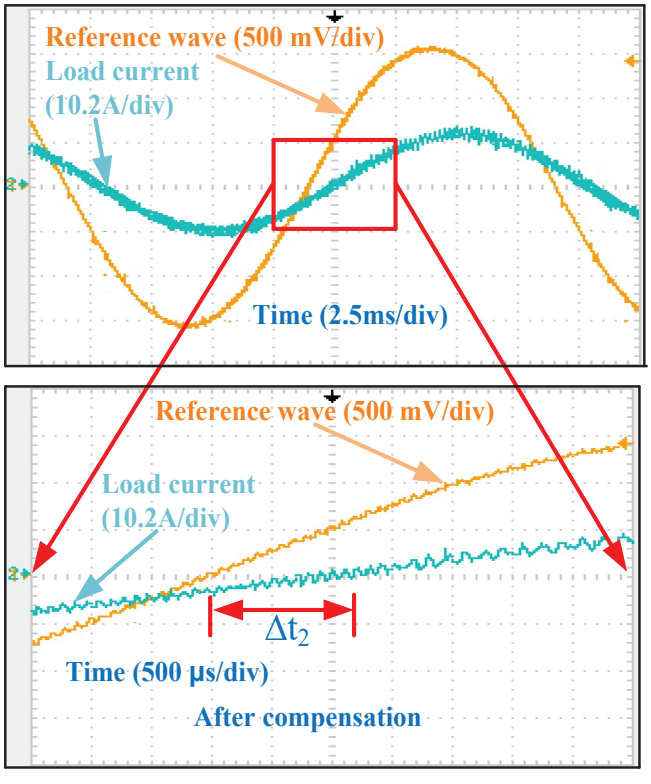

Fig. 15. Load current (blue) (10.2 A/div) and reference waveform (yellow) (500 mV/div) for load series impedance angle 32° after compensation for R-L load.

7. Conclusion

This paper presents the concept of shift in current-zero crossing due to dead-time distortion compensation in PWM VSI. This phenomenon is analysed in detail along with its dependence on different operating parameters. The results obtained from simulation and experimentation in the laboratory are compared with theoretically obtained values, and the comparison results clearly demonstrate the validity of the proposed concept. This paper also recommends a method by which the concept can be utilised for achieving proper compensation, especially in case of current-sensor-less compensation techniques.

References

Bedetti, N., Calligaro, S. and Petrella, R. (2015). Self-Commissioning of Inverter Dead-Time Compensation by Multiple Linear Regression Based on a Physical Model. *IEEE Transactions on Industry Applications*, 51(5), pp. 3954–3964.

Ben-Brahim, L. (1998). The analysis and compensation of dead-time effects in three phase PWM inverters. In: *Proceedings of the 24th Annual Conference of the IEEE Industrial Electronics Society IECON '98*, Aachen, Germany, 31 August, 1998. Vol. 32, pp. 792–797.

Beniak, R. and Rogowski, K. (2016). A Method of Reducing Switching Losses in Three-Level NPC Inverter. *Power Electronics and Drives*, 1(36), No. 2, pp. 55–63.

Berg, M. and Roinila, T. (2020). Nonlinear Effect of Dead Time in Small-Signal Modeling of Power-Electronic System Under Low-Load Conditions. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(4), pp. 3204–3213.

Bhowmick, S., Mukherjee, D., Maiti, S. and Chakraborty, C. (2021). Grid-Tied Neutral Point Clamped based Centralised Photovoltaic Inverter with Improved DC Link Voltage Balancing and Harmonic Minimisation Control. *Power Electronics and Drives*, 6(41), pp. 185–203.

Chierchie, F., Stefanazzi, L., Paolini, E. E. and Oliva, A. R. (2014). Frequency Analysis of PWM Inverters with Dead-Time for Arbitrary Modulating Signals. *IEEE Transactions on Power Electronics*, 29(6), pp. 2850–2860.

Choi, C., Cho, K. and Seok, J. (2007). Inverter Nonlinearity Compensation in the Presence of Current Measurement Errors and Switching Device Parameter Uncertainties. *IEEE Transactions on Power Electronics*, 22(2), pp. 576–583.

Herran, M. A., Fischer, J. R., Gonzalez, S. A., Marcos, G., Judewicz, M. G., Daniel, O. and Carrica, D. O. (2013). Adaptive Dead-Time Compensation for Grid-Connected PWM Inverters of Single-Stage PV Systems. *IEEE Transactions on Power Electronics*, 28(6), pp. 2816–2825.

Hwang, S. and Kim, J. (2010). Dead Time Compensation Method for Voltage-Fed PWM Inverter. *IEEE Transactions on Energy Conversion*, 25(1), pp. 1–10.

Jena, K., Gupta, K. K., Bhatnagar, P., Jain, S. K., Stala, R., Waradzyn, Z., Piróg, S., Penczek, A., Mondzik, A. and Skała, A. (2022). Single-Source Three-Phase Switched-Capacitor-based MLI. *Power Electronics and Drives*, 7(42), pp. 197–209.

Kim, H., Kim, K. and Youn, M. (2003). On-Line Dead-Time Compensation Method Based on Time Delay Control. *IEEE Transactions on Control Systems Technology*, 11(2), pp. 279–285.

Kim, S. and Park, S. (2007). Compensation of Dead-Time Effects Based on Adaptive Harmonic Filtering in the Vector-Controlled AC Motor Drives. *IEEE Transactions on Industrial Electronics*, 54(3), pp. 1768–1777.

Kumar, M. (2018). Time-Domain Characterization of Digitized PWM Inverter with Dead-Time Effect. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 65(10), pp. 3592–3601.

Leggate, D. and Kerkman, R. J. (1997). Pulse-Based Dead-Time Compensator for PWM Voltage Inverters. *IEEE Transactions on Industrial Electronics*, 44(2), pp. 191–197.

Lin, J. (2002). A New Approach of Dead-Time Compensation for PWM Voltage Inverters. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 49(4), pp. 476–483.

Liu, G., Wang, D., Jin, Y., Wang, M. and Peng Zhang, P. (2017). Current-Detection-Independent Dead-Time Compensation Method Based on Terminal Voltage A/D Conversion for PWM VSI. *IEEE Transactions on Industrial Electronics*, 64(10), pp. 7689–7699.

Munoz, A. R. and Lipo, T. A. (1999). On-Line Dead-Time Compensation Technique for Open-Loop

PWM-VSI Drives. *IEEE Transactions on Power Electronics*, 14(4), pp. 683–689.

Rąbkowski, J. and Kopacz, R. (2018). Extended T-type Inverter. *Power Electronics and Drives*, 3(38), No. 1, pp. 55–64.

Roomi, M. M. (2019). An Overview of Carrier-based Modulation Methods for Z-Source Inverter. *Power Electronics and Drives*, 4(39), pp. 15–31.

Seyyedzadeh, S. M., Mohamadian, S., Siami, M. and Shoulaie, A. (2019). Modeling of the Nonlinear Characteristics of Voltage Source Inverters for Motor Self-Commissioning. *IEEE Transactions on Power Electronics*, 34(12), pp. 12154–12164.

Seyyedzadeh, S. M. and Shoulaie, A. (2019). Accurate Modeling of the Nonlinear Characteristic of a Voltage Source Inverter for Better Performance in Near Zero Currents. *IEEE Transactions on Industrial Electronics*, 66(1), pp. 71–78.

Shen, Z. and Jiang, D. (2019). Dead-Time Effect Compensation Method Based on Current Ripple Prediction for Voltage-Source Inverters. *IEEE Transactions on Power Electronics*, 34(1), pp. 971–984.

Tang, Z. and Akin, B. (2017). Suppression of Dead-Time Distortion through Revised Repetitive Controller in PMSM Drives. *IEEE Transactions on Energy Conversion*, 32(3), pp. 918–930.

Wu, C. M., Lau, W. H. and Chung, H. S. (1999). Analytical Technique for Calculating the Output Harmonics of an H-Bridge Inverter with Dead Time. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 46(5), pp. 617–627.

Yu, Q., Lemmen, E., Wijnands, C. G. E. and Vermulst, B. (2021). Output Spectrum Modeling of an H-Bridge Inverter with Dead-Time Based on Switching Mode Analysis. *IEEE Transactions on Power Electronics*, 36(10), pp. 11344–11356.

Zhao, H., Wu, Q. M. G. and Kawamura, A. (2004). An Accurate Approach of Nonlinearity Compensation for VSI Inverter Output Voltage. *IEEE Transactions on Power Electronics*, 19(4), pp. 279–285.