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Hardware in the loop simulation of single-phase PWM rectifiers for improved power quality via ASWFA

Abstract. *This paper presents a control approach that utilizes adaptive sliding window Fourier analysis (ASWFA) for single-phase PWM rectifiers. The primary objective is to effectively regulate the output voltage and minimize the ingress of harmonic currents into the utility grid. Through extensive MIL and HIL simulations, the control system demonstrates its efficacy in maintaining voltage regulation, achieving grid synchronization, and managing harmonic currents across various scenarios. The evaluation results affirm the precise control of voltage and regulation of harmonics under different operational conditions. Furthermore, statistical analysis employing box plots provides validation of the control technique's capability to reduce harmonic distortion. The study reveals that only the harmonic groups within the range of 35 ≤ h < 50 exceeded the thresholds prescribed by IEEE Std. 519-2014 for power systems operating at rated voltages between 120 V and 69 kV at the most stringent ISC/IL < 20 requirements. Overall, the proposed control technique presents a viable solution to effectively reduce harmonic distortion.*

Streszczenie. *W artykule przedstawiono podejście do sterowania, które wykorzystuje adaptacyjną analizę Fouriera z przesuwanym oknem (ASWFA) dla jednofazowych prostowników PWM. Głównym celem jest skuteczna regulacja napięcia wyjściowego i zminimalizowanie przedostawania się harmonicznych do sieci elektroenergetycznej. Dzięki obszernym symulacjom MIL i HIL system sterowania demonstruje swoją skuteczność w utrzymywaniu regulacji napięcia, osiąganiu synchronizacji sieci i zarządzaniu prądami harmonicznymi w różnych scenariuszach. Wyniki oceny potwierdzają precyzyjną kontrolę napięcia i regulację harmonicznych w różnych warunkach pracy. Ponadto analiza statystyczna wykorzystująca wykresy pudełkowe zapewnia walidację zdolności techniki sterowania do redukcji zniekształceń harmonicznych. Z przeprowadzonych badań wynika, że tylko grupy harmoniczne z przedziału 35 ≤ h < 50 przekraczały progi określone przez IEEE Std. 519-2014 dla systemów elektroenergetycznych pracujących przy napięciu znamionowym od 120 V do 69 kV przy najbardziej rygorystycznych wymaganiach ISC/IL < 20. Ogólnie rzecz biorąc, proponowana technika sterowania stanowi realne rozwiązanie skutecznej redukcji zniekształceń harmonicznych.* (***Sprzętowa symulacja pętli jednofazowych prostowników PWM w celu poprawy jakości zasilania poprzez ASWFA***)

Keywords: Hardware-in-the-loop simulation, Single-phase PWM rectifiers, ASWFA, Harmonic distortion.
Słowa kluczowe: Symulacja sprzętu w pętli, jednofazowe prostowniki PWM, ASWFA, zniekształcenia harmoniczne.

Introduction

Single-phase PWM rectifiers are widely used in industries that require DC bus voltage control, such as in AC railway electrification systems [1], electric train traction inverters [2], Uninterruptible Power Supplies [3], electric vehicle battery charging systems [4], micro turbine generators, and wind turbine renewable energy systems [5] [6]. These rectifiers convert AC input voltage into a regulated DC output voltage with the help of a switching device that is controlled with a Pulse Width Modulation (PWM) technique. The PWM rectifier operates by modulating the duty cycle of the switching device to control the voltage and the current waveforms. Single-phase PWM rectifiers can be used as active filters to reduce the current distortion, caused by non-linear loads that are connected to utility grids. However, the performance of these systems is subject to the design of the control strategy, which needs to ensure that the output voltage is regulated and stabilized, while the harmonic distortion is limited. Therefore, various control techniques have been proposed in [7-8]. This paper suggests a new way to control single-phase PWM rectifiers by combining a proportional-integral (PI) controller with an adaptive sliding window Fourier analysis (ASWFA) harmonic calculator. The proposed control method has been designed to maintain the output voltage, to control harmonic current distortion, and to maintain grid synchronization, while also complying with IEEE Standard 519-2014.

The use of Hardware-in-the-Loop (HIL) simulations in power electronics is becoming increasingly prevalent due to its effectiveness in validating control strategies before implementing them in real-world scenarios. The ability to test and verify control strategies in a simulated environment before deploying them in hardware helps to minimize the risks associated with implementation, such as system downtime and equipment damage [9-10]. In this context, HIL simulation is particularly valuable in the development of power electronic systems. This paper focuses on the development and evaluation of a control strategy for a single-phase PWM rectifier in order to improve power quality in utility grids. The proposed control strategy was evaluated using both MATLAB/Simulink and hardware-in-the-loop simulations. The results demonstrated that the proposed control strategy had effectively regulated the output voltage, had mitigated the harmonic distortions, and had achieved grid synchronization, making it a promising solution for power quality improvement applications.

Therefore, this study aimed at providing a comprehensive understanding of the proposed control strategy's capabilities in improving the power quality of single-phase PWM rectifiers. The paper is organized in the following manner. Section 2 provides an overview of the PWM rectifier system and the proposed control method. Section 3 describes the controller design and the tuning parameters. Section 4 presents the results of a MATLAB/Simulink simulation of the proposed controller, while Section 5 presents the HIL simulation configuration, and Section 6 presents the HIL simulation results. Finally, the paper concludes with a summary of the findings and suggestions.

The proposed Single-phase PWM rectifier control

The circuit structure of a PWM rectifier is depicted in Figure 1. It is exactly the same as a four-quadrant inverter. The rectifier comprises the full-bridge IGBT transistors, an input impedance (x_s), and a capacitor at the output (C). IGBTs operate via a pulse width modulation (PWM) technique. Assuming only the fundamental frequency, both the source voltage (v_s) and the rectifier input terminal voltage (v_r) are sinusoidal waveforms that are separated by the input impedance. The power flow is dependent on the angle between v_s and v_r, as illustrated in Figure 2. The direction of power flow from the source to the rectifier input terminal can be expressed as Equation (1) [11].

(1) $$P = \frac{V_s V_r}{X_s} \sin\delta = V_s I_s \cos(\theta)$$

in which: V_s – fundamental RMS voltage, V_r – fundamental RMS voltage, δ - phase displacement between V_s and V_r, X_s – input impedance, and $cos(\theta)$ – power factor

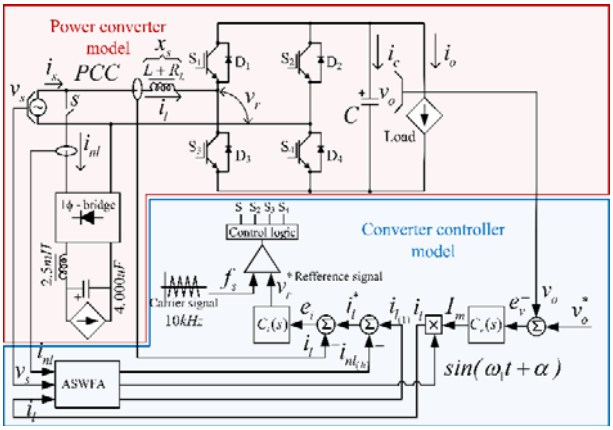

Fig.1. The proposed circuit and control diagram of a single-phase PWM rectifier

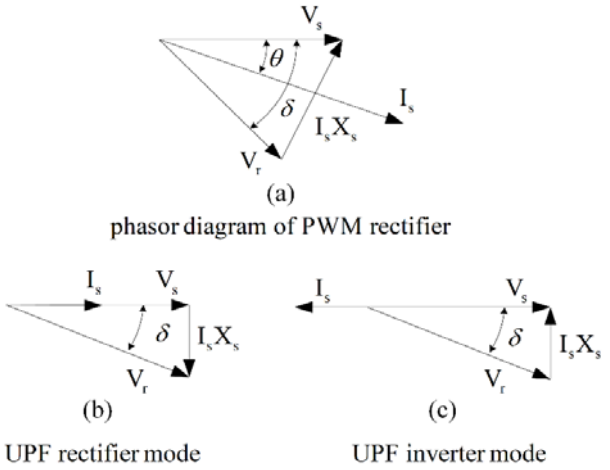

Fig.2. The phasor diagram of a single-phase PWM rectifier

The converter functioned as a rectifier and an inverter with a unity power factor, as depicted in Figure 2 (b) and (c), respectively. The purpose of this converter was to regulate the direction of power at the point of common coupling (PCC) in order to maintain a constant dc output voltage (v_o) and a low total harmonic distortion (THD) of the source current (i_s). However, if a non-linear load is connected to the source voltage, the source current will become distorted, resulting in a low power factor (PF) due to the increase of THD_i at the PCC. As a result, the function of removing the source harmonic current, which as previously mentioned was generated by the non-linear loads, was added in this work.

The Harmonic feed-forward compensation

The Adaptive Sliding Window Fourier Analysis block (ASWFA) was added to the controller model section of Figure 1 to compensate for the harmonic currents using the feed-forward method. The disturbance, caused by the harmonic components of the non-linear load current ($i_{nl(h)}$), can theoretically be wholly eliminated if the value of $i_{nl(h)}$ can be accurately measured and calculated from the non-linear load current (i_{nl}) [12]. The ASWFA block generates only the harmonic components of the non-linear load current and eliminates them via negative feed-forward into the summing point of the inductor reference current (i_l*). As illustrated in Figure 3, the source current (i_s) will consist entirely of the fundamental components of the non-linear load current ($i_{nl(1)}$) and the inductor current ($i_{l(1)}$). However, in practice, the effectiveness of eliminating this harmonic current is dependent on the accuracy of the harmonic extractor ASWFA and the performance of the current controller ($C_i(s)$), as illustrated in the controller section of Figure 1.

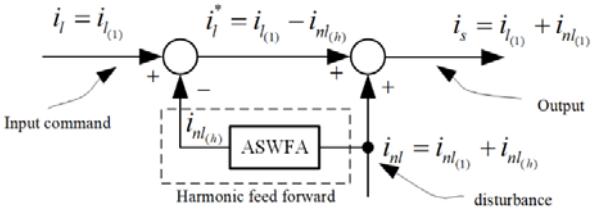

Fig.3. The Harmonic current feed-forward compensation

The Adaptive sliding window Fourier analysis

The rectifier must operate in synchronization with the utility grid frequency at all times. As a result, this work enhanced the sliding window Fourier analysis (SWFA) method [13-14] by adapting the sliding window width algorithm to the utility grid frequency. The zero-crossing detector technique (ZCD) is used in this work to determine the window width (N) that could be used to adjust the sliding window. It is a straightforward method that is readily applicable to the SWFA algorithm. According to [15], Equation (2) can calculate the synchronized fundamental frequency, while Equation (3) can express the window width.

(2) $$f_1 = \frac{1}{T_1} = \frac{m}{t_{cz,m} - t_{cz,1}}$$

(3) $$N \cong \frac{t_{cz,m} - t_{cz,1}}{T_s}$$

in which: f_1 denotes the fundamental frequency, and T_1 denotes the fundamental component's period. T_s – sampling period; $t_{cz,1}$ and $t_{cz,m}$ – timestamps for the signal's first and last transitions through zero; m – the number of complete periods contained within the total duration of the measurement; N – the number of samples corresponding to the time interval between the signal's first and last transitions, which was the window width of the ASWFA method.

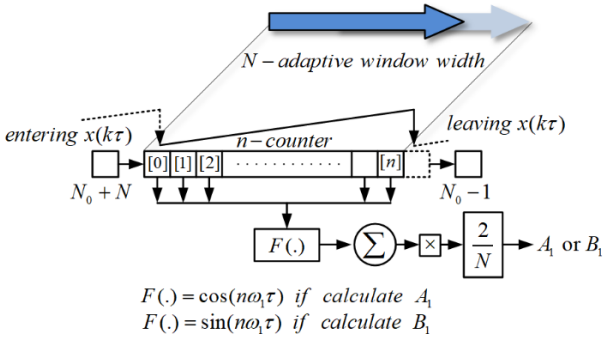

Fig.4. The calculation process for Fourier coefficients A_1 and B_1

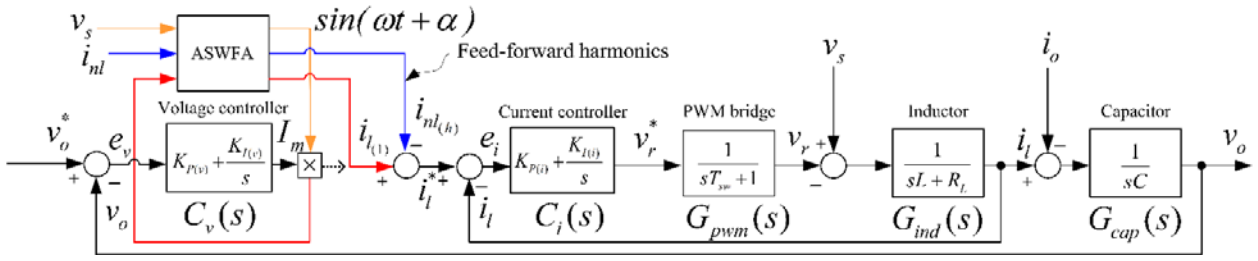

Fig.5. The block diagram of the simplified control system

The adaptive sliding window Fourier analysis (ASWFA) block in the controller section of Figure 1 was designed to generate harmonic components of the non-linear load current, the fundamental component of the inductor current, and the phase angle (α) of the synchronization signal ($sin(\omega_1 t+\alpha)$) for use in the current control loop. The proposed method enabled the calculation of these three signals using the non-linear load current, inductor current, and source voltage, respectively. However, the method only calculated the fundamental component of the three signals using equations (4) and (5), which are composed of the fundamental coefficients of the source voltage ($A_{1(vs)}$ and $B_{1(vs)}$), the non-linear load current ($A_{1(inl)}$ and $B_{1(inl)}$), and the inductor current ($A_{1(il)}$ and $B_{1(il)}$). A sampling period (τ) is defined as the time of an entire fundamental period (T_1) divided by N, in which k = 0, 1, 2, ...(n-1) and n is the number of discrete samples within T_1.

$$(4)\qquad A_1 = \begin{bmatrix} A_{1(v_s)} = \frac{2}{N}\sum_{n=N_0}^{N_0+N-1} v_s(n\tau)\cos(n\omega_1\tau) \\ A_{1(i_{nl})} = \frac{2}{N}\sum_{n=N_0}^{N_0+N-1} i_{nl}(n\tau)\cos(n\omega_1\tau) \\ A_{1(i_l)} = \frac{2}{N}\sum_{n=N_0}^{N_0+N-1} i_l(n\tau)\cos(n\omega_1\tau) \end{bmatrix}$$

$$(5)\qquad B_1 = \begin{bmatrix} B_{1(v_s)} = \frac{2}{N}\sum_{n=N_0}^{N_0+N-1} v_s(n\tau)\sin(n\omega_1\tau) \\ B_{1(i_{nl})} = \frac{2}{N}\sum_{n=N_0}^{N_0+N-1} i_{nl}(n\tau)\sin(n\omega_1\tau) \\ B_{1(i_l)} = \frac{2}{N}\sum_{n=N_0}^{N_0+N-1} i_l(n\tau)\sin(n\omega_1\tau) \end{bmatrix}$$

The process of a data block sliding through an adaptive window is depicted in Figure 4, and equations (6) and (7) can be used to update the coefficients $A_1^{(new)}$ and $B_1^{(new)}$ at each sampling interval.

By using equations (8) and (9), it is possible to determine the instantaneous waveform of the fundamental component of the non-linear load current and the inductor current. The harmonic component of the non-linear load current for feed-forward in the current control loop was calculated using equation (10). For source synchronization, the phase angle (α) of the sine template ($sin(\omega_1 t+\alpha)$) was calculated from equation (11), in which the fundamental angular frequency (ω_1) was obtained from $f_1=1/N$, in which N was the total number of n-samples within the window.

Overall, it was determined that the ASWFA method had facilitated the synchronization of the PWM rectifier with the utility source, while keeping the power factor at the point of common coupling (PCC) close to unity at all times. Furthermore, the same block can compensate for harmonic currents at the PCC, eliminating the need for separate synchronization control.

$$(6)\quad A_1^{(new)} = \begin{bmatrix} A_{1(v_s)}^{(new)} = A_{1(v_s)}^{(old)} + \frac{2}{N}\{v_s[(N_0+N)\tau]... \\ \cos[(N_0+N)\omega_1\tau] - v_s[(N_0-1)\tau]... \\ \cos[(N_0-1)\omega_1\tau]\} \\ A_{1(i_{nl})}^{(new)} = A_{1(i_{nl})}^{(old)} + \frac{2}{N}\{i_{nl}[(N_0+N)\tau]... \\ \cos[(N_0+N)\omega_1\tau] - i_{nl}[(N_0-1)\tau]... \\ \cos[(N_0-1)\omega_1\tau]\} \\ A_{1(i_l)}^{(new)} = A_{1(i_l)}^{(old)} + \frac{2}{N}\{i_l[(N_0+N)\tau]... \\ \cos[(N_0+N)\omega_1\tau] - i_l[(N_0-1)\tau]... \\ \cos[(N_0-1)\omega_1\tau]\} \end{bmatrix}$$

$$(7)\quad B_1^{(new)} = \begin{bmatrix} B_{1(v_s)}^{(new)} = B_{1(v_s)}^{(old)} + \frac{2}{N}\{v_s[(N_0+N)\tau]... \\ \sin[(N_0+N)\omega_1\tau] - v_s[(N_0-1)\tau]... \\ \sin[(N_0-1)\omega_1\tau]\} \\ B_{1(i_{nl})}^{(new)} = B_{1(i_{nl})}^{(old)} + \frac{2}{N}\{i_{nl}[(N_0+N)\tau]... \\ \sin[(N_0+N)\omega_1\tau] - i_{nl}[(N_0-1)\tau]... \\ \sin[(N_0-1)\omega_1\tau]\} \\ B_{1(i_l)}^{(new)} = B_{1(i_l)}^{(old)} + \frac{2}{N}\{i_l[(N_0+N)\tau]... \\ \sin[(N_0+N)\omega_1\tau] - i_l[(N_0-1)\tau]... \\ \sin[(N_0-1)\omega_1\tau]\} \end{bmatrix}$$

$$(8)\qquad i_{nl(1)}(k\tau) = A_{1(i_{nl})}\cos(\omega_1 k\tau) + B_{1(i_{nl})}\sin(\omega_1 k\tau)$$

$$(9)\qquad i_{l(1)}(k\tau) = A_{1(i_l)}\cos(\omega_1 k\tau) + B_{1(i_l)}\sin(\omega_1 k\tau)$$

$$(10)\qquad i_{nl(h)}(k\tau) = i_{nl}(k\tau) - i_{nl(1)}(k\tau)$$

$$(11)\qquad \alpha(k\tau) = \tan^{-1}\left(\frac{A_{1v_s}}{B_{1v_s}}\right)$$

The Proposed controller design

The current controller

The current control system diagram, as described in [16] and shown in Figure 5, comprises two control loops: the current control loop (inner) and the voltage control loop

(outer). The current error (e_i) was determined by the difference between the inductor reference current (i_l^*) and the measured current (i_l), which was then sent to the current controller ($C_i(s)$) to generate the rectifier input terminal voltage (v_r) using the PWM rectifier bridge transfer function ($G_{pwm}(s)$). The difference between the source voltage (v_s) and the rectifier input terminal voltage (v_r) was then fed to the inductor transfer function ($G_{ind}(s)$) to create an inductor current (i_l) that would be close to the inductor reference current as designed. The transfer function of the current control loop was calculated using equation (12), in which the external interference term was considered to be the source voltage (v_s).

$$\frac{I_l(s)}{I_l^*(s)} = \frac{C_i G_{pwm} G_{ind}(s)}{1 + C_i G_{pwm} G_{ind}(s)} \tag{12}$$

The voltage controller

In the voltage control loop section, the error value (e_v), resulting from the difference between the output reference capacitor voltage (v_o^*) and the measured output voltage (v_o), was sent to the voltage controller ($C_v(s)$) to produce an inductor reference current magnitude (I_m). The inductor reference current was then constructed by passing the $I_m \times sin(\omega_1 t + \alpha)$ signal through the ASWFA block to filter out the harmonics produced by the capacitor ripple voltage [17]. The inductor reference current (i_l^*) consisted entirely of the fundamental component and was fed into the current control loop, where the difference between the inductor current and the DC load current (i_o) yielded the output voltage via the capacitor transfer function ($G_{cap}(s)$), which was close to the intended output reference voltage.

$$\frac{V_o(s)}{V_o^*(s)} = \frac{C_v G_i G_{cap}(s)}{1 + C_v G_i G_{cap}(s)} \tag{13}$$

Table 1: The parameter of circuits and controller

Parameters		Values
Circuits		
v_s		220 V_{rms} / 50*Hz*
v_o^*		500 V
L		7.5 *mH*
R		0.01 Ω
C		10,000 *uF*
T_{sw}		0.1*ms*
Controllers		
$C_v(s)$	$K_{P(v)}$	0.48
	$K_{I(v)}$	10.00
$C_i(s)$	$K_{P(i)}$	-101.78
	$K_{I(i)}$	-1.00

The PI controllers' tuning parameters for the current and voltage control loops were developed using the bandwidth approach. According to the controller design in [18], the inner current loop must be faster than the outer voltage loop to quickly follow the design input current i_l^*. Hence, the bandwidth of the inner loop must be greater than the outer loop for at least one decade because the output current i_l is expected to have fast dynamics and to be stable. The PI controller of the current control loop was designed to have a close loop bandwidth of approximately 2.5 kHz with an open-loop phase margin of 45.8˚ at a select crossover frequency of about 1.55 kHz, which is sufficient to compensate for the first fifty harmonic currents based on a 50 Hz system. The outer loop was designed to have a bandwidth of approximately 10 Hz because the input signal was DC voltage. In the same way, the open-loop system has a phase margin of approximately 68.1˚ at a select crossover frequency of about 8.29 Hz. The voltage and current control loop responses, derived by substituting the parameters from Table 1 into Equations (12) and (13), are depicted in Figure 6.

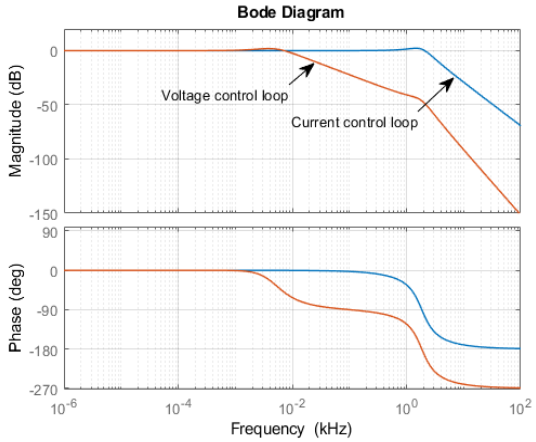

Fig.6. The Bode diagram of proposed control system

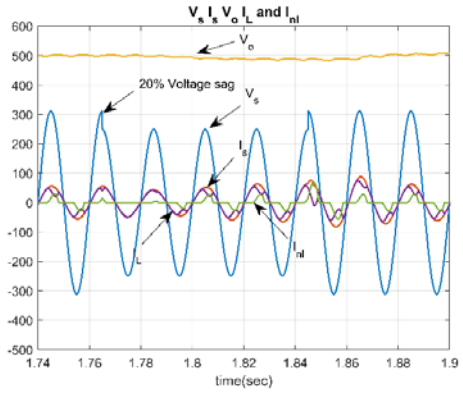

Fig.7. The simulated response to the source voltage sag

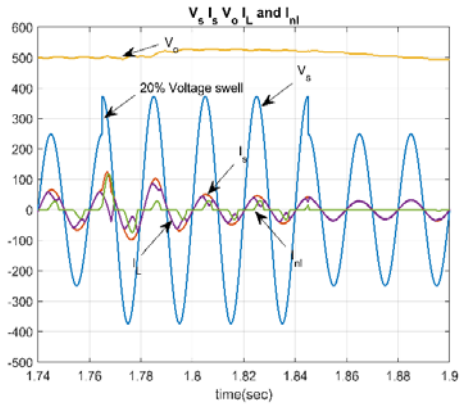

Fig.8. The simulated response to the source voltage swell

Model-in-the-loop (MIL) simulation of the proposed controller

To ensure the effectiveness of the proposed controller prior to its implementation in a hardware-in-the-loop (HIL) scenario, a single-phase PWM rectifier model was constructed and simulated using MATLAB/Simulink (MIL simulation), as illustrated in Figure 1. The MIL simulation consisted of a non-linear load rated at 13 Arms (2,860VA),

simulated using a single-phase rectifier that had been connected to an LC filter and a current-controlled source. Additionally, a DC load, rated at 12Arms (6,000VA), was modeled with the controlled source, and the current at the point of common coupling (PCC) was 39.2 Arms at both rated loads, which served as the maximum demand load current (I_L) for calculating the IEEE standard of total demand distortion (TDD).

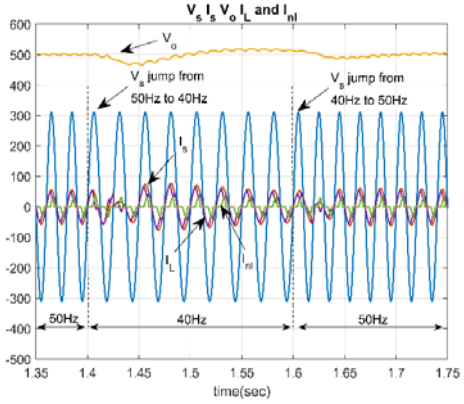

Fig.9. The simulated response to the source frequency jumps

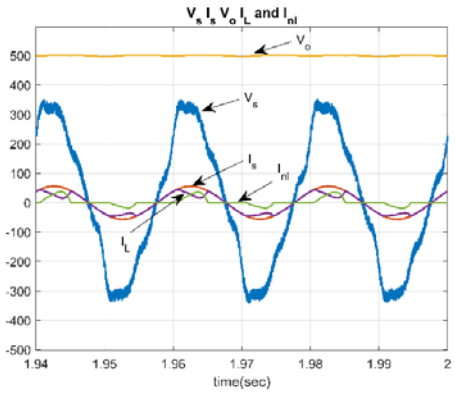

Fig.10 The simulated response to the source voltage distortion

Based on the MIL simulation results, the proposed control method maintained the output voltage and low distortion of the input current in accordance with the IEEE Std 519-2014 $I_{SC}/I_L<20^c$ [19]. The simulation results were also evaluated under various fault conditions, consisting of voltage sag, voltage swell, frequency jumps, and source distortion at the loads ratings, as depicted in Figures 7 to 10, respectively. The results indicated that the proposed control method had effectively maintained the output voltage, had synchronized with the source, and had controlled the harmonic current, even during the event of a source malfunction. Figure 11 presents the simulation results of THD_i and TDD before and after filtering out the harmonics, which were caused by the capacitor ripple voltage when the DC load had varied from -120 to 120 percent of the rated value without the non-linear load. The results showed that the THD_i and TDD values had been lower after filtering, while the TDD and the individual harmonic orders had remained within the limits specified by IEEE Std 519-2014. These results suggested that the proposed control had been effective at maintaining the output voltage, regulating the harmonic current, and at meeting the standards under a variety of fault conditions.

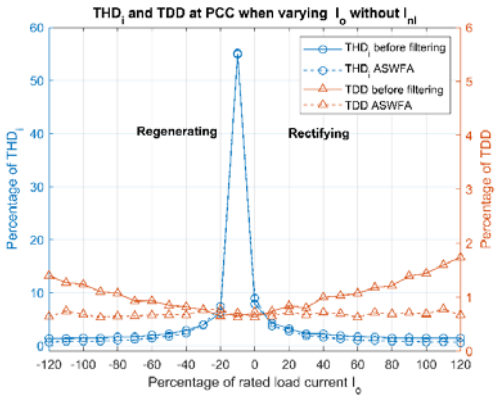

Fig.11 The harmonics reduction via ASWFA in the voltage control loop

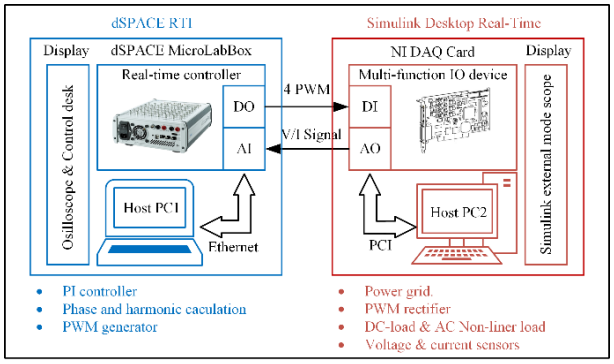

Fig.12 The HIL simulation configuration diagram

Fig.13 The installation of the HIL testing equipment

The HIL configuration

This work employed the hardware-in-the-loop simulation method, which partitions the system into two primary components: the controller and the plant, as illustrated in Figure 1. The controller component (blue box) was comprised of a Proportional-Integral controller, a phase angle calculator, an adaptive sliding window Fourier analysis (ASWFA) harmonic calculator, and a pulse width modulation (PWM) signal generator. Whereas, the plant component (red box) was composed of a utility source, a PWM rectifier, a DC load, an AC non-linear load, a voltage sensor, and a current sensor.

To perform the HIL simulation, the controller was developed using dSPACE DS1202, while the plant was simulated using a real-time simulator that had been created from Simulink Desktop Real-time and an NI Data Acquisition card, as depicted in Figure 12. The communication between the hardware of both components

was enabled by digital and analog input/output ports, which were controlled by Host PC1 and Host PC2, respectively. The installation of the HIL testing equipment is presented in Figure 13.

The HIL simulation results

As shown in Figure 14, the real-time simulation results by HIL for the rated DC and non-linear loads demonstrated that the controller had been able to stabilize the DC voltage output at 500V within 20 cycles. The steady-state source currents at the rated DC loads of 12A and -12A are presented in Figures 15 and 16, respectively. The current waveform appeared sinusoidal with a phase angle matching the source voltage, while the DC output voltage remained constant at 500V. In addition, Figure 17 displays the system's performance at a 12A DC rated load. The ASWFA algorithm accurately calculated the frequency of the fundamental component and grid synchronization when the supply frequency was varied from 50Hz to 40Hz, while the output DC voltage at 500V was also stabilized.

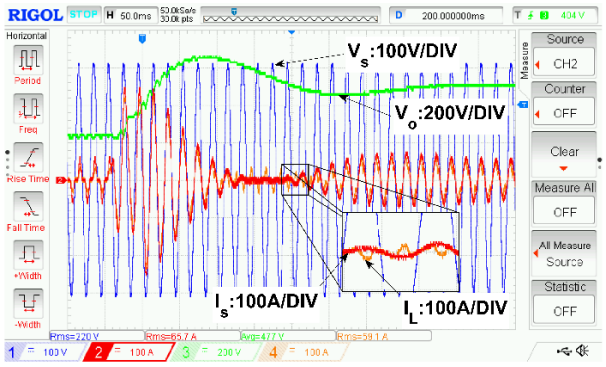

Fig.14 The transient response at the rated DC and non-linear loads

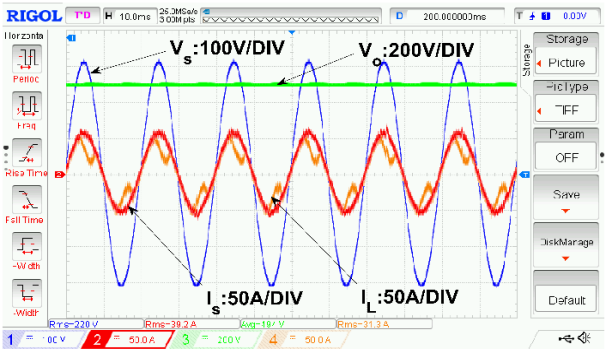

Fig.15 The steady-state source currents at the rated DC loads of 12A

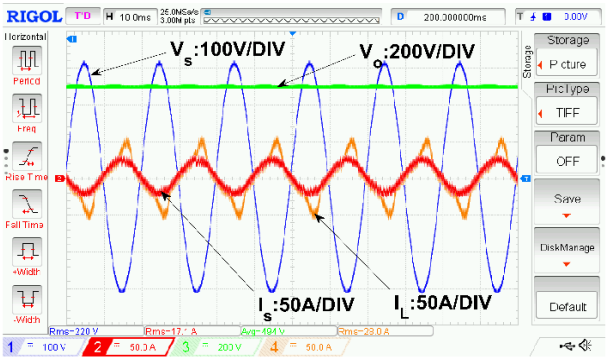

Fig.16 The steady-state source currents at the DC loads of -12A

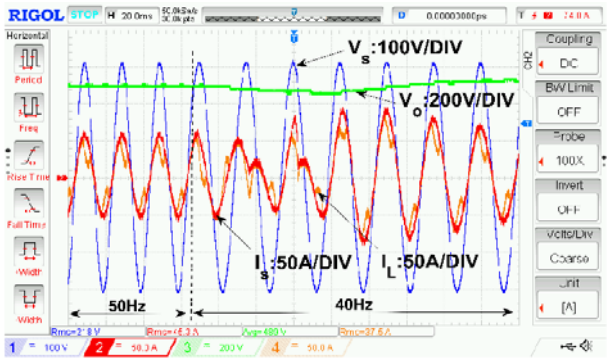

Fig.17 The responses during the frequency changes from 50Hz to 40Hz

Comparing the MIL and HIL simulation results

A comparison between the MIL and HIL simulations was performed to evaluate the performance of the system under load variations that ranged from 0 to 200 percent. Figure 18 compares the MIL and HIL for THD_i and TDD as the DC load current is varied, while the non-linear load current is held constant at zero. Figure 19 compares the MIL and HIL for total PF under the same conditions. Figures 20 and 21 depict the comparison results when variations in the non-linear load current occurred while the DC load current was equal to the rated load. All experiments were performed with both rectifying and regenerating modes.

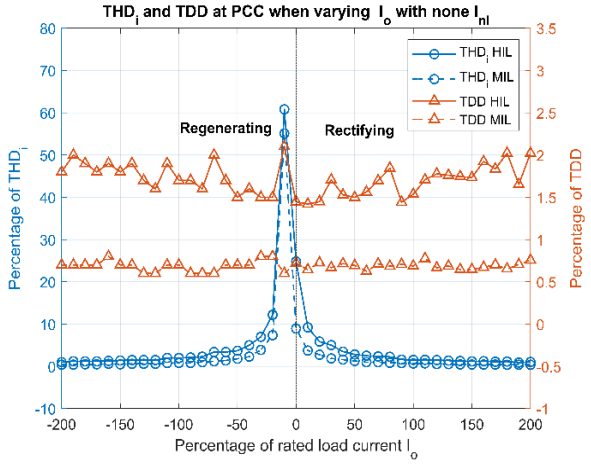

Fig.18 A Comparison of the THDi and TDD between MIL and HIL when varying DC loads without a non-linear load

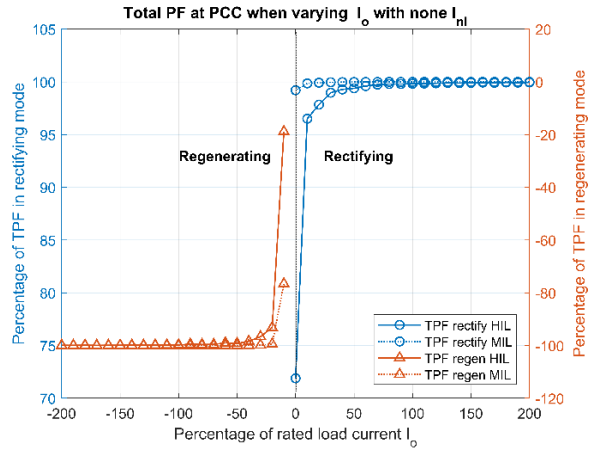

Fig.19 A Comparison of TPF between MIL and HIL when varying DC loads without a non-linear load

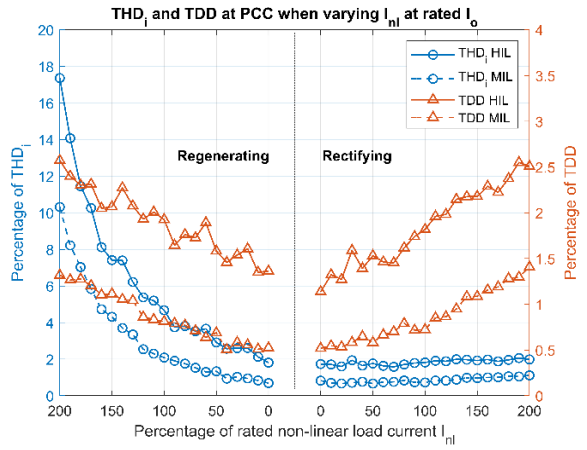

Fig.20 A Comparison of the THDi and TDD between MIL and HIL when varying the non-linear load at the rated DC load

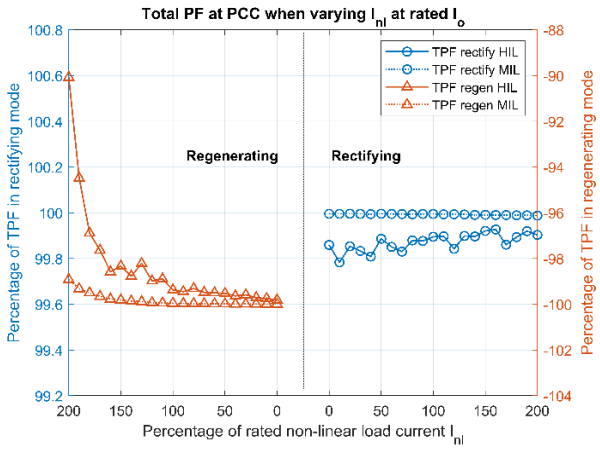

Fig.21 A Comparison of the TPF between MIL and HIL when varying the non-linear load at the rated DC load

According to the results of the DC load current variation test in Figures 18 and 19, the mean absolute difference (MAD) between the MIL and HIL simulations of THD_i had been 1.925%. The MAD of TDD was found to be 1.035%, while the MAD of TPF was found to be 2.71%. Similarly, the non-linear load current variation results, depicted in Figures 20 and 21, demonstrated that the MAD of THD_i had been 1.925%, the MAD of TDD had been 1.01%, and the MAD of TPF had been 0.785%.

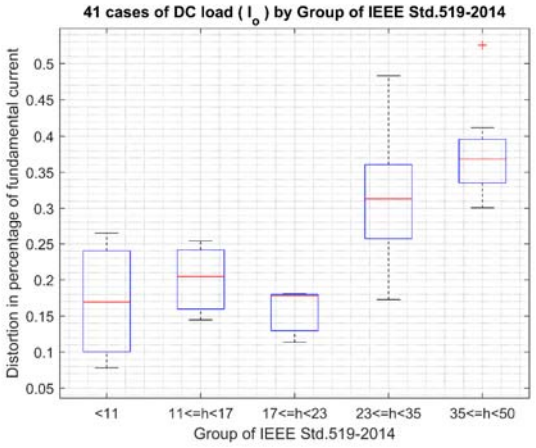

Fig.22 The individual harmonic current statistical distribution when varying the DC loads without a non-linear load

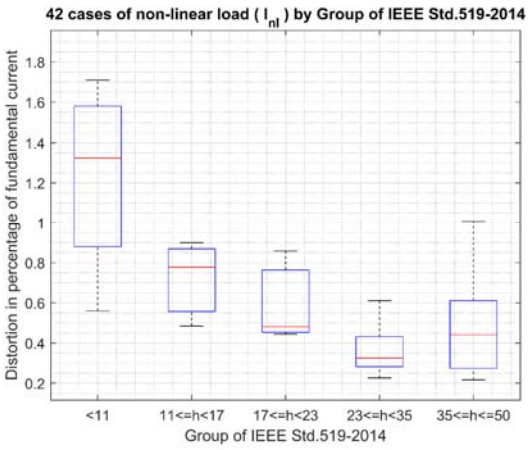

Fig.23 The individual harmonic current statistical distribution when varying the non-linear load at the rated DC load

The individual harmonic current statistical distribution data from the HIL test was compared to the IEEE Std. 519-2014 [17] recommended current distortion limits for systems nominally rated 120 V through 69 kV using the most stringent criteria I_{SC}/I_L<20 via box plot analysis, as illustrated in Figure 22 and Figure 23. The results of the DC load current variations in Figure 22 and the non-linear load current variations in Figure 23 indicated that only the harmonic groups 35 <= h < 50 had exceeded the aforementioned requirement. When considering the criteria of I_{SC}/I_L > 20, it was found that all the individual harmonic groups had been compliant with the IEEE Standard. Additionally, the total demand distortion (TDD) of all the test cases had been less than 5 percent, which met the IEEE Std. 519-2014.

Conclusions

The present study introduced a control approach for single-phase PWM rectifiers using an algorithm called an adaptive sliding window Fourier analysis (ASWFA). The primary objective of this method was to regulate the direct current output voltage and to limit the ingress of the harmonic current into the utility grid. The effectiveness of the control system in regulating the output voltage, achieving synchronization with the utility grid, and in managing the harmonic current across various operational scenarios, including load fluctuations and grid voltage faults, was demonstrated through MIL and HIL simulations.

The evaluation of the MIL and HIL simulation results showed that the proposed control approach had been highly precise in managing the output voltage and in regulating the harmonic current across diverse operational scenarios. The effectiveness of the proposed control technique in constraining harmonic distortion was demonstrated by using hardware-in-the-loop (HIL) simulation outcomes. This statement was further confirmed through statistical analysis, which employed box plots.

The study revealed that only the harmonic groups within the range of 35 <= h < 50 had exceeded the thresholds set by IEEE Std. 519-2014 for power systems operating at rated voltages between 120 V and 69 kV, while adhering to the most stringent requirements I_{SC}/I_L < 20. The findings of the study indicated that the proposed control technique is a viable solution that can be used to reduce harmonic distortion via single-phase PWM rectifiers.

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REFERENCES

[1] W. Song, S. Wang, C. Xiong, X. Ge, and X. Feng, "Single-phase three-level space vector pulse width modulation algorithm for grid-side railway traction converter and its relationship of carrier-based pulse width modulation," *IET Electrical Systems in Transportation*, vol. 4, No. 3, pp. 78–87, Sep. 2014.

[2] V. Blahnik and J. Talla, "Single-phase synchronization for traction active rectifier," *International Conference on Applied Electronics (AE)*, Sep. 2016, pp. 23–26.

[3] H. Komurcugil, N. Altin, S. Ozdemir, and I. Sefa, "An Extended Lyapunov-Function-Based Control Strategy for Single-Phase UPS Inverters," *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3976–3983, Jul. 2015.

[4] L. Pan and C. Zhang, "Model Predictive Control of a Single-Phase PWM Rectifier for Electric Vehicle Charger," *Energy Procedia*, vol. 105, pp. 4027–4033, May 2017.

[5] D. A. Khaburi and A. Nazempour, "Design and simulation of a PWM rectifier connected to a PM generator of micro turbine unit," *Scientia Iranica*, vol. 19, no. 3, pp. 820–828, Jun. 2012.

[6] A. Mirecki, X. Roboam, and F. Richardeau, "Architecture Complexity and Energy Efficiency of Small Wind Turbines," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 1, pp. 660–670, Feb. 2007.

[7] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 5, pp. 962–981, Oct. 2003.

[8] M. Mansouri, S. Hr. Aghay Kaboli, J. Selvaraj, and N. Abd. Rahim, "A review of single phase power factor correction A.C.-D.C. converters," *IEEE Conference on Clean Energy and Technology (CEAT)*, Nov. 2013, pp. 389–394.

[9] A. Belkhiri, "Hardware in the Loop Co-Simulation of an FPGA Based Sine Pulse Width Modulator for Variable Speed AC Drives," *Przegląd Elektrotechniczny*, vol. 1, no. 12, pp. 49–54, Dec. 2020.

[10] A. Rosa, "Integrated PBL and HIL practices for real-time simulations applied in technical and engineering teaching using embedded systems," *Przegląd Elektrotechniczny*, vol. 1, no. 1, pp. 48–54, Jan. 2021.

[11] J. Bauer, "Single-Phase Pulse Width Modulated Rectifier," *Acta Polytechnica,* vol. 48, no. 3, Jan. 2008, doi: 10.14311/1025.

[12] C. L. Phillips and J. Parr, Feedback Control Systems, 5 edition. Boston: Pearson, 2010.

[13] M. El-Habrouk and M. K. Darwish, "Design and implementation of a modified Fourier analysis harmonic current computation technique for power active filters using DSPs," *IEE Proceedings - Electric Power Applications*, vol. 148, no. 1, pp. 21–28, Jan. 2001.

[14] K. Areerak, S. Visawa-Phatra-Dhanadhorn, and S. Sujitjorn, "Hybrid compensation for harmonic and power factor in single-phase AC drive," *International Conference on Circuits, Systems and Signals - Proceedings*, pp. 68–73, Jan. 2010.

[15] K. A. Ivanenko and A. N. Serov, "Zero-Crossing Technique Modification for the Frequency Measurements of Real Power Grids," *IEEE International Conference on Electrical Engineering and Photonics (EExPolytech)*, Oct. 2020, pp. 106–109.

[16] E. dos Santos and E. R. da Silva, Advanced Power Electronics Converters: PWM Converters Processing AC Voltages, 1 edition. Hoboken, New Jersey: Wiley-IEEE Press, 2014.

[17] S. Somkun, P. Sehakul, and V. Chunkag, "Novel control technique of single-phase PWM rectifier by compensating output ripple voltage," in 2005 *IEEE International Conference on Industrial Technology*, Dec. 2005, pp. 969–974.

[18] R. C. Dorf and R. H. Bishop, Modern Control Systems, 13 edition. Hoboken: Pearson, 2016.

[19] "IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," IEEE Std 519-2014 (Revision of IEEE Std 519-1992), pp. 1–29, Jun. 2014.