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Grid-Tied Neutral Point Clamped based Centralised Photovoltaic Inverter with Improved DC Link Voltage Balancing and Harmonic Minimisation Control

Research article

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Abstract: This paper proposes an improved space vector pulse width modulation (SVPWM) based DC link voltage balancing control of a three-phase three-level neutral point clamped (NPC) centralised inverter supplying the generated power from photo voltaic (PV) array to a three-phase utility grid. Two possible schemes have been developed based on the power conversion stage between PV array and the utility grid namely, two-stage (three-level boost converter three-phase three-level NPC inverter) and single-stage (three-phase three-level NPC inverter alone). The comparison between these two schemes has been thoroughly discussed in terms of the control strategies employed, power loss analysis and efficiency. The performance of the centralised inverter under different modes of operation has been investigated by developing the required control strategies for smooth operation. Using the proposed control strategy, the centralised inverter can be operated as a static synchronous compensator (STATCOM) during night time, if needed. The power loss incurred in the power-electronic converters has been analysed for constant and also for variable ambient temperature. The effectiveness of the centralised inverter as an active filter (AF) has also been verified when a three-phase non-linear load is considered in the system.

Keywords: *photovoltaic multilevel inverters • neutral point voltage balancing • space vector pulse width modulation • current harmonic minimisation*

1. Introduction

The enormous growth in the renewable generation due to shortage of the fossil fuels has resulted in significant research studies over the last few years. Among these, photo voltaic (PV) being the most common due to its noiseless operation, simple installation process and possibility of installing nearer to the consumer, has signified the applications of the grid-tied PV inverters as an important part to these systems (Cavalcanti et al., 2012; Zhang et al., 2016). For three-phase grid-connected systems, large-scale PV installations with capacity from 10 kWp (rooftop installations) can be achieved as more constant output power require smaller capacitors and hence lower cost, higher reliability and lifetime as compared to the single-phase systems (Janardhan et al., 2020; Kerekes et al., 2009). Most of the PV inverter topologies have the line-frequency transformer connected at the grid side, which provides galvanic isolation thereby limiting the leakage current flow through the parasitic capacitance of the PV array arising due to fluctuations in potential between the PV array and ground. However, the presence of the transformer increases the system size, weight and loss, and reduces the system efficiency (Cavalcanti et al., 2010).

For lower cost and improved efficiency of the PV grid-tied inverter systems, several research studies have been made for comparing performance between the three-level and two-level PV inverters. For higher switching frequency, the three-level PV inverters are seen to have lower total semi-conductor power loss as compared to the two-level ones, although the number of power semiconductor devices is more in the three-level inverters

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(Raseena and George, 2020; Schweizer et al., 2013; Teichmann and Bernet, 2005). But, the possibility of non-uniform power loss distribution of the devices increases as the number of level increases for the PV inverters (Bruckner and Bernet, 2007).

Another important aspect for the grid-tied inverters is to function as active filter (AF) for improving the power quality of the system. These inverters can be controlled to operate for the reactive power and harmonic compensation of the grid, even under unbalancing conditions (Singh et al., 1999). For accomplishing these functionalities of the grid-tied inverters, a *p*–*q* theory was developed in (Akagi et al., 1984). Although this theory was initially proposed for three-phase three-wire systems, later this was extended to three-phase four-wire systems in (Aredes and Watanabe, 1995; Watanabe et al., 1993).

Among the various topologies used for grid-tied PV inverters, three-level neutral point clamped (NPC) topology is commonly popular due to reduced harmonic distortion, improved conversion efficiency and reduced voltage stress across the power semiconductor devices (Nabae et al., 1981; Rodriguez et al., 2010; Taheri and Zhalebaghi, 2017; Yaramasu et al., 2015). However, the problem of unbalanced neutral point voltage has been a critical issue in NPC inverters since it deteriorates the three-phase currents and causes uneven voltage stress on the switching devices leading to catastrophic failure (Chen et al., 2019; Jiang et al., 2019). Therefore, balancing of neutral point voltage is needed for a reliable and stable operation of the three-level NPC inverter. Several neutral point voltage balancing methods have been proposed in the past based on the employed modulation strategies. In (Bharatiraja et al., 2014; Mishra et al., 2003; Mouton, 2002; Xia et al., 2011), neutral point voltage control methods based on space vector pulse width modulation (SVPWM) has been studied. However, these methods greatly depend on the load power factor and cause significant low-frequency oscillation in the neutral point voltage at higher modulation index and lower power factor. In Ben-Brahim (2008), Lee et al. (2016) and Xia et al. (2017), neutral point voltage control methods based on discontinuous pulse width modulation (DPWM) have been proposed, but these have not mitigated the low-frequency oscillation in the neutral point voltage.

This paper introduces a novel control technique for balancing the DC link voltages of a three-phase three-level NPC inverter, which is working as a power interface between PV and a three-phase utility grid. The balancing of the DC link voltages of the centralised inverter has been achieved under the following conditions:

1) Under three-phase balanced grid without non-linear load, operating with several conditions like, with reference active and reactive power at the grid, maximum power point tracking (MPPT) mode of operation and during the absence of PV generated power. The DC link voltage balancing from the three-level boost converter has also been established which justifies its importance in the system. In addition to this, the power loss occurred in different parts of the system has been studied in detail. The dependency of the total converter loss and system efficiency on the ambient temperature has also been discussed under this subsection.
2) In presence of a three-phase non-linear load being connected at the point of common coupling (PCC). The control strategy for maintaining the waveform quality of the grid current in presence of non-linear current has been established.

The remaining sections of the manuscript have been summarised as follows: Section 'System Configuration' discusses the possible schematic diagrams of the entire system. Section 'Control Architecture' elaborates the control techniques required for implementing the above-mentioned conditions. Section 'Operation without Non-linear Load' presents the system operation with utility grid in absence of any non-linear load showing the simulation results with analysis of power loss in the system. Section 'Operation with Non-linear Load' describes the operation with utility grid considering the non-linear load. Section 'Conclusion' concludes the manuscript.

2. System Configuration

The general structure of the PV grid interconnected system consists of a PV array connected to the utility grid through a power conversion system. The power conversion may be of two stages; in this case a three-level DC–DC boost converter along with a three-phase three-level NPC centralised inverter have been considered (Figure 1a). The three-level boost converter offers many advantages as compared to conventional boost converters such as lower input inductance, reduced switching and reverse recovery losses and control of DC link voltage balancing at the output (Chen and Lin, 2014; Kwon et al., 2008). The power conversion stage is connected to the grid through a

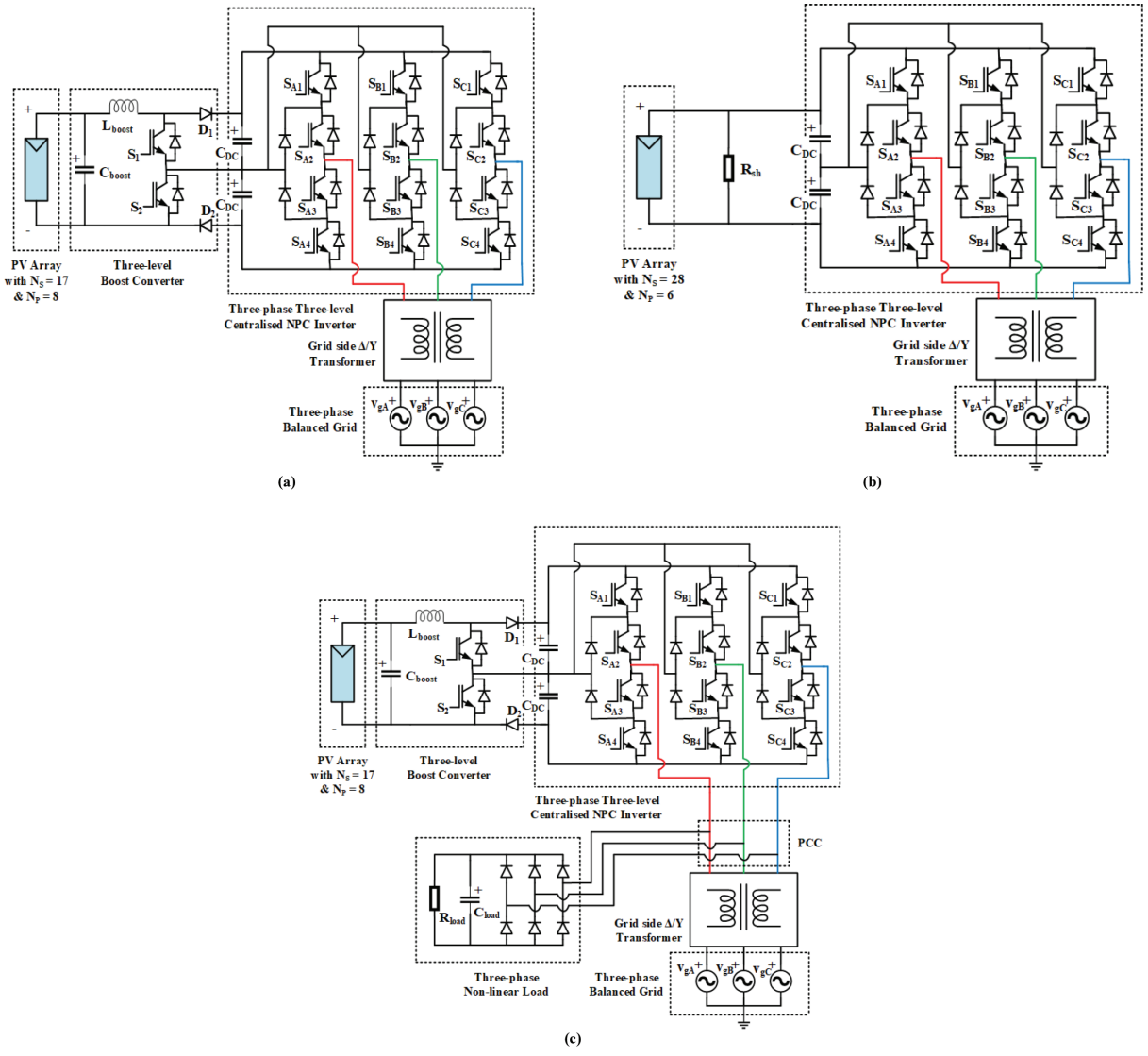


Fig. 1. Schematic diagram of the PV generated grid-connected system with (a) Two stage power conversion, (b) Single stage power conversion, (c) Two stage power conversion in presence of non-linear load at PCC. PCC, point of common coupling; PV, photo voltaic.

three-phase delta/wye transformer for achieving the grid voltage level. A proper design of leakage reactance of the transformer will eliminate the requirement of any passive filter for minimising the harmonic distortions of the inverter output voltage.

The power conversion can be of single-stage also; consisting of only the centralised inverter (Figure 1b). The elimination of the boost converter stage reduces the power semiconductor losses incurred. But this requires the increment of the number of series connected PV modules in a string so as to achieve the minimum DC link voltage level and hence decreases the number of parallel connected strings to maintain the same PV generated power. Another major difference of this single-stage power conversion based system compared with the two-stage power conversion is that all the control strategies (MPPT, DC link voltage balancing control etc.) have to be implemented for the centralised inverter only. The detailed control structures have been discussed in the next section.

To establish the AF characteristics of the centralised inverter, the schematic diagram as shown in Figure 1c has been considered. A highly non-linear load consisting of a three-phase diode bridge (uncontrolled) rectifier with resistive-capacitive load has been connected at the PCC. The location of PCC has been chosen before the grid side delta/wye transformer to justify that the active filtering is implemented by the centralised inverter alone and not by the grid side transformer. The detailed control technique has been conversed in the next section.

3. Control Architecture

Note that having several functionalities of the power conversion stage results in different control strategies employed for the overall system. The major control blocks have been described in the following subsections.

3.1. DC link voltage balancing control

The balancing of the DC link capacitor voltages can be controlled either from the three-level DC–DC boost converter or from the three-phase three-level NPC inverter for the two-stage power conversion system, however for the single stage system it has to be controlled from the centralised NPC inverter only.

For balancing the DC link voltages of NPC inverter, the concept of space vector diagram has been used in this paper. For a three-phase three-level NPC inverter, the pole voltage in each phase can have three possible voltage levels namely $+\frac{V_{DC}}{2}$, *0* and $-\frac{V_{DC}}{2}$, respectively depending on the switching combinations (Table 1), where V_{DC} is the total DC bus voltage. It is to be noted that the inverter pole voltage of a particular phase *i* (i $\in$ A,B,C) (Table 1) is defined as the voltage between the inverter outputs *i*-th phase leg and the mid-point of the DC link capacitor. The inverter pole voltage levels have been demarcated as '+' '0' and '–' in the space vector diagram and therefore constituting 27 possible switching states which result in 19 different space vectors (Figure 2). These space vectors can be subdivided as small, medium and large vectors depending on the magnitude of the resultant voltage. An investigation on these vectors reveals that each sub categorised vector has its unique effect on the mid-point current flow of the NPC inverter.

Table 1. Switching sequence of three-phase three-level NPC inverter

Switches in conduction	Inverter pole voltage	Demarcation in Figure 2
S_{i1}, S_{i2}	$+\frac{V_{DC}}{2}$	+
S_{i2}, S_{i3}	0	0
S_{i3}, S_{i4}	$-\frac{V_{DC}}{2}$	-

NPC, neutral point clamped.

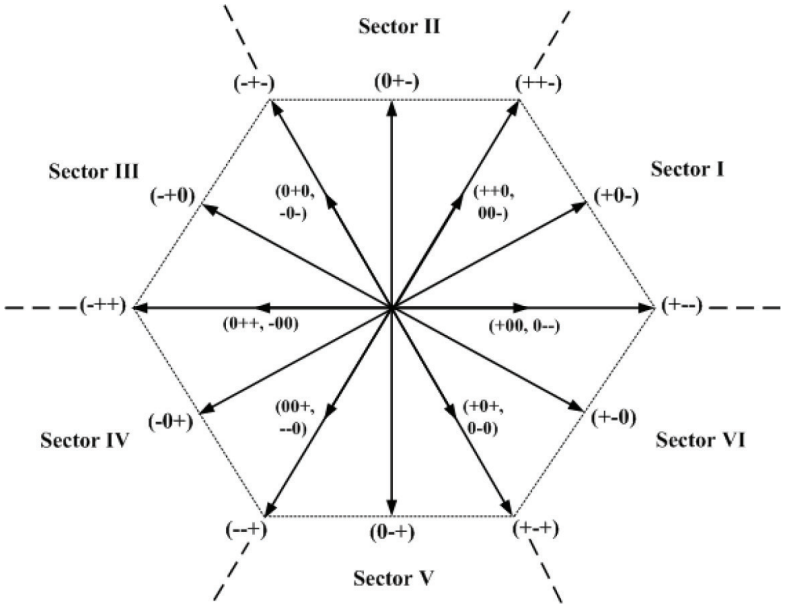


Fig. 2. Space vector diagram for three-phase three-level NPC inverter. NPC, neutral point clamped.

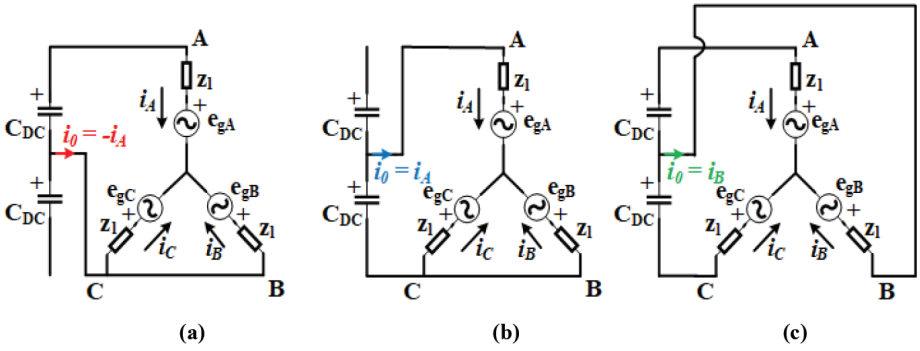


Fig. 3. Mid-point current analysis in sector I of three-phase three-level NPC inverter for (a) (+00) small vector, (b) (0 –) small vector, and (c) (+0–) medium vector. NPC, neutral point clampedl.

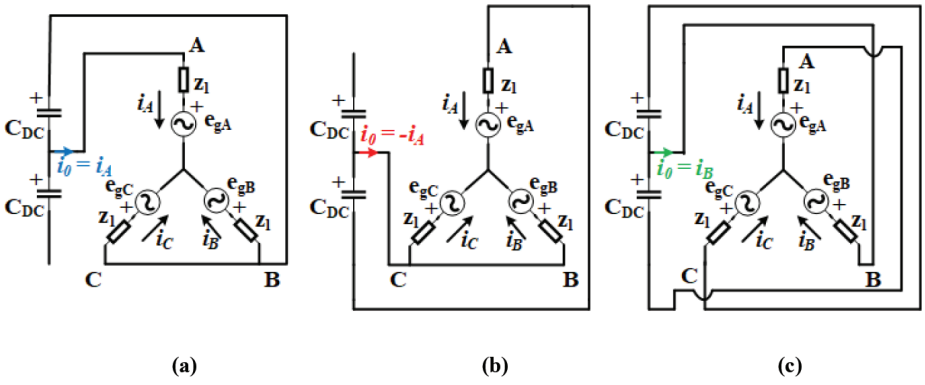


Fig. 4. Mid-point current analysis in sector IV of three-phase three-level NPC inverter for (a) (0++) small vector, (b) (−00) small vector, and (c) (−0+) medium vector. NPC, neutral point clamped.

Considering one leg of the three-phase NPC inverter, it is evident that the individual DC link voltages become unbalanced whenever there is a flow of mid-point current (i_0). In other words, the unbalancing of the individual DC link voltages occurs only when the switching state '0' is accessed. This also concludes that only the small and medium vectors have their effects on the voltage unbalancing since none of the large vectors has '0' as their switching states. The medium vectors result in the mid-point current to flow in a particular direction and, for small vectors, the two multiplicities of a particular small vector have the opposite effect on the mid-point current flow (Figures 3a, b and 4a, b) and hence they can be properly utilised to make the average mid-point current over a switching period to be 0. The small vectors are seen to have opposite effects when two different sectors are considered. For example, in Figures 3 and 4, the similar small vector multiplicities ((+00) and (0++), (0–) and (–00)) of sectors I and IV are seen to have the exact opposite effect on the mid-point current flow. A similar analysis on the other sectors reveals that the odd sectors (i.e. I, III, V) have the opposite effect as their even counterparts (i.e. II, IV, VI). The overall analysis of the effect of all the voltage space vectors on the mid-point current flow has been tabulated in Table 2. It is to be noted that the 0 voltage vectors ((+++), (– –) and (000)) do not contribute for the mid-point current flow and hence they haven't been considered for this analysis.

The amount of common-mode DC offset that needs to be added with the three-phase normalised modulated signals for selecting the space vector pattern with appropriate dwell times is determined based on the concept of making the average of the mid-point current over a switching time-period to be 0. It has already been established that the mid-point current flows during '0' switching state only i.e. when the switches S_{i2} and S_{i3} (i ∈ A,B,C) are in conduction. Therefore, if m_i ($-1 \le m_i \le 1$) be the normalised modulating signal for the *i*-th phase (i ∈ A,B,C), then at any instant of time, the mid-point current can be expressed in terms of the phase currents as follows

$$i_0 = (1-m_A)i_A + (1-m_B)i_B + (1-m_C)i_C$$

$$\text{or, } i_0 = (i_A + i_B + i_C) - (m_A i_A + m_B i_B + m_C i_C) \quad (1)$$

Table 2. Mid-point current analysis of three-phase three-level NPC inverter

Sector	Voltage space vector	Category	Mid-point current
I	(+00)	Small	$-i_A$
	(0 –)	Small	i_A
	(+ –)	Large	*0*
	(+0-)	Medium	i_B
II	(++0)	Small	i_C
	(00-)	Small	$-i_C$
	(++-)	Large	*0*
	(0+-)	Medium	i_A
III	(0+0)	Small	$-i_B$
	(-0-)	Small	i_B
	(-+-)	Large	*0*
	(-+0)	Medium	i_C
IV	(0++)	Small	i_A
	(-00)	Small	$-i_A$
	(-++)	Large	*0*
	(-0+)	Medium	i_B
V	(00+)	Small	$-i_C$
	(–0)	Small	i_C
	(-+)	Large	*0*
	(0-+)	Medium	i_A
VI	(+0+)	Small	i_B
	(0-0)	Small	$-i_B$
	(+-+)	Large	*0*
	(+-0)	Medium	i_C

NPC, neutral point clamped.

Considering the neutral path to be isolated i.e. the summation of three-phase inverter output currents at any instant of time to be 0, then the Eq. (1) can be rewritten as,

$$i_0 = -(m_A i_A + m_B i_B + m_C i_C)$$

$$\text{or, } i_0 = -\sum_{i \in A,B,C} m_i i_i \tag{2}$$

From Eqn. (2), it can therefore be concluded that the common-mode offset to be added with the three-phase normalised modulating signals should be such that the summation of $m_i i_i$ for all the three-phases becomes 0 over a switching time-period. The parameters of the DC-link voltage balancing controller have been designed based on this concept to compensate for the voltage difference between the individual DC link capacitors. Figure 5 shows the overall block diagram for controlling the centralised inverter. The normalised modulating signals m_{ABC} have been generated depending on the reference inverter currents i.e. the required active and reactive powers at the grid. The common-mode injection function m_{inj} which has been added with these generated normalised modulating signals to yield a centred SVPWM, is given as follows

$$m_{inj} = -\frac{(m_{max} + m_{min})}{2} \tag{3}$$

where m_{max} and m_{min} are the maximum and minimum of the generated three-phase normalised modulating signals m_{ABC}, respectively.

The sector determination block, which has been demonstrated in Figure 6, shows that it generates +1 when the sector is either I, III or V and generates -1 when the sector is their even counterparts. A ceiling function (y = [u]) has been used for this purpose to find out the sector in which the reference voltage vector lies in depending on the phase angle of mABC and iABC as shown in Figure 6. Finally, the amount of common-mode offset to be added with the centered modulating signals to balance the DC link voltages has been determined by the output of the DC link voltage balancing PI controller.

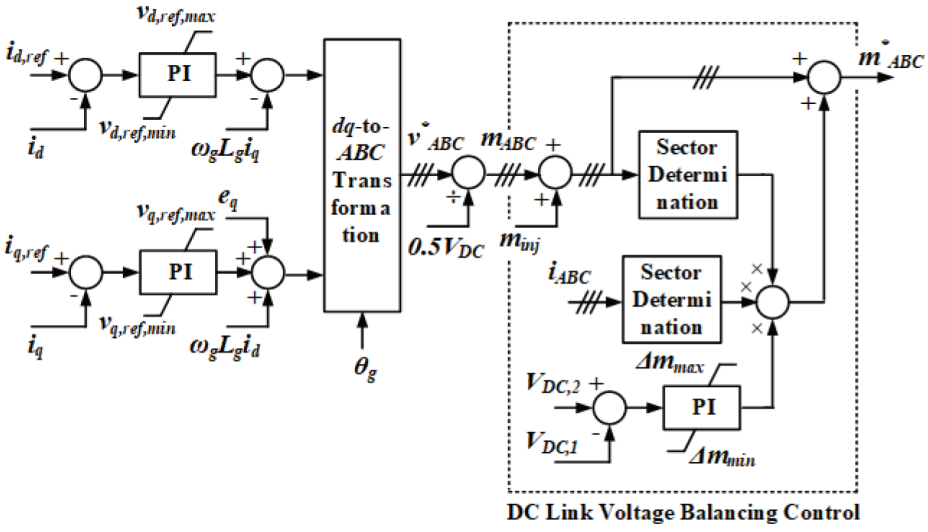


Fig. 5. Block diagram for controlling the three-phase three-level centralised NPC inverter. NPC, neutral point clamped.

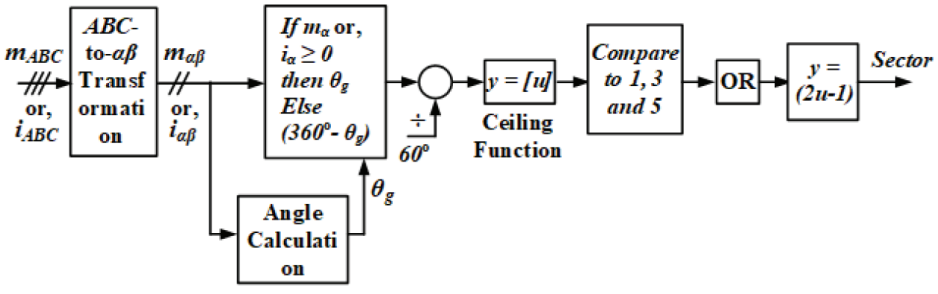


Fig. 6. Detailed block diagram showing the sector determination.

In case of two-stage power conversion, the presence of the three-level DC–DC boost converter adds to the flexibility in controlling the individual DC link capacitor voltages. Following the maximum power extraction from the PV panel at a specific irradiance and temperature, the duty ratio (d^*) has been yielded as shown in Figure 7. This duty ratio (d^*) has been adjusted to balance the individual DC link capacitor voltages at the output side of the boost converter (Figure 7). The DC link voltage balancing controller in this case generates the compensating duty ratio (d_{comp}) depending on the difference in voltage of the DC link capacitors. This compensating duty ratio compensates for the voltage imbalance between the DC-link capacitors and generates the duty ratios for the two switches in the three-level boost converter. It is to be noted that for generating the duty ratio of the three-level boost converter switches, the total DC bus voltage (V_{DC}) has been considered, which is the output voltage to this converter as the converter dynamics does not support the regulation of both the input and output voltages at the same time.

3.2. Harmonic minimisation control

The exponential growth of the power semi-conductor devices in different types of loads connected at the utility grid results in a significant non-linear behaviour and inherently distorts the grid current profile. So, for the centralised inverter, it is essential to perform as an AF so that the grid current remains nearly sinusoidal in the presence of these non-linear loads. So, the main objective of this control strategy is to regulate the different harmonic components that are present in the inverter output current in such a way that the inverter supplies the required non-linear current of the load and maintains the power quality at the utility grid.

To accomplish the harmonic minimisation of the grid current, the normalised modulating signals (m_{ABC}) for the centralised inverter have been generated from the sensed grid current ($i_{g,ABC}$). The filtering technique basically lies in the generation of the reference frame angle (θ_g) of the grid which has been used for transforming the instantaneous grid currents from ABC to dq reference frame. The grid currents thus generated in the dq reference frame has been used as the reference inputs for producing the normalised modulating signals for the inverter.

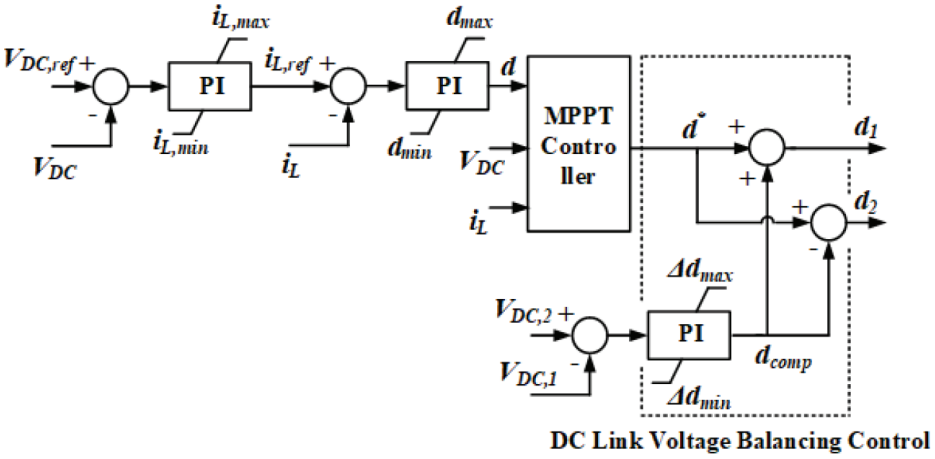


Fig. 7. Block diagram for controlling the three-level boost converter.

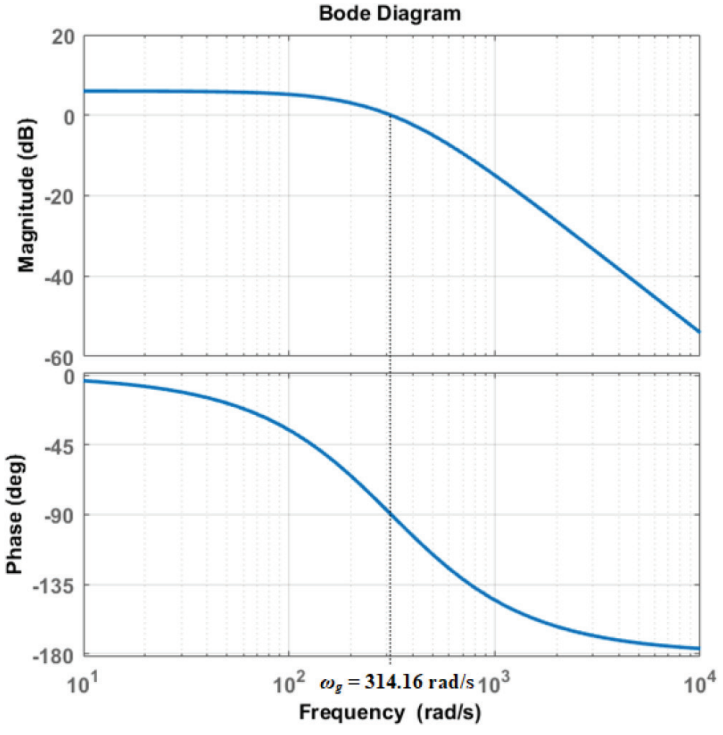


Fig. 8. Bode magnitude and phase plot of the delay transfer function $G_d(s)$.

A transfer function block $G_d(s)$ has been used to delay the input signal by 90°, as shown in Figure 9, is expressed as follows

$$G_{\mathrm{d}}(\mathrm{s}) = 2 \times \frac{(2\pi \times 50)^2}{(\mathrm{s} + 2\pi \times 50)^2} \tag{4}$$

Figure 8 shows the bode magnitude and phase plot of the transfer function. Also, the expression of $G_d(s)$ (Eqn. 4) reveals that, at the fundamental grid frequency ω_g

$$\left|G_{\mathrm{d}}\left(\mathrm{j}\omega_{\mathrm{g}}\right)\right| G_{\mathrm{d}}\left(\mathrm{j}\omega_{\mathrm{g}}\right) = 1 - 90^{\circ}$$

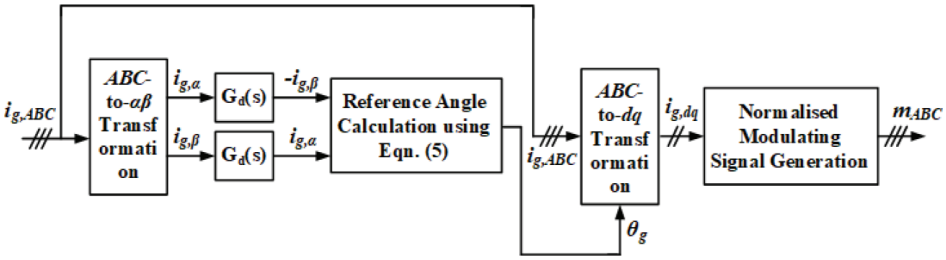


Fig. 9. Block diagram for the centralised inverter to control the grid current harmonic components in presence of non-linear load.

This point has also been marked in Figure 8 (at ω_g = 314.16 rad/s) which has the magnitude and phase values of 0 dB and –90°, respectively. Also, from the bode plot of the transfer function $G_d(s)$, it can be concluded that the dB magnitude gain of the transfer function starts to reduce as the harmonic order decreases from the fundamental. This low-pass filter characteristic of the transfer function $G_d(s)$ helps to minimise the other significant lower order harmonic components which are present in the grid current profile.

The block diagram for minimising the grid current harmonic components in presence of a non-linear load is shown in Figure 9. The sensed three-phase grid currents ($i_{g,ABC}$) have been transformed into the stationary αβ reference frame components ($i_{g,\alpha\beta}$). The grid current components in αβ stationary reference frame have then been delayed by 90° using the delay transfer function $G_d(s)$. Finally, the grid current is transformed from ABC to dq reference frame rotating synchronously with the reference grid phase angle (θ_g) which is calculated as follows

$$\theta_g = \cos^{-1}\left(\frac{i_{g,\alpha}}{\sqrt{i_{g,\alpha}^2 + i_{g,\beta}^2}}\right) \tag{5}$$

The grid current components in dq reference frame have been used as the reference currents for the generating the normalised modulating signals (m_{ABC}) for the centralised inverter.

4. Operation without Non-linear Load

This section presents the operation of the centralised inverter under balanced utility grid in absence of any non-linear load connected. The simulation results and the power loss analysis of the system have been presented in the following subsections.

4.1. Simulation results

This subsection illustrates the simulation of the PV centralised inverter connected to a three-phase balanced grid. Refer to the schematic diagram of Figure 1(a), the simulation has been performed in PLECS software tool considering the parameters as tabulated in Table 3. The total simulation time of 1.3 s has been divided into two parts: day time (0–1 s) and night time (1–1.3 s). During the day time, the reference active power consumed by the grid has been set as 5 kW till 0.25 s when the MPPT operation is considered. A reference grid reactive power of 10 KVAR is considered at 0.6 s in order to study whether the system can fulfil the reactive power demand at the grid, even during the night time. The irradiation to the PV cells has been decreased linearly from 1,000 W/m^2 at 0.9 s to 0 W/m^2 at 1 s in a drooping rate of 10,000 W/m^2/s considering the twilight period, while the ambient temperature has been kept constant at 40 °C throughout the operation.

Figure 10 shows the different waveforms of the PV array subjected to the operations as mentioned before. It is evident from these waveforms that the PV array intends to generate maximum power during starting which has been limited by controlling the initial current. This initial current limit has been incorporated in the control structure for the three-level boost converter ($i_{L,max}$ in Figure 7). The generated power by PV eventually settles at 5 kW, supplying the active power demanded by the grid. At 0.25 s, when the MPPT has been operated, the PV array generates its maximum power within 0.4 s (Figure 10c) and supplies to the grid. This operating sequence confirms that the centralised inverter can be controlled to extract the active power from the PV array and supply it to the grid

Table 3. Specification of system parameters

Specification of PV array:
Nominal open-circuit cell voltage = 47.8 V
Nominal short-circuit cell current = 5.4 A Maximum power of the PV array = 27.2 kW under standard conditions (i.e. G = 1,000 W/m^2 & T = 25 °C)
Output capacitance at the PV array terminals = 10 μF
Specification of three-level boost converter:
Series inductance = 3.1 mH; Effective series resistance = 0.05 Ω Switching frequency = 5 kHz
Specification of three-phase three-level NPC inverter:
DC link capacitance = 4.7 mF; Rated capacitor voltage = 1,200 V Switching frequency = 5 kHz
Specification of grid side three-phase Δ/Y transformer:
Turns ratio = 1:10.585 Equivalent winding resistance referred to primary = 0.168 Ω Equivalent leakage inductance referred to primary = 10.64 mH Magnetising inductance = 1 H
Specification of three-phase utility grid:
Line-to-line grid voltage = 11 kV (rms) Per phase grid impedance = (0.6 + j0.974) Ω

NPC, neutral point clamped; PV, photo voltaic.

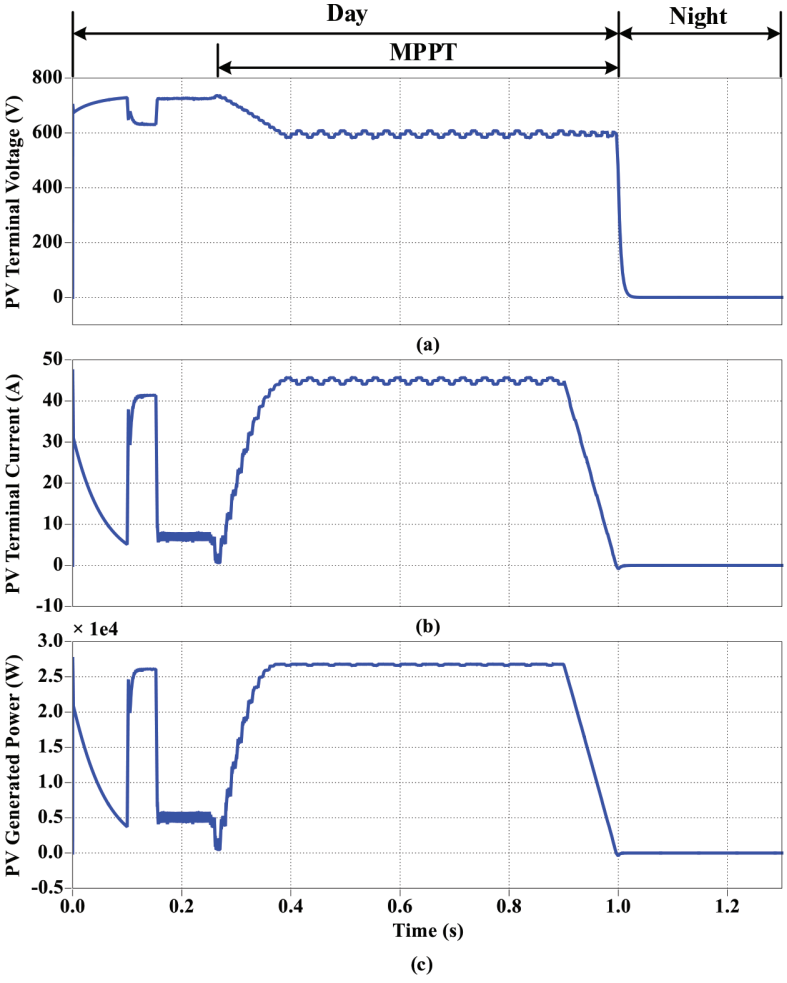


Fig. 10. Simulation results showing the waveforms of (a) PV array terminal voltage, (b) PV array terminal current and (c) PV generated power during different times of operation. PV, photo voltaic.

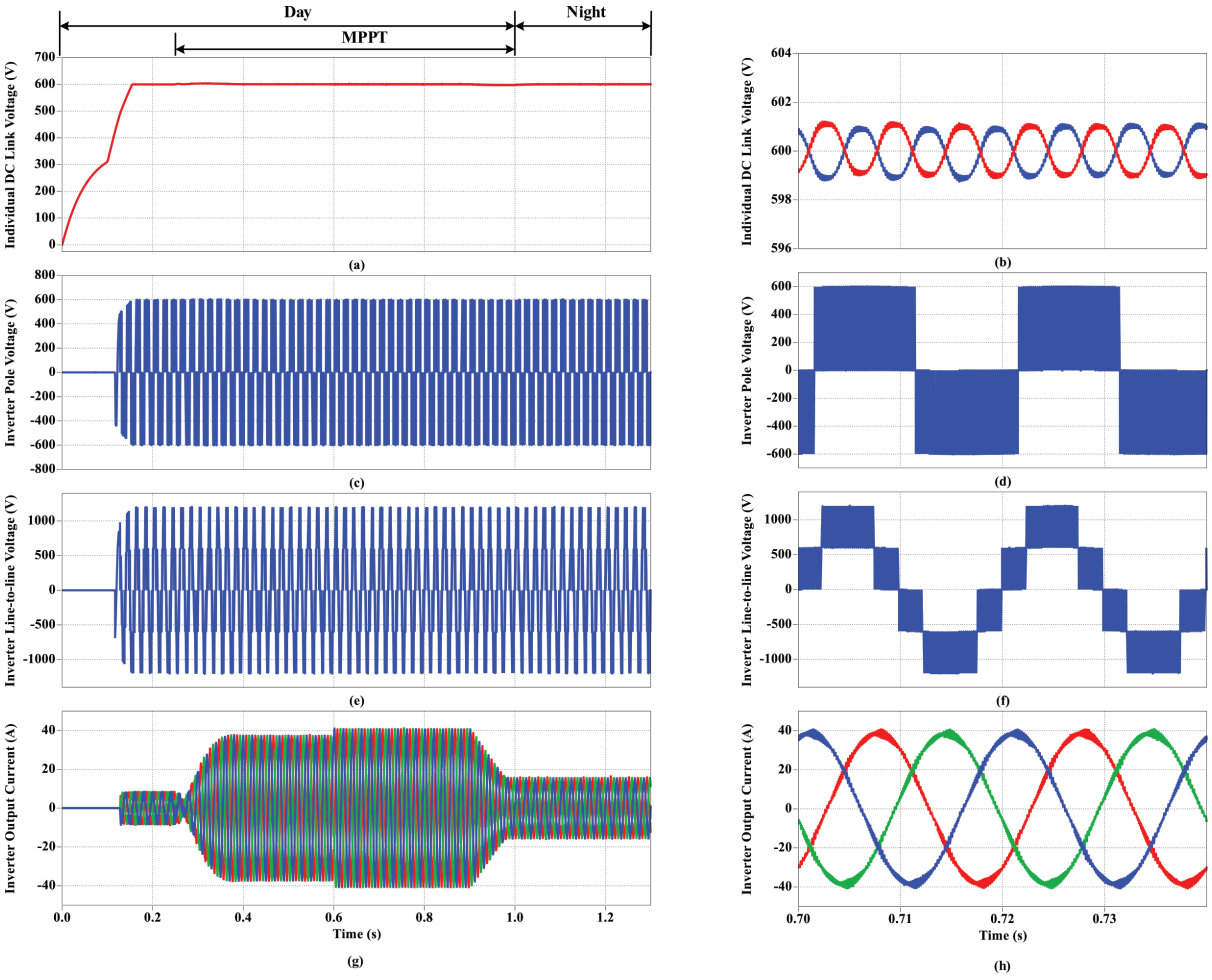


Fig. 11. Simulation results showing the waveforms of Individual DC link voltage for (a) entire simulation time, (b) two complete time periods; Inverter pole voltage for (c) entire simulation time, (d) two complete time periods; Inverter line-to-line voltage for (e) entire simulation time, (f) two complete time periods; and Inverter output current for (g) entire simulation time, (h) two complete time periods during different times of operation.

depending on whether the MPPT or non-MPPT operation is required. The PV generated power gradually reduces to 0 at 1 s confirming the end of day time.

The simulation results of the centralised inverter subjected to the corresponding operations have been shown in Figure 11. The individual DC link voltages rise up to their steady state value of 600 V within 0.2 s which ensures that the inverter produces the rated line-to-line voltage at its output to maintain the grid voltage level. The individual DC link voltages are seen to be balanced and unaffected corresponding to the different modes of operations (Figure 11a). Following the balanced individual DC link voltages, the inverter produces the required pole and line-to-line voltage at its output (Figures 11b, c). The inverter produces three-phase balanced currents at its output whose magnitudes change according to the active and reactive powers demanded by the grid (Figure 11d). During night time, in absence of the PV generation, the inverter alone supplies the current to the grid for fulfilling its reactive power requirement, thus working as a static synchronous compensator (STATCOM).

The electrical parameters of the grid are demonstrated in Figure 12 under different times of operation. At first, the grid is made ON only after the total DC link voltage reaches up to the minimum threshold voltage for maintaining the grid voltage level. Once the grid is made ON, the grid currents change their magnitudes according to the required power level (Figure 12b) while the grid voltage being steady throughout (Figure 12a). The grid active power is seen to follow the active power as generated by the PV array during day time (Figure 12c). The grid reactive power also tracks its commanded value (10 KVAR) from 0.6 s onwards (Figure 12d), ensuring the centralised inverter's operation as STATCOM. It is important to note that the incorporation of reactive power at the grid doesn't have any

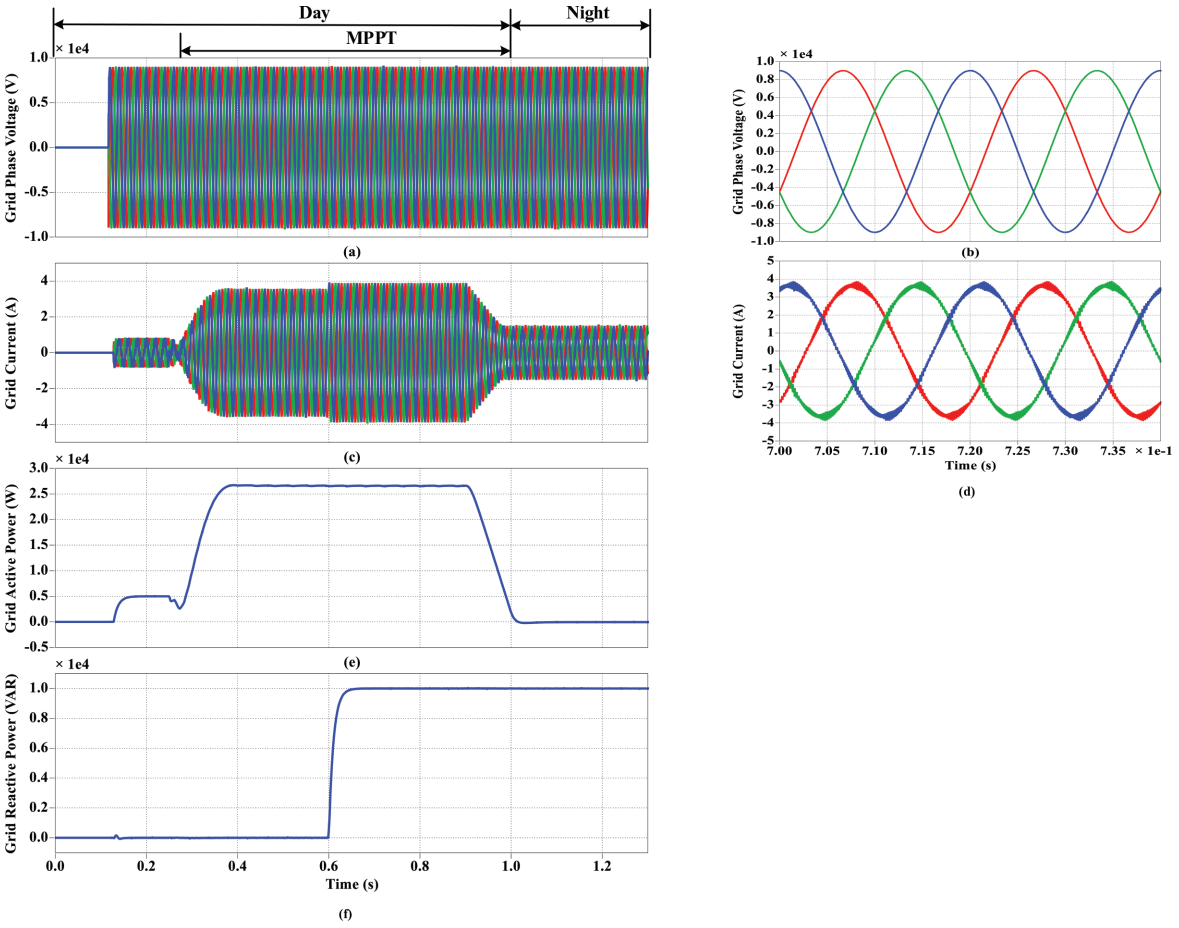


Fig. 12. Simulation results showing the waveforms of Grid phase voltage for (a) entire simulation time, (b) two complete time periods; Grid current for (c) entire simulation time, (d) two complete time periods; and (e) Grid active power for entire simulation time and (f) Grid reactive power for entire simulation time during different times of operation.

effect on neither of the active power and the DC link voltage profiles, showing the decoupling nature of the current controllers in dq reference frame. Also, before the grid is made ON, the individual DC link voltages are balanced by the three-level boost converter since the centralised inverter is not in operation.

4.2. Power loss analysis

This subsection presents the detailed description of the power loss occurring in different parts of the system and a comparative analysis with the single-stage power conversion system. The major contributors towards the total power lost in the system are mainly power semiconductor devices, grid side transformer and the non-ideal elements (for example, inductive resistance etc.) present in the system. The power dissipation in the semi-conductor devices happens mainly during its conduction state and it is known as the conduction loss while the loss occurring during its switching instants (turn ON & OFF) is known as the switching loss.

The switching and conduction losses are mainly calculated in terms of energies as follows,

$$\text{Energy lost during turn ON, } E_{ON} = \int_0^{t_{ON}} v_{ON} i_{ON} dt \tag{6}$$

where v_{ON} is the instantaneous voltage across the device during turn ON, i_{ON} is the instantaneous current through the device during turn ON and t_{ON} is the total turn ON time consisting of the current rise time (t_{ri}) and the voltage fall time (t_{fv}), energy lost during turn OFF

$$E_{OFF} = \int_{0}^{t_{OFF}} v_{OFF} i_{OFF} dt \tag{7}$$

where v_{OFF} is the instantaneous voltage across the device during turn OFF, i_{OFF} is the instantaneous current through the device during turn OFF and t_{OFF} is the total turn OFF time consisting of the voltage rise time (t_{rv}) and the current fall time (t_{fi}), hence total switching energy dissipated in the device,

$$E_{sw} = E_{ON} + E_{OFF} + E_{rr} \tag{8}$$

where E_{rr} is the reverse recovery loss during turn OFF of the anti-parallel diode across the device.

Similarly, conduction energy dissipated in the device can be obtained as follows,

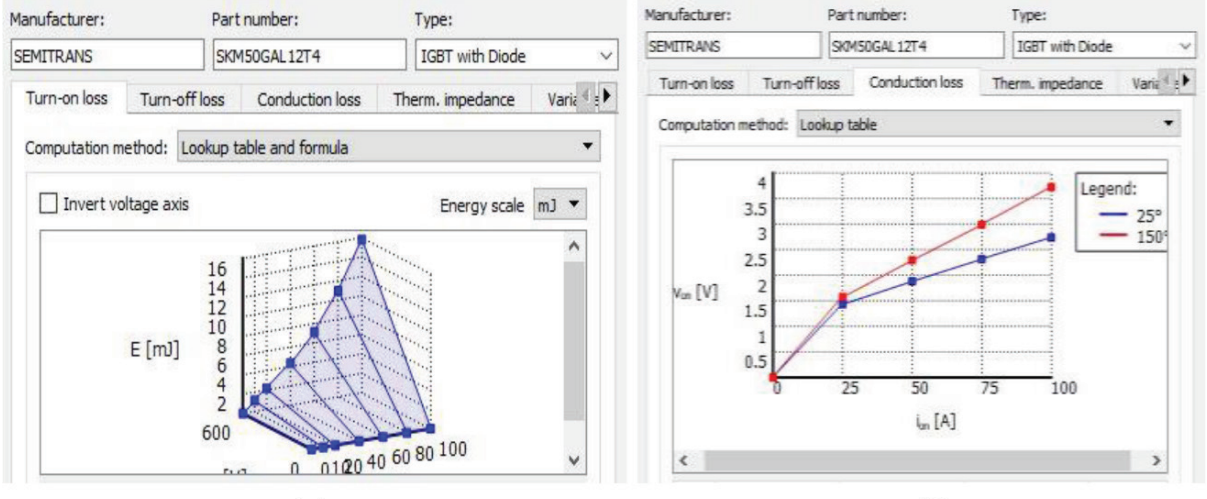
$$E_{cond} = \int_{0}^{t_{cond}} I_{ON,rms}^2 R_{CE,ON} dt \tag{9}$$

where $I_{ON,rms}$ is the root mean square value of the current through the device during its conduction, $R_{CE,ON}$ is the ON state resistance across the device and t_{cond} is the conduction time of the device.

The switching and conduction power dissipations can be obtained from the respective energy dissipations by averaging over a switching period which concludes that the total power dissipated in the device is proportional to its switching frequency.

To simulate the dissipated power in all the devices, the characteristics from the datasheet have been considered and incorporated in the PLECS software (Figure 13). The datasheet of a 1200 V/50 A Si IGBT (SKM50GAL12T4 datasheet, 2013) has been considered for this purpose. For switching loss, data from the characteristics of $E_{ON}/E_{OFF}/E_{rr}$ vs I_C and $E_{ON}/E_{OFF}/E_{rr}$ vs R_G have been extracted and incorporated in terms of look-up tables and temperature dependent equations (Figure 13a) since the operating temperature (40 °C) is different from the temperature for which these characteristics are defined. For conduction loss, the output characteristics of the device i.e. I_C vs V_{CE} for the two defined temperatures have been incorporated (Figure 13b), where I_C and V_{CE} are the collector current and collector-emitter voltage of the IGBT device, respectively. The switching and conduction power losses have been estimated by calculating switching average of the respective energy dissipations.

The power loss occurred in different parts of the system has been presented in Figure 14. Following the simulation of each IGBT switch present in the boost converter and in the centralised NPC inverter as discussed before, the power loss incurred due to these converters have been shown in Figures 14a, and b, respectively. The



(a) (b)

Fig. 13. Simulation of (a) Turn-on loss and (b) Conduction loss contributed by a power semi-conductor device in PLECS software.

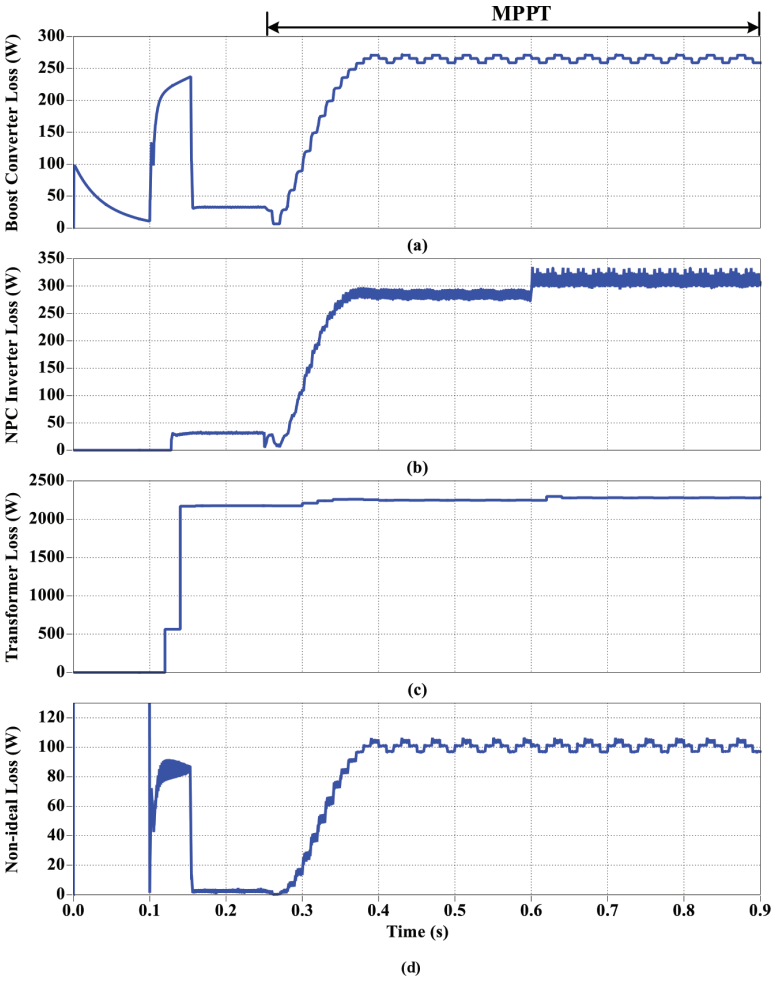


Fig. 14. Simulation results showing the power dissipated as (a) Boost converter loss, (b) NPC inverter loss, (c) Grid side transformer loss and (d) Non-ideal loss of the PV balanced grid-tied system with two-stage power conversion at ambient temperature of 40°C. NPC, neutral point clamped. PV, photo voltaic.

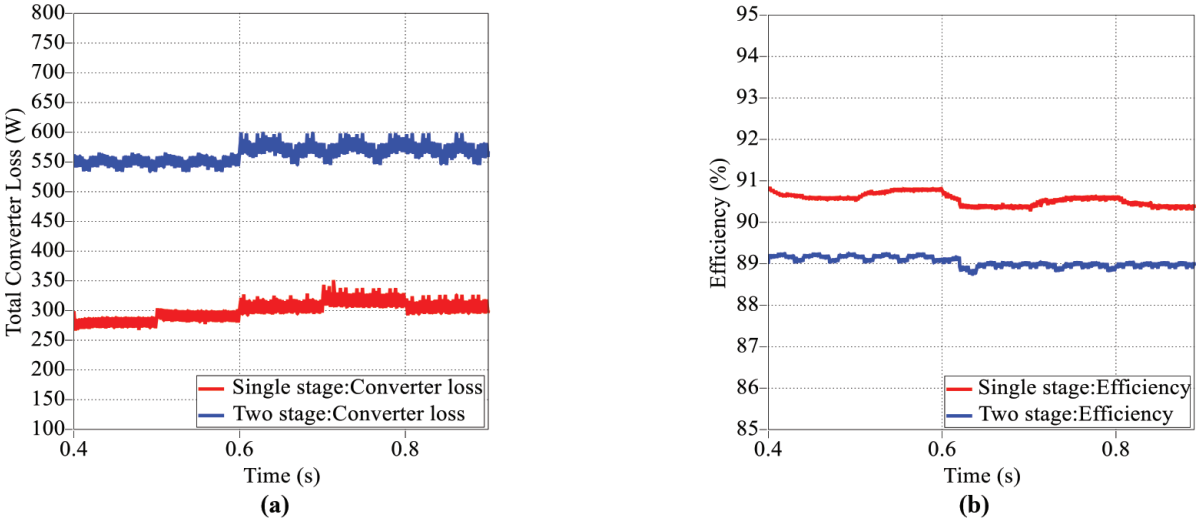


Fig. 15. Simulation results showing the comparison between the PV balanced grid-tied system with single-stage and two-stage power conversion in terms of (a) Total converter loss, and (b) Efficiency during MPPT operation at ambient temperature of 40°C. MPPT, maximum power point tracking; PV, photo voltaic.

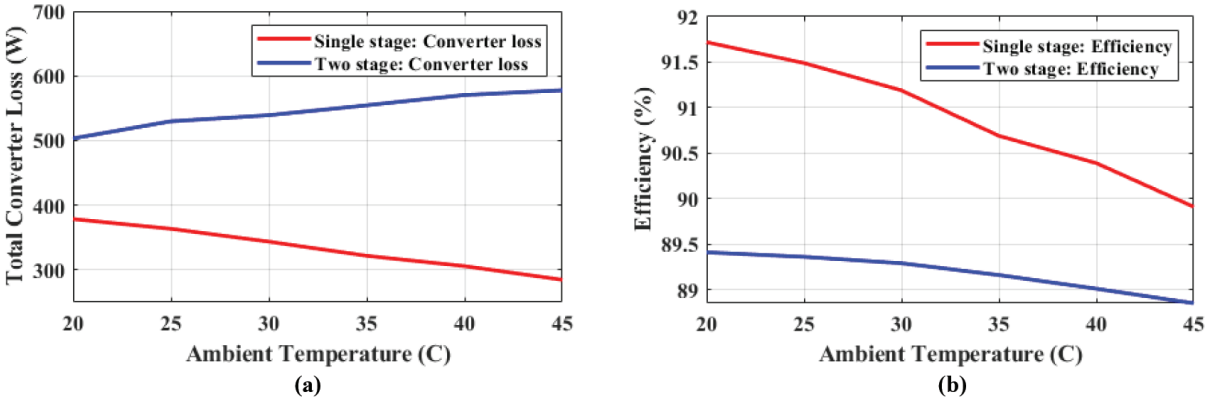


Fig. 16. Simulation results showing the comparison between the PV balanced grid-tied system with single-stage and two-stage power conversion in terms of (a) Total converter loss, and (b) Efficiency during MPPT operation at different ambient temperatures. MPPT, maximum power point tracking; PV, photo voltaic.

power dissipated in the grid side transformer and in the non-ideal elements has been presented in Figures 14c, and d, respectively. It is important to note that the power loss in the system increases with the increase in current i.e. the analysis is more significant during the MPPT operation. Hence for the comparative analysis, the results during the MPPT operation have only been considered.

The power loss analysis has also been carried out for the PV grid-connected system with single- stage power conversion (Figure 1b) and the results are compared with the two-stage power conversion system. Figure 15 shows the comparison of the two systems in terms of the total converter loss (Figure 15a) and the system efficiency (Figure 15b). The absence of the boost converter stage reduces the total converter loss and therefore improves the system efficiency in case of the single-stage power conversion system. This comparison has been carried out during the MPPT operation (0.4–0.9 s) maintaining the ambient temperature constant at 40 °C across all the heat sinks, which implies that the heat is uniformly distributed across all the heat sinks. It is to be noted that the MPPT power generated by the PV array changes with the variation of the ambient temperature. Therefore, a similar comparative study has also been executed when the ambient temperature of the PV array and all the heat sinks is varied in the range from 20 °C to 45 °C. The results of total converter loss and system efficiency for the variation of the ambient temperature have been plotted in Figures 16a and b, respectively. For the single-stage system, the converter loss decreases with the increase in the ambient temperature while the total converter loss for the two-stage system increases with the ambient temperature (Figure 16a). Hence, it can be concluded that the positive change in the boost converter loss with respect to the ambient temperature has been more dominant over the negative change in the NPC inverter loss. The system efficiency, however, decreases with increase in the ambient temperature for the both the cases (Figure 16b).

5. Operation with Non-linear Load

This section incorporates the three-phase non-linear load connected at the PCC. Referring to the schematic diagram of Figure 1c, the presence of the highly non-linear three-phase uncontrolled rectifier with Resistive Capacitive (RC) load of 7.5 kW introduces several harmonic components in the grid current. The centralised inverter therefore needs to perform as an AF to supply the non-linear load current and maintain the power quality at the grid side.

The waveforms of the grid voltage and current at the primary side of the grid side transformer in presence of the non-linear load have been shown in Figures 17a and b, respectively. The non-linear load current is seen to contain significant harmonic components (Figure 17c) and the inverter supplies this non-sinusoidal load current (Figure 17d) and maintains the waveform quality of the grid current. The simulation results of the centralised inverter in presence of the non-linear load current have been shown in Figure 18. The individual DC link voltages of the inverter are seen to be balanced with 0.39% of ripple voltage (Δv_{DC} = 2.301 V).

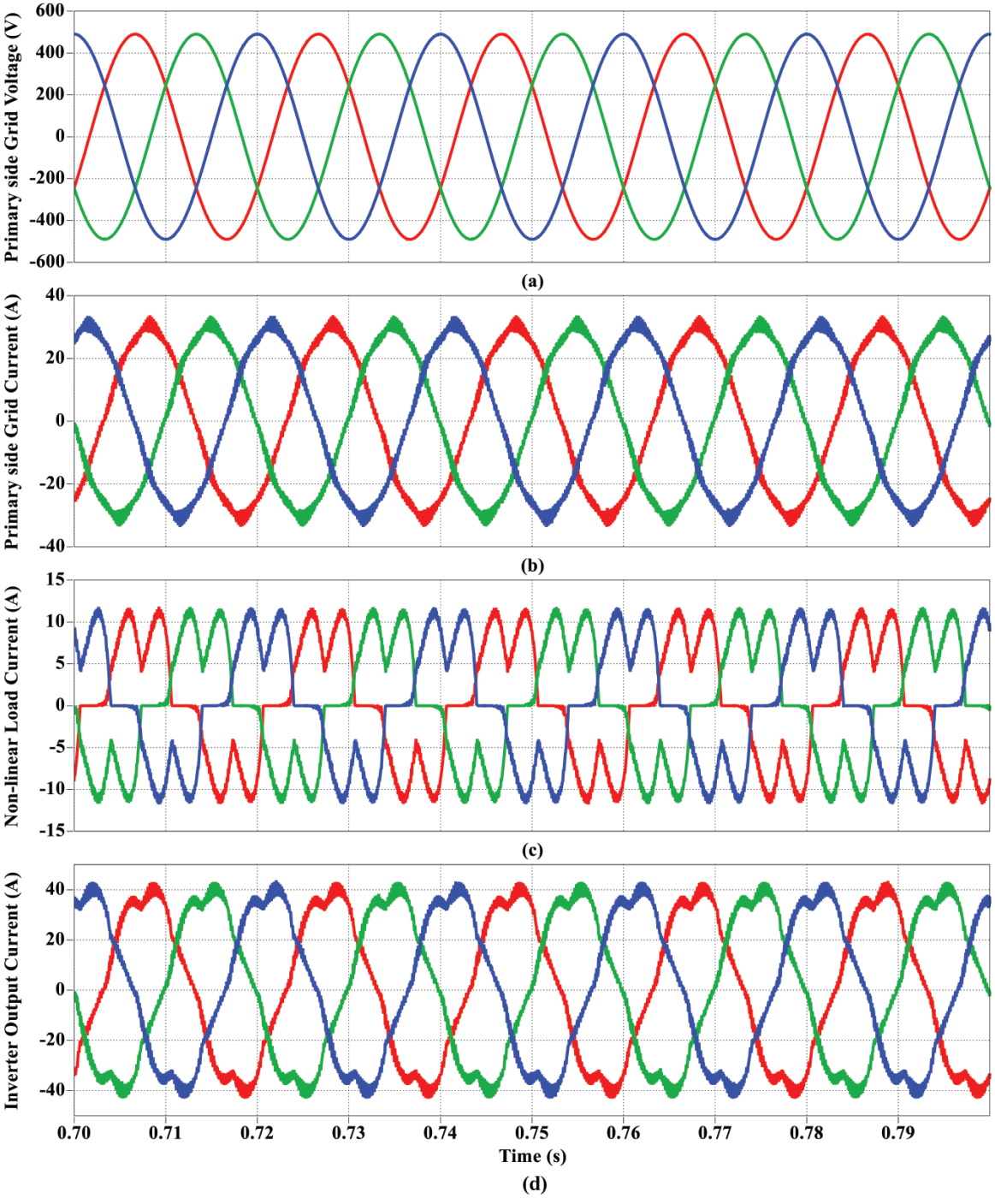


Fig. 17. Simulation results showing the waveforms of (a) Primary side grid voltage, (b) Primary side grid current, (c) Non-linear load current and (d) Inverter output current in presence of non-linear load at PCC. PCC, point of common coupling.

The operation of the centralised inverter as AF has been well established when the Fourier analysis of non-linear load current (Figure 19a) and primary side grid current (Figure 19b) are investigated. The highly non-linear load current consists of severe lower order harmonics except the fundamental (Figure 19a) and hence resulting in Total Harmonic Distortion (THD) of 36.61%. The minimisation of the harmonic contents by the centralised inverter reduces the non-fundamental lower order harmonics present in the grid current profile (Figure 19b). The THD of the grid current therefore remains at 2.20% which is below the IEEE Std 519-2014 grid code limit (IEEE Std 519-2014, 2014).

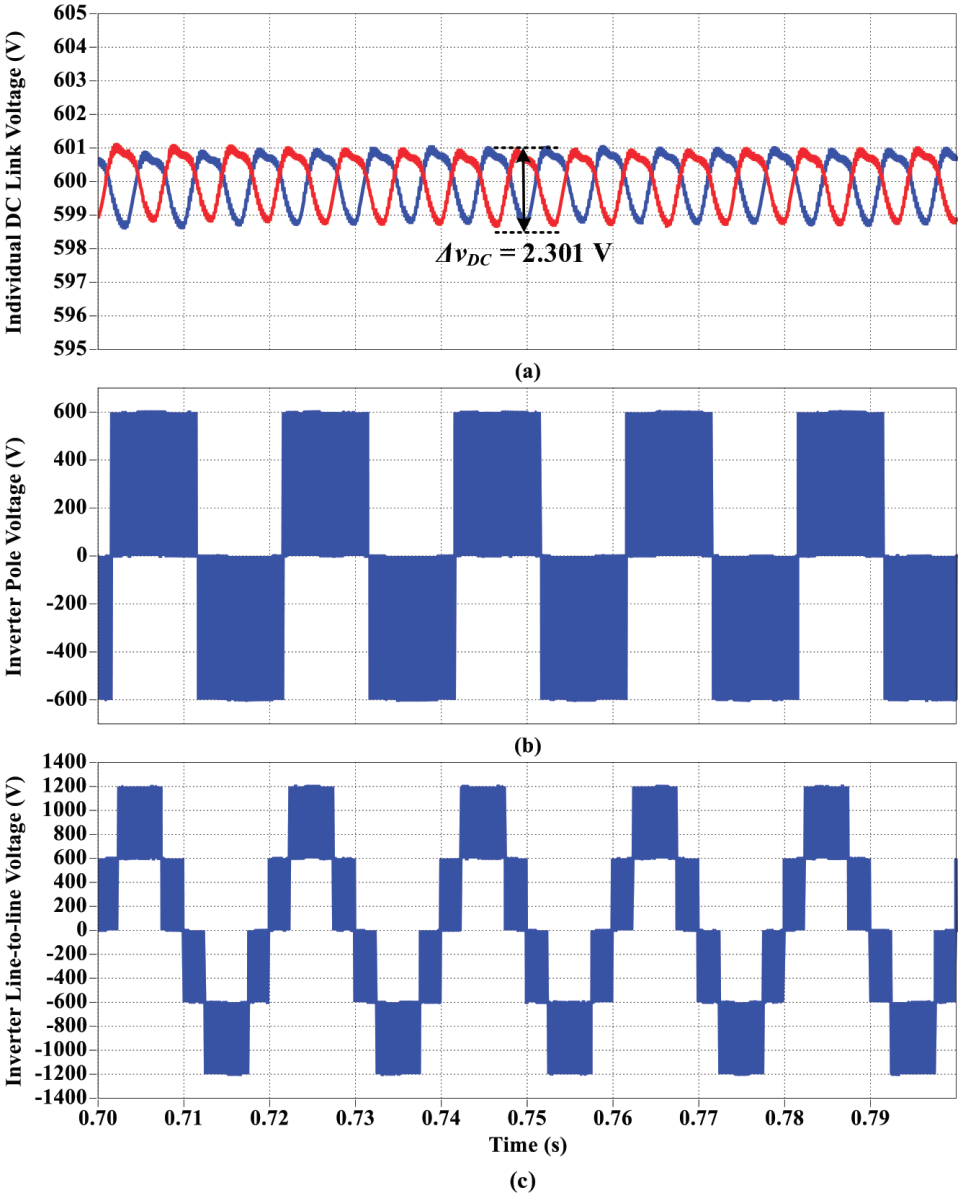


Fig. 18. Simulation results showing the waveforms of (a) Individual DC link voltage, (b) Inverter pole voltage and (c) Inverter line-to-line voltage in presence of non-linear load at PCC. PCC, point of common coupling.

6. Conclusion

In this paper, an improved SVPWM-based DC link voltage balancing control of a three-phase three-level NPC inverter operating as PV centralised inverter has been developed. Two possible power conversion stages for the PV grid-connected system have been presented namely, two- stage power conversion consisting of three-level boost converter and three-phase three-level centralised NPC inverter, and single-stage power conversion consisting of the centralised inverter only. The proposed SVPWM-based control method for balancing the individual DC link voltages of the centralised NPC inverter has been developed by formulating the mid-point current analysis for different voltage space vectors. The performance of the centralised inverter along with an investigation on balancing of the individual DC link voltages have been studied under different conditions of operation like, non-MPPT mode of operation with reference active power at the grid, MPPT mode of operation with reference reactive power at the grid and non PV generation during night time with reference reactive power at the grid. An extensive power loss analysis has also

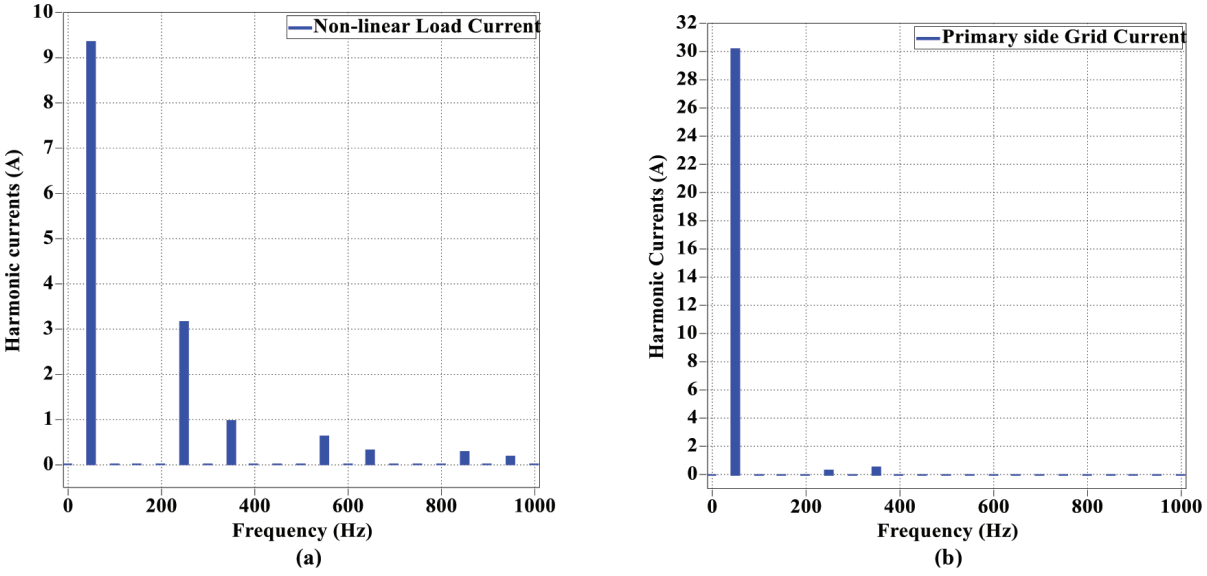


Fig. 19. Fourier spectrum analysis of (a) Non-linear load current and (b) Primary side grid current in presence of non-linear load at PCC. PCC, point of common coupling.

been carried out and the results of the single-stage and two-stage systems have been compared under same ambient temperature and with its variation in the range from 20 °C to 45 °C for depicting the system performance during different times of a day. The PV grid-tied system with the single-stage power conversion is seen to be more efficient with a maximum efficiency of 91.72% at 20 °C and with minimum converter loss of 284.74 W at 45 °C, where the two-stage conversion system has a maximum efficiency of 89.41% and a minimum converter loss of 503.23 W both at 20 °C. On the other hand, the single-stage power conversion system increases the required number of cells in the PV array for maintaining the total DC link voltage level and therefore increases the cost and maintenance of the PV array, hence restricting its suitability in medium/high voltage grid applications. The performance of the system in presence of non-linear load has also been studied and the operation of the centralised inverter as an AF is justified when the inverter current mostly supplies the harmonic components of the non-linear load current (36.61% THD) and maintains the waveform quality of the grid current with THD of 2.20% which is below the acceptable limits of IEEE Std 519-2014 grid code. The individual DC link voltages under the non-linear load operation are also found to be balanced with 0.39% of ripple voltage and hence not affected by the presence of non-linear load in the system.

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