Cascode Amplifiers with Low-Gain Variability and Gain Enhancement Using a Body-Biasing Technique

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***Abstract*—This paper presents a simple circuit technique to reduce gain variability with PVT variations in cascode amplifiers using a body-biasing scheme, while enhancing the overall gain of the amplifier. Simulation results of a standard telescopic-cascode amplifier, in two different nanoscale CMOS technologies (130 nm and 65 nm) show that the proposed compensated circuit amplifier exhibits a (DC) gain variability smaller (below ± 0.5 dB) than the original (uncompensated) circuit, while reaching a gain enhancement of about 3 dB. The required auxiliary biasing circuit dissipates around 5% of the main amplifier circuit.**

***Index Terms*—amplifier, body-biasing, cascode, CMOS analog circuits, PVT compensation**

I. Introduction

MOS devices are scaled down to increase speed and reduce area. However, this leads to short channel effects, which reduce the intrinsic gain. Therefore, high gain OpAmps are harder to design and cascode techniques are more difficult to employ [1], due to the supply reduction.

In analog CMOS circuit design, the transistor is preferentially used in saturation. The intrinsic gain of a MOS transistor is given by

$$A_{vi} = g_m/g_{ds} \quad (1)$$

where g_m is the transconductance and g_{ds} is the output conductance.

For a MOS device in saturation, assuming an approximate square law for the drain current, the transconductance is

$$g_m = \mu C'_{ox}(W/L)(V_{GS} - V_t)^2 \quad (2)$$

where μ is the carrier mobility, C'_{ox} is the oxide capacitance per unit of area, W and L are the width and length of the transistor, V_t is the threshold voltage, and V_{GS} is the biasing gate source voltage. With a short channel, if V_{DS} increases V_t decreases, thus increasing the drain current. This gives rise to an increase of g_{ds}. Thus, despite the increase of transconductance with scaling, the intrinsic gain is reduced [1]. This is illustrated in Table I.

TABLE I.
IBM DIGITAL CMOS TECHNOLOGY [2]

Node	nm	250	180	130	90	65
L	nm	180	130	92	63	43
V_{DD}	V	2.5	1.8	1.5	1.2	1
V_{th}	V	0.44	0.43	0.34	0.36	0.24
g_m (peak)	µS/µm	335	500	720	1060	1400
g_{ds}	µS/µm	22	40	65	100	230
g_m/g_{ds}	-	15.2	12.5	11.1	10.6	6.1

The temperature variation leads to a decrease in both the carrier mobility and the threshold voltage. In regards to the latter, it may decrease from 2 mV up to 4 mV for every 1º C rise [3]. As seen in (2), both these factors will have a direct effect on the transconductance of a transistor.

Also, process corners refer to the variation of fabrication parameters used in applying an integrated circuit design to a wafer. If a circuit running on devices fabricated at these process corners does not function as desired, the design is considered to have inadequate design margin.

Operational and transconductance amplifiers are, most probably, the most active building-block in analog and mixed-signal integrated circuits used in wireless and wire line communication systems. The work presented in this paper can provide improved energy efficient circuit amplifier architectures, robust to temperature and supply variations. This ensures that a circuit manufactured to work, will perform as expected, regardless of the environment conditions.

In this paper we present a circuit technique to reduce gain variability with temperature, supply and process variations in cascode amplifiers using a body-biasing circuitry and at the same time increase the overall amplifier gain by about 3 dB.

In section II we will describe the traditional cascode amplifier. In section III we present the PTAT body-biasing circuit, which is used to bias the cascode amplifier. In section IV we present the simulation results and finally in section V we draw the conclusions.

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II. Cascode Amplifiers

A single-stage operational transconductance amplifier (OTA) has usually a cascode configuration [4].

We consider a traditional cascode amplifier, shown in Fig. 1. The gain of this circuit is given by

$$A_v = g_{m1} \cdot \left[\frac{1}{g_{ds1}} \cdot \left(\frac{g_{m2}}{g_{ds2}}\right)\right] || R_B \quad (3)$$

where R_B is the resistance of the biasing current source, whose value is 100 µA and 150 µA for 65 nm and 130 nm technology, respectively. The positive supply voltage is 1.2 V.

Fig. 2 shows the variations g_m, g_{ds} and the intrinsic gain of transistor M_2 (g_m/g_{ds}) for 65 nm and 130 nm.

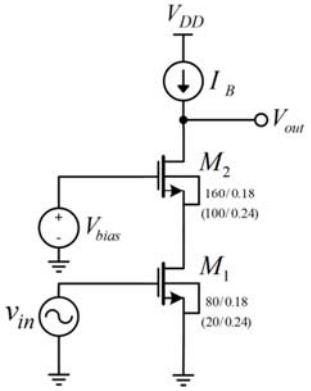

Figure 1. Cascode Amplifier. All transistor sizes (W/L) are in µm. Sizes without brackets are for a 65 nm technology and those within brackets are for a 0.13 µm one.

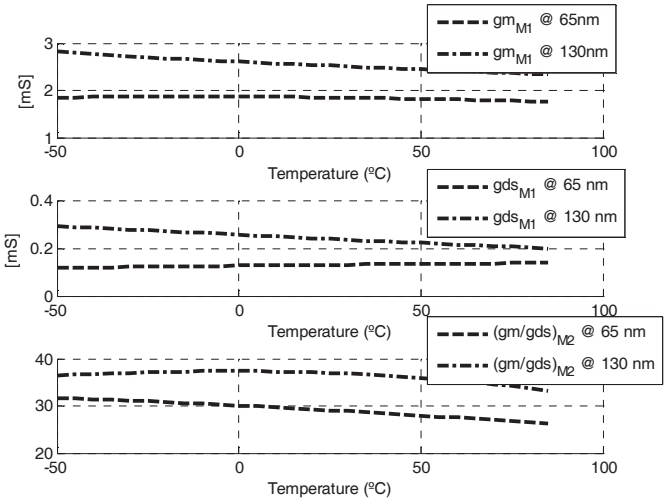

Figure 2. Parameter variation with temperature for both node technol`ogies.

III. Proposed Solution

The proportional-to-absolute-temperature (PTAT) circuit used in this paper is shown in Fig. 3. This is the "constant transconductance" bias circuit, proposed in [4], [5].

We investigate the variation with temperature of the voltages V_A, V_B, and V_C, when all the transistors are matched and R_1 = 2 kΩ.

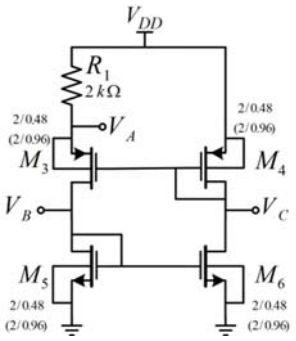

Figure 3. Constant Transconductance Bias. All transistor sizes (W/L) are in µm. Sizes without brackets are for a 65 nm technology and those within brackets are for a 0.13 µm one. The supply voltage is of 1.2 V.

The variation of V_A is deemed irrelevant, since it varies less than 5 mV for the temperature range (-40 ºC to +85 ºC). For both technology nodes, V_B decreases with temperature while V_C increases, as shown in Fig. 4.

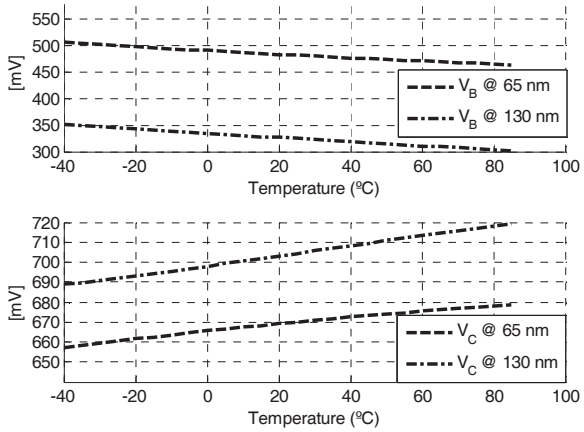

Figure 4. Voltage variation at the gate of M_4 and M_5 (for both node technologies).

The cascode amplifier (Fig. 1) with body-biasing by the circuit of Fig. 3 is shown in Fig. 5. The I_B current source is replaced with a current mirror, and every biasing voltage source is replaced with a MOSFET in diode configuration.

In section II we have plotted the variations of g_m and g_{ds} in 65 nm and 130 nm. The main objective is to choose one of these voltage variations and apply it to the bulk of the M_2 transistor of the cascode circuit, biasing it in order to reduce the variability of the intrinsic gain, thus narrowing the variability of the overall gain, and increase the total gain of the circuit. The voltage V_B is used, since it decreases with temperature (for either technology), as seen in Fig. 4. If it is applied to the bulk of the M_5 transistor, it reduces the amplifier gain variability.

After replacing the current source with the current mirror, the MOSFETS that compose it also needed to have a temperature-independent behavior. Thus, the bulk of M_{11} should be connected to a symmetrical voltage to that applied to the bulk of M_2. In order to do so, a mirrored version of the "constant transconductance" bias circuit was designed. The bulk of the M_{12} is directly connected to V_{DD}, thus avoiding the body-effect on this transistor.

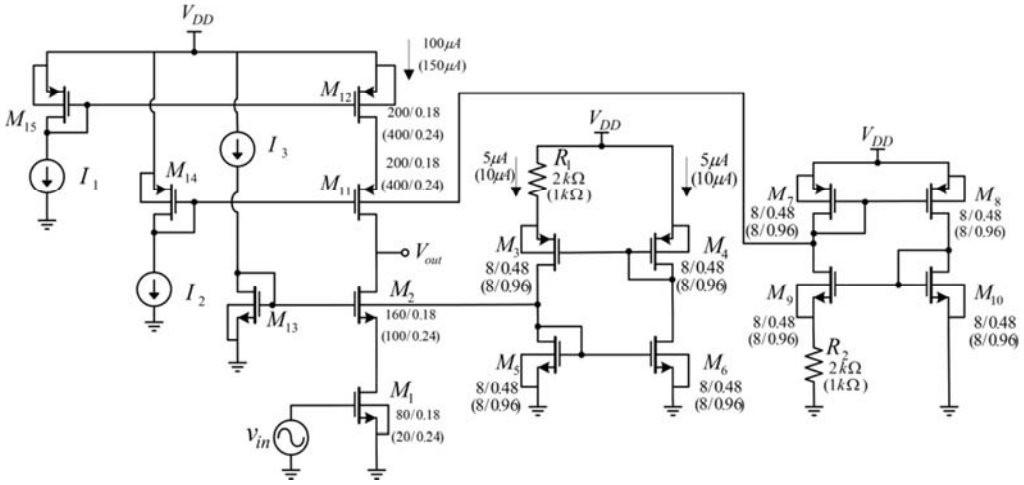

Figure 5. Telescopic-cascode with body-biasing circuitry. All transistor sizes (W/L) are in μm. Sizes without brackets are for a 65 nm technology and those within brackets are for a 0.13 μm one.

Figs. 6 and 7 present the variations of the transconductances of the $M_{1,2}$ transistors, when using body-biasing compensation.

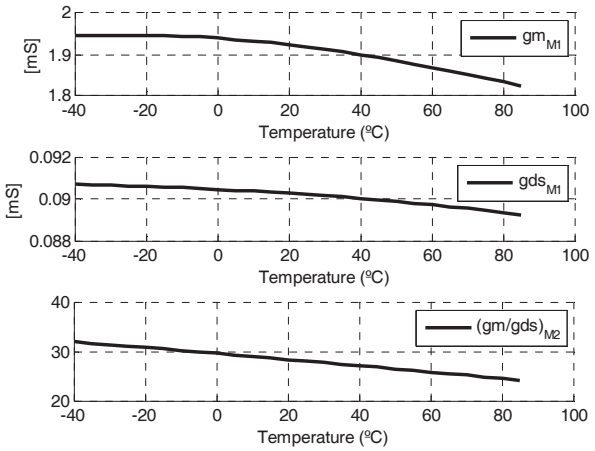

Figure 6. Parameter variation with temperature with body-biasing compensation for 65 nm.

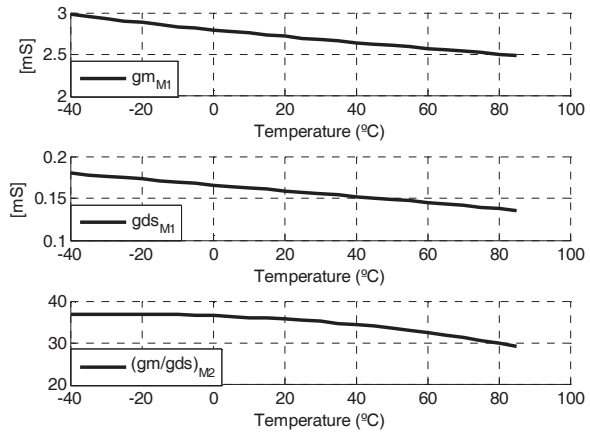

Figure 7. Parameter variation with temperature with body-biasing compensation for 130 nm.

As it can be seen, the intrinsic gain of the M_2 transistor has a lower variation than that obtained when no body-biasing technique is used (Fig. 2), for both node technologies. Furthermore, the g_{ds} of the M_1 transistor also reduces its value while g_m increases, thus boosting the gain.

IV. Simulations and Results

All simulations are performed using BSIM3v3 models for standard logic 65 nm and 130 nm CMOS technology. A supply voltage of 1.2 V is used and and the process variations considered are slow-slow (ss), typical-typical (tt) and fast-fast (ff). The temperature range is from -40 to +85 ºC.

In Fig 8, the gain of the circuit is plotted, for both technology nodes, with and without body-biasing technique. For both technology nodes the gain variability is lower when using the body-biasing circuitry. Furthermore, there is an enhancing of the gain by about 3 dB, as expected, as it was explained in section III. Therefore, lower gain variability can be achieved without degrading the overall gain of the amplifier.

With regard to supply variation, Fig. 9 shows that with a variation of ± 5% (1.14 V to 1.26 V) of the supply voltage, the body-biasing circuitry leads to a lower variability for the gain (below 1 dB). Some traces can be superimposed.

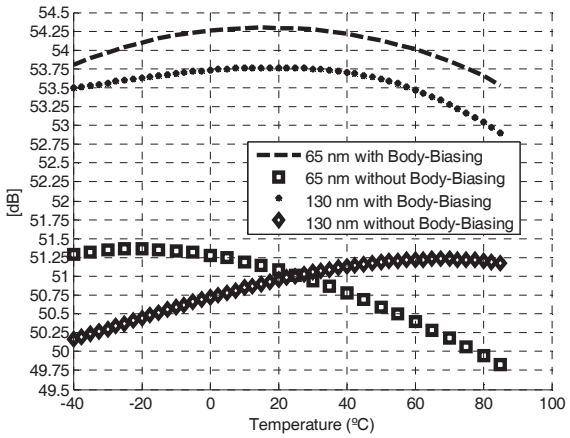

Figure 8. Overall gain variability with temperature for both technologies node (with and without body-biasing technique). [6]

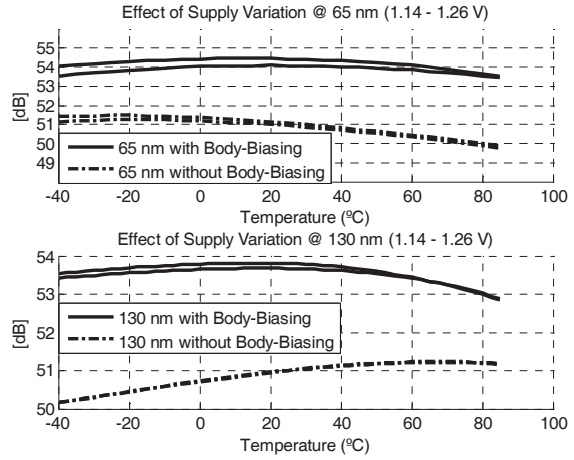

Figure 9. Overall gain variability with temperature & supply variation for both technologies node (with and without body-biasing technique). [6]

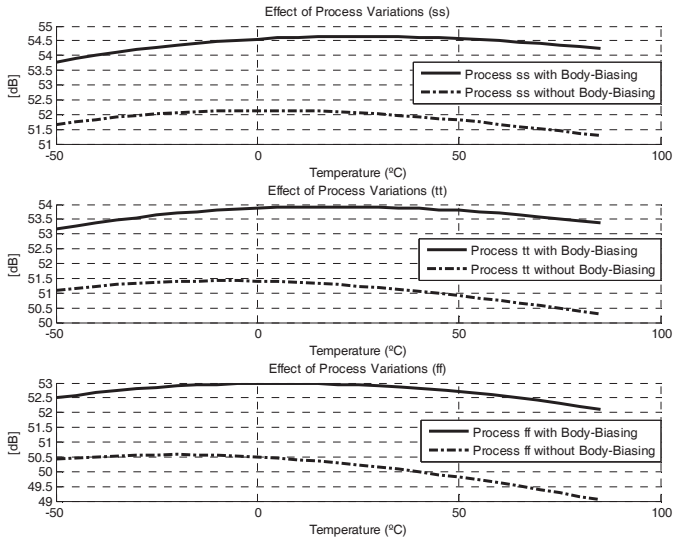

Figure 10. Overall gain variability with temperature & process variation for 65 nm (with and without body-biasing). [7]

Concerning process variation, Figs. 10 and 11 show that for the processes considered (ss, tt and ff), there is always an enhancement of the gain by about 3 dB. For most of the cases, the (DC) gain variability is below ± 0.5 dB (except for process ff, at 130 nm node technology, where the variability is higher than that without body-biasing).

This body-biasing circuitry requires only an extra current consumption of about 5% to 7% (for both technologies) of the total current consumption of the amplifier. This results in low power consumption, for both node technologies, from a 1.2 V supply.

V. Conclusions

This paper presented a simple circuit technique to reduce gain variability with temperature, supply, and process variations in cascode amplifiers using a body-biasing scheme, and at the same time, enhance the overall gain of the amplifier.

Simulation results of a standard telescopic-cascode amplifier, in two different nanoscale CMOS technologies (130 nm and 65 nm) have shown that it is possible to obtain process-supply-and-temperature-compensation.

The simulated DC gain has low variability (below ± 0.5 dB) while it is enhanced by 3 dB, over all PVT corners. This shows that higher gain can be obtained while also achieving lower gain variability.

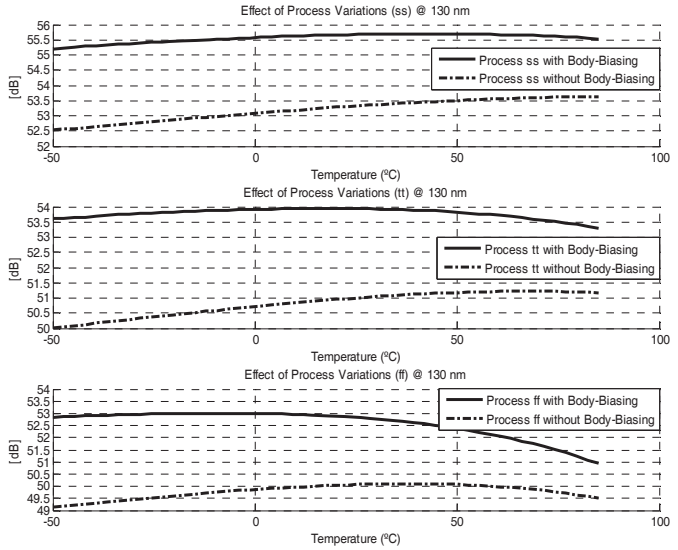

Figure 11. Overall gain variability with temperature & process variation for 130 nm (with and without body-biasing). [7]

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