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SIMULATION STUDIES OF HALF-BRIDGE ISOLATED DC/DC BOOST CONVERTER

In order to utilize energy from low voltage power source it is necessary to use isolated DC/DC boost converter which will provide desirable input voltage step-up. To obtain a high voltage gain it is necessary to apply a magnetic device with the relevant turns ratio to the converter structure. This can be coupled inductor or transformer. The great advantage of the transformer is galvanic isolation between the subsequent power levels. Unfortunately, the high values of voltage gain is accompanied by significant currents on the primary transformer side. Large DC input currents cause an increase in power losses as the transistor conduction losses are proportional to square of current. The solution to this problem would be to divide a large input current into smaller currents through applying balancing transformers in converter structure. The input current in one stage exactly matches the current in the parallel branch, therefore there is no need for additional control to guarantee current balancing between power stages. This technique, together with the use of transistors with a small drain-source resistance and output SiC (silicon carbide) Schottky diodes enables converter to achieve necessary output voltage. This paper presents PSpice simulation results and mathematical analysis of half-bridge isolated DC/DC boost converter. In presented circuit high voltage gain and high conversion efficiency were achieved.

KEYWORDS: Pspice simulation, boost converter, high voltage step-up, high efficiency

1. INTRODUCTION

Low DC voltage from current source should be stepped-up by DC/DC converter, transformed to AC and then connected to the grid. Thus, it is necessary to design a high step-up converter with a wide line regulation performance to interface low voltage current source to various loads. To achieve a high voltage gain, converters based on a transformer or coupled inductor have been developed [1–3]. Compared with a transformer-type converters, the ones with coupled inductors lack the electrical isolation. Separating the individual power levels isolated current-fed converters obtain not only a high voltage gain thanks to turns ratio, but also are galvanically isolated.

The main causes of energy loss in DC/DC converters are switching and conduction processes of semiconductor switches and the losses in magnetic

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components. Switching losses can be reduced by lowering operation frequency of the converter. As the conduction losses are depended on resistance of the transistor switches and currents that flow through all semiconductors they can be reduced by dividing of the currents (the conduction losses grow in current square) and by using low drain-source resistance ($R_{DS(on)}$) transistors.

The number of magnetic elements that affect the circuit volume can be reduced by using the current-fed half-bridge converter with two magnetic devices: balancing and isolation transformer. The proposed converter is characterized by high efficiency and high voltage gain thanks to balancing transformer which allow equitable distribution of input current among converter transistors.

The simulation model of the presented converter incorporates some properties and essential features of the magnetic components very often neglected in this type of research. As the input voltage is in the range of tens of volts, transistors with a low drain-source resistance can be applied to the structure. Models of power transistors and diodes used come from the manufacturer's websites [4, 5].

2. HALF-BRIDGE ISOLATED DC/DC BOOST CONVERTER TOPOLOGY

2.1. Electrical Scheme

Half-bridge isolated DC/DC boost converter with voltage doubler is depicted in Fig. 1a. High input current i_{in} is divided equally into two smaller currents. Balancing transformer T_1 shall further split currents flowing through the input inductor L_1. As a result both transistors (S_1,S_2) of the converter conduct only half the input current.

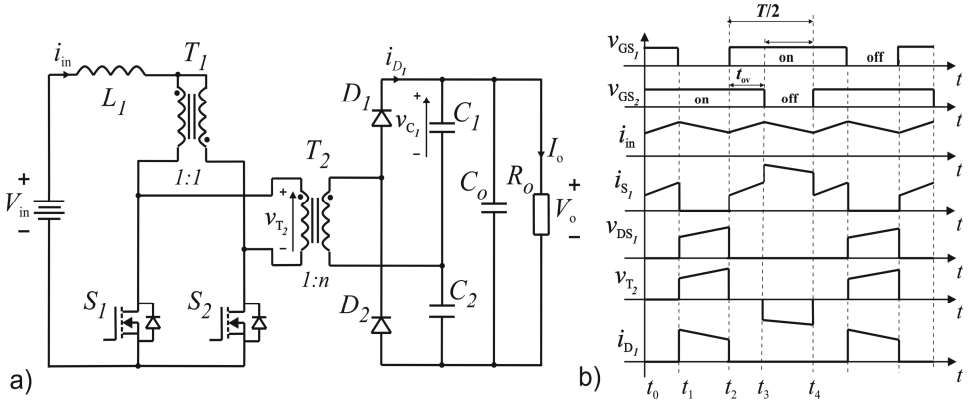

Fig. 1. a) Half-bridge isolated DC/DC boost converter, b) typical waveforms

Half-bridge boost converter forms first section of voltage step-up. Transformer T_2 assures galvanic isolation between two power stages as well as second voltage step-up stage (due to turns ratio n). The output diode rectifier (D_1,D_2) with capacitors (C_1,C_2) double rectified AC voltage of transformer T_2 secondary windings.

2.2. Principle of operation

The converter operation principle can be divided into several time intervals in which all transistors are driven at the same time or alternately (Fig. 1b). Duration of each operation mode depends on the duty cycle D.

(t_0-t_1) – transistors S_1 and S_2 are in the conducting state each of them conducts approximately half of the input current; input current i_{in} is rising, output diodes D_1 and D_2 are off;

(t_1) – transistors S_1 is turned off; transistors S_2 is in the conduction state, diode D_1 begins to conduct, input current i_{in} reaches maximum value;

(t_1-t_2) – transistor S_1 is turned off; S_2 is conducting, the input current i_{in} is falling, diode D_1 is conducting;

(t_2) – transistor S_2 is still conducting, transistor S_1 begin to conduct, input current i_{in} reaches minimum value, diode D_1 is turned off, transformer T_2 voltage drops to zero;

(t_2-t_3) – transistors S_1,S_2 are in conduction state, primary side of transformer voltage $T2$ is zero, input current i_{in} rises, diode D_1 and D_2 are off;

(t_3) – transistors S_2 is turned off; transistors S_1 is still conducting diode D_2 is turned on;

(t_3-t_4) – transistors S_1 conducts input current i_{in}, S_2 is turned off, diode D_2 is conducting, input current i_{in} is falling.

In order to calculate the voltage gain B, two variants of the sub-circuit with inductor L_1 should be considered in transistor conduction time intervals DT and $(T\text{-}DT)$.

$$\frac{V_{in}n}{L_1}DT = \frac{(V_{in} - \frac{v_{C_1}}{n})}{L_1}(T - DT) \tag{1}$$

Since the sum of the voltages on the two capacitors $C1$ and $C2$ is equal to the output voltage V_o :

$$V_{in}D = (V_{in} - \frac{V_o}{2n})(1 - D) \tag{2}$$

From the equation (2) we determine the dependence on the voltage gain in the converter.

$$B = \frac{V_o}{V_{in}} = \frac{2n}{(1 - D)} \tag{3}$$

Voltage V_{in} in series with L_1 act as DC current source. In step-up DC/DC converter value of the duty cycle has to be greater than 0.5. Assuming duty cycle of 0.51 the minimum voltage gain B_{min} in the converter is 8.16.

3. PSPICE SIMULATION MODEL OF HALF-BRIDGE ISOLATED DC/DC BOOST CONVERTER

Half-bridge isolated DC/DC converter model (Fig. 2) is supplied from constant DC source V_{in} = 40 V. Balancing transformer T1 provide equal distribution of input current. Transformer T2 is ensuring galvanic isolation. The transformers turns ratio is n = 1:2. Output AC voltage of the transformer is rectified by diode half-bridge. Voltage doubler output capacitors C_1 and C_2 (10 μF both) provide third stage of voltage step-up. Output filter capacitor is 50 μF. Output voltage V_o changes in function of load resistance R_o, duty cycle D and operation frequency f.

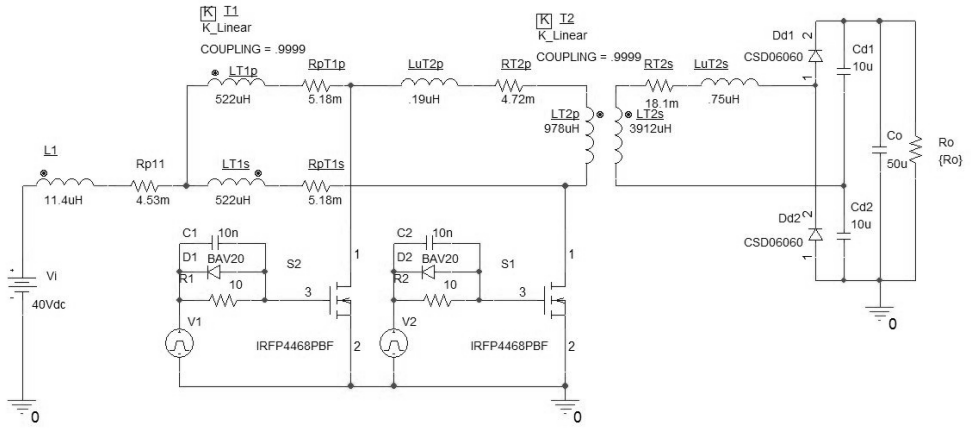

Fig. 2. Pspice model of DC-DC half-bridge converter

Optimal configuration for transistor gate driving was proposed in order to improve the quality of transistor switching. The BAV20 Schottky diode accelerate turning off of the transistor, 10nF capacitor and 10 Ω resistance all in parallel form the gate circuit at each transistor gate. The value of driving voltage was 20 V.

The converter half-bridge is realized on the low drain to source resistance MOSFET transistors - IRFP4468 ($R_{DS(on)}$ = 2.00 mΩ). As the energy losses increase in the current square they are expected to decrease with single mili-Ohms drain to source resistance. With this feature conduction losses of the transistors can be significantly reduced.

In output rectifier silicon carbide CSD06060 (SiC) Schottky diodes simulation models were used. The negligible reverse recovery current of this diodes

contributes to reduction of energy losses in the output half-bridge. Reverse recovery time declared by the manufacturer are less then 1ns for SiC diode and 18ns for Si (Silicon) diode for similar voltage/current rating.

In order to create possibly precise PSpice models of the balancing and isolation transformers were designed, made and examined. Listed below are specified parameters provided by the manufacturer.

The input inductor L_1 was located on the balancing transformer core, sharing the magnetic circuit. It ensures continuity of the current delivered to the load. Measured value of L_1 inductance and resistance for fixed frequency f = 20 kHz was equal 11.4 μH and 4.53 mΩ. Balancing transformers T_1 turns ratio *n* is 1:1.As it was made in planar technology it's leakage inductance was less than μ-Henry. Thus, considering the balancing transformer as two parallel inductors LT1p and LT1s connected in series with the input inductor L_1, we can neglect the leakage inductance. Parasitic parameters of the both sides will not differ. Measured values of windings resistances were equal 5.18 mΩ. Both primary (LT1p) and secondary (LT1s) windings inductances were 522 μH. Therefore leakage inductance of 0.21μH may not be included in the model. Isolation transformer T_2 (turns ratio 1:2) were also made in planar technology so its leakage inductances were significantly smaller than for similar power/turns ratio/frequency ratings transformers with no planar and interleaving techniques applied. Measured values of primary and secondary windings resistances (RT2p, RT2s) and inductances (LT2s, LT2p) were equal: 4.72 mΩ, 0.978 μH and 18.1 mΩ, 3912 μH respectively. Leakage inductances of transformer were equal 0.19 μH primary and .75 μH secondary respectively. Abovementioned parasitic parameters were included in transformers simulation models.

4. SIMULATION RESULTS

For fixed frequency 18 kHz ,duty cycle of D = 0.55 and load resistance R_o = 100 Ω switching transient waveforms are presented on Fig. 3. Switching nature of the transistor currents and voltages is associated with the control strategy.

As can be seen the waveform control signals are devoid of parasitic oscillations. Input inductance L1 provides continuous input current of satisfactory pulsation. The small oscillations of the current IS1 waveform are associated with the switching processes of transistor.Oscillations visible on the transistor S_1 drain to source voltage waveform are associated with loading of the entering conduction state transistors capacitance. As long as the current in the leakage inductance does not exceed ½ of the input current value its surplus charges capacitances of turn-off transistor to large dangerous voltage values. The oscillations are generated by the resonant circuit which consists of the isolation transformer leakage inductance and the transistor parasitic capacitance. This phenomenon is disadvantageous from two

factors. This causes a threat to the transistor whose maximum drain-source voltage can be exceeded. In addition, the oscillations increase the loss of transistor turn-off. Output diode D1 current oscillations are connected with its parasitic capacitances.

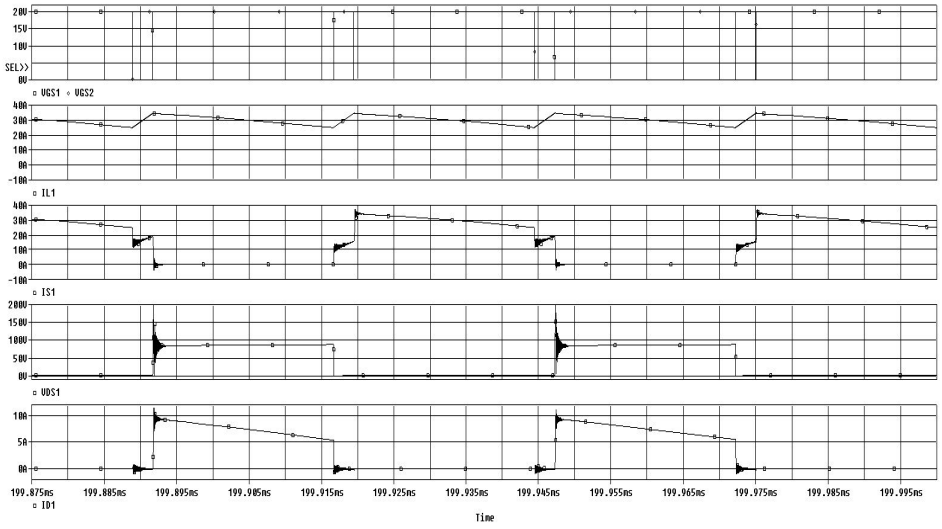

Fig. 3. Transient characteristics of half-bridge DC/DC boost converter; driving voltages of transistors VGS1,VGS2 ; transistor S1 current IDS1 ; transistor S1drain to source voltage VDS1 and output diode D1 current ID1

As can be seen in Figure 3, waveforms obtained as a result of simulation coincide with the theoretical ones. With increasing duty cycle the of time simultaneous conduction of both transistors would be lengthened which would led to increase in power processed in the circuit. The nature of parasitic oscillations would not change.

Electrical characteristics were plotted as a function of key parameters (efficiency η, voltage gain B and one of the transistors energy losses P_{S1}) of the converter as a function of the frequency for fixed output resistance $R_o = 100\ \Omega$ and frequency f = 18 kHz (Fig. 4.).The highest reported efficiency was 95.1% for duty cycle D = 0.60. Output voltages varied from 336 to 568 volts for 0.55÷0.75 duty cycle range, so that nearly 14 voltage gain could be achieved. Above D = 0.65 the converter efficiency rapidly decreases reaching 88.8 %. Characteristics of both converter parameters (B, P_{S1}) have increasing nature in function of duty cycle – the longer overshoot time of driving signals the greater amount of energy is accumulated in the input inductor L1 consequently greater is voltage step-up.

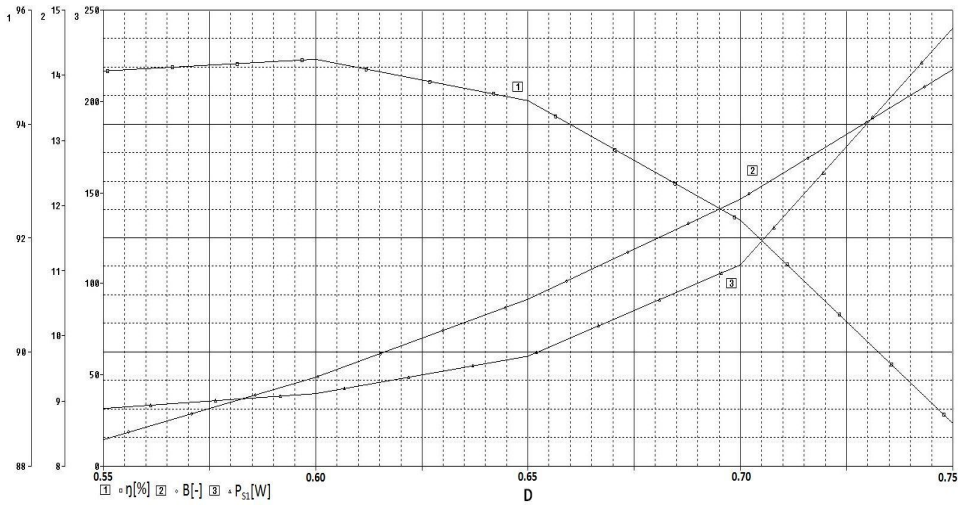

Fig. 4. Efficiency η, voltage gain B and transistor S_1 energy losses P_{S1} as a function of the duty cycle D for fixed output resistance $R_o = 100\ \Omega$ and frequency f = 18 kHz

Unfortunately for "hard switched" DC/DC boost converters high voltage step-up is connected with larger currents flowing trough transistors and increase in energy losses. Below 1.6 kW of output power, the transistor power losses does not exceeded 50 Watts what maintained efficiency above 94%. The simulation results confirmed the theoretical assumptions.

6. CONCLUSION

The presented model of the isolated half-bridge DC/DC converter has been subjected to a thorough analysis and simulation. Waveforms obtained confirmed the high efficiency and voltage gain for the value of the duty cycle not exceeding 0.75. The proper choice of semiconductor devices made possible to reduce the conduction losses of transistors and diodes turn-off losses. Application of planar magnetic with low leakage inductance lowered losses in this devices. Balancing transformer structure by splitting large input current, occurring in low voltage step-up DC/DC converters, reduced conduction losses of transistors.

Despite the hard switching of semiconductor devices circuit achieved maximum efficiency and voltage gain of the converter η = 95.1%, B = 14.1. It was not necessary to work with high duty cycle in order to achieve efficiency above 90% and voltage gain suitable for DC to AC conversion. Even small values (0.55) of duty cycle provided voltage above 330 V DC. Easily adaptable driving scheme and simple topology make proposed converter a good choice to apply in low DC input voltage applications.

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