INTL JOURNAL OF ELECTRONICS AND TELECOMMUNICATIONS, 2013, VOL. 59, NO. 2, PP. 161–167
Manuscript received March 4, 2013; revised May, 2013. DOI: 10.2478/eletel-2013-0019

The Impact of Noise and Mismatch on SAR ADCs and a Calibratable Capacitance Array Based Approach for High Resolutions

Jan Henning Mueller, Sebastian Strache, Laurens Busch, Ralf Wunderlich, and Stefan Heinen

***Abstract*—This paper describes widely used capacitor structures for charge-redistribution (CR) successive approximation register (SAR) based analog-to-digital converters (ADCs) and analyzes their linearity limitations due to kT/C noise, mismatch and parasitics. Results of mathematical considerations and statistical simulations are presented which show that most widespread dimensioning rules are overcritical. For high-resolution CR SAR ADCs in current CMOS technologies, matching of the capacitors, influenced by local mismatch and parasitics, is a limiting factor. For high-resolution medium-speed CR SAR ADCs, a novel capacitance array based approach using in-field calibration is proposed. This architecture promises a high resolution with small unit capacitances and without expensive factory calibration as laser trimming.**

***Keywords*—analog-digital conversion, analog-digital integrated circuits, calibration, CMOS integrated circuits, mathematical model, MATLAB, mixed analog digital integrated circuits, noise, numerical simulation, prediction methods**

I. Introduction

A. CR SAR ADC Principle

THE SAR ADC basic structure is shown in Fig. 1. A digital-to-analog converter (DAC) generated signal is compared to the analog input voltage. Using binary search algorithm, the generated signal is changed until the difference at the comparator inputs is below a certain threshold and the digital output word is determined. As the input voltage should be constant for the conversion time, a sample and hold (S&H) element is usually placed previous to the analog input.

The CR SAR ADC (CSA) principle has been published first in 1975 [1]. Figure 2 shows the basic single-ended structure. Here, the capacitors represent both the S&H element and the DAC. During the sampling phase, the upper plates of the capacitors are connected to GND by S_A and the input voltage is sampled via connection to the bottom plates. Then, S_A is opened and S_B is connected to V_{ref}. $S_{0...N}$ are connected to GND which forces the comparator negative input voltage to $-V_{in}$. By switching S_N...S_1, the DAC operation is performed.

B. Background and Recent Trends

CSAs are widely used for medium-resolution and medium-speed applications because of their simple structure and their low power consumption [2]. In the last years, an increasing number of papers about this topic has been published [3], proposing several approaches to reduce the power consumption of the capacitor recharging by use of other reference voltages, a fully- or semi-differential structure or an advanced switching scheme [4]–[6]. The split-capacitor (SC) named fragmentation of the most-significant bit (MSB) capacitor [7] significantly reduces the power dissipation for down transistions. Furthermore, a small overall capacitance decreases area and power consumption and increases speed. To reduce the overall capacitance of the ADC without reduction of the unity capacitance, one or more attenuation capacitors can be added in serial [8], but in [2] it was shown that this approach requires a larger unit capacitance resulting in an even higher overall area consumption. This assumption was confirmed by the simulations in [9]. Therefore, the most-promising approach seems to be a differential, conventional SC structure with a small unit capacitance, e. g. $0.5\,\mathrm{pF}$ as described in [10]. However, a small capacitance limits the linearity and the resolution of the ADC due to kT/C noise and mismatch, whereas mismatch means not only mismatch due to production accuracy but also due to parasitics.

C. Paper Structure

The paper is structured as follows. In Section II, the unit capacitor sizing limits are considered. The principle of a calibratable structure is introduced and its advantages are discussed. Finally, the mismatch and linearity simulations of the different concepts are explained and the simulation results are presented. In Section III, a hardware realization of a calibratable CSA and its calibration concept are proposed. Section IV gives an overview over the next development steps; the paper is concluded in Section V.

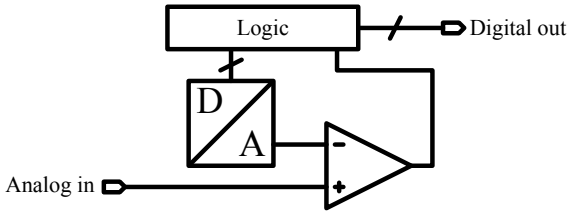

Fig. 1. Principle of SAR ADC.

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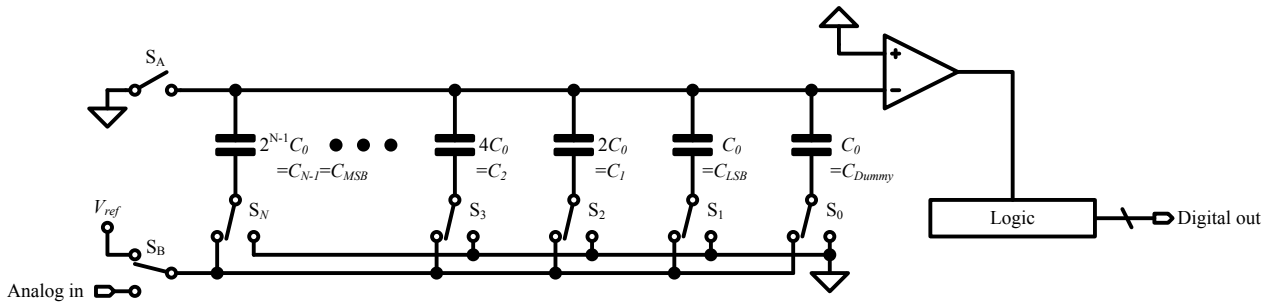


Fig. 2. CR SAR ADC.

II. Limitations to Unit Capacitor Sizing

The smaller the capacitance, the lower are area, power consumption and conversion time which makes small unit capacitor sizes desirable in general. Further, high resolution converters require large amounts of unit capacitors, so a small unit capacitor sizing only allows high resolutions on a reasonable area. But with higher resolutions, the voltage accuracy gets more critical, which also depends on the capacitance. Smaller capacitances lead to problems due to kT/C noise and mismatch.

A. kT/C Noise

kT/C noise is a special case of the thermal noise of a resistor given by

$$\overline{v^2} = 4 \cdot k \cdot T \cdot R \cdot \Delta f, \tag{1}$$

resulting from the capacitor and the parasitic resistances building a low pass filter. The resulting formula

$$\overline{v^2} = \frac{k \cdot T}{C} \tag{2}$$

is independend of the resistance. The kT/C noise is higher for smaller capacitances. This value has to be considered during the S&H phase. The corresponding capacitance is the overall capacitance

$$C = \sum_i C_i = 2^N \cdot C_0, \tag{3}$$

whereas the last term is only valid for a conventional structure without attenuation capacitor. The kT/C noise should be much smaller than the least-significant bit (LSB) voltage. Often, it is assumed that it should be at most half the value of V_{LSB}:

$$V_{LSB} = \frac{V_{ref}}{2^N} >> \sqrt{\overline{v^2}} = \frac{1}{2} \cdot \frac{V_{ref}}{2^N}, \tag{4}$$

which allows to give the achievable resolution N as a function of the unit capacitance C_0:

$$N\left(C_0\right) = 2 \cdot \mathrm{ld}\left(\frac{V_{ref}}{2} \cdot \sqrt{\frac{C_0}{k \cdot T}}\right). \tag{5}$$

This relation is shown in Fig. 3(a) which exposes that kT/C noise is not the limiting problem for a conventional CSA architecture. Assuming 0.5 fF unit capacitor size, the smallest unit capacitor size ever used in a CSA [10] to the knowledge of the authors, even with a low reference voltage such as 1 V the possible resolution was 11 bit, 3 bit more then targeted in the mentioned design.

B. Matching

Mismatch of the unity cells is caused by production process non-idealities such as varying capacitor size and dielectric thickness. The parasitics of the capacitors themselves and their wiring can also affect the capacitance of each unit capacitor. If a normal distribution is assumed, the capacitance standard variation σ_{C0} can be used to describe all these effects. It has to be considered that with increasing capacitance, usually this standard variation in relation to the capacitance decreases due to the law of area:

$$\frac{\sigma_C}{C} = \frac{A_C}{\sqrt{W \cdot L}}, \tag{6}$$

with A_C as technology specific constant. If parallel unit cells are used instead of larger capacitors, this equation also can be used because of the root-square addition of random variables. This is important for proper mismatch estimation of the larger capacitors in the CSA structure.

1) Worst-Case and Normal-Distribution Estimation: To get a relation between the standard variation σ_{C0} and the resulting nonlinearities, the most critical transistion point at MSB/2 has to be considered [11]. The relative capacitance mismatch error is

$$\left|\Delta C_x\right| = \left|C_{x,target} - C_{x,error}\right|. \tag{7}$$

For worst-case analysis [11] it is assumed, that the MSB capacitor is at maximum size while all other capacitors are at minimum size:

$$C_{N,error} = 2^{N-1}\left(C_0 + \left|\Delta C_0\right|\right) \text{ and} \tag{8}$$

$$C_{0\ldots N-1,error} = 2^{N-1}\left(C_0 - \left|\Delta C_0\right|\right). \tag{9}$$

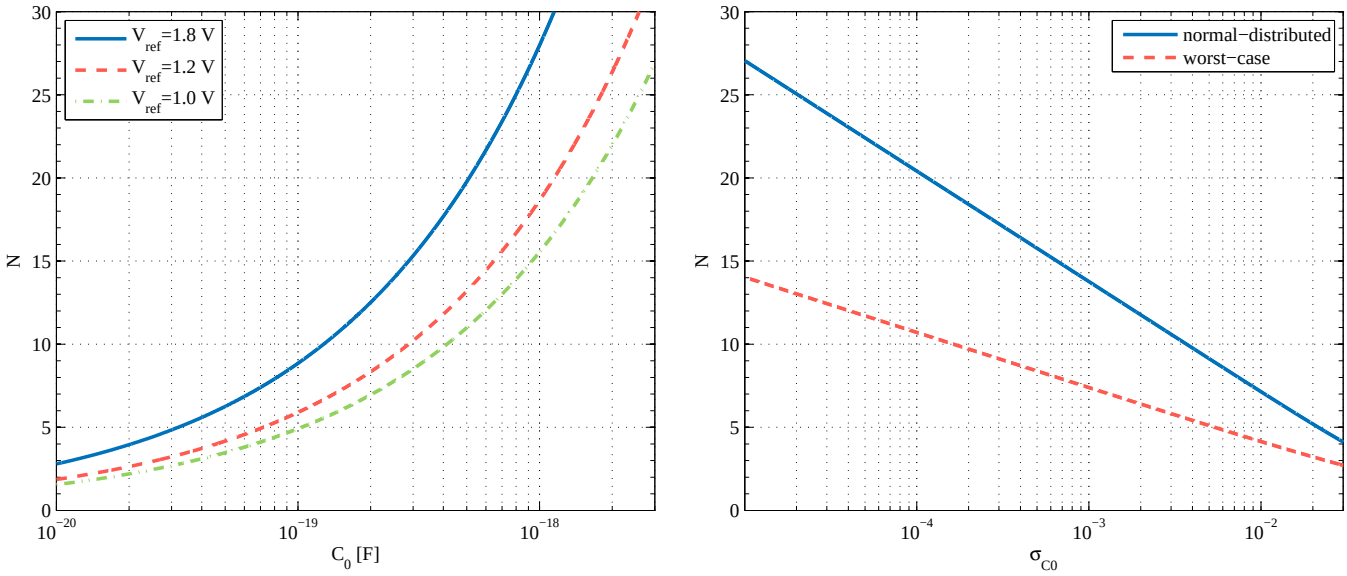
Demanding the differential non-linearity (DNL) to be $< \frac{1}{2}$ LSB, this equations lead to

$$\left|\Delta C_0\right| < \frac{C_0}{2^{N+1} - 2} \tag{10}$$

with e. g. the assumption $|\Delta C_0| = 3\sigma_{C0} \cdot C_0$. Simulations show, that this worst-case estimation is overcritical because it neglects the law of area (or the square-root addition of random variables, respectively). Respecting Eq. (6), Eq. (10) turns into

$$\left|\Delta C_0\right| < \frac{\sqrt{2^{N-1}}}{2^{N+1} - 2} \cdot C_0. \tag{11}$$

The simulations in [9] are also based on this approach. Fig. 3(b) shows the achievable resolution as a function of σ_{C0}



(a) Due to kT/C noise, $T = 300\,\mathrm{K}$.

(b) Due to mismatch with $|\Delta C_0| = 3\sigma_{C0} \cdot C_0$.

Fig. 3. Achievable resolution for conventional CSA architectures.

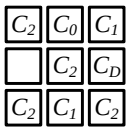


Fig. 4. Array structure of individually usable unit capacitor cells for a 3-bit CSA with elements C_{Dummy} and $C_0 \ldots C_2$ composed of unit cells. The blank cell is unused.

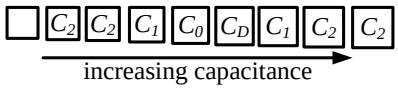


Fig. 5. Simple calibration algorithm.

following Eq. (10) and (11), which are slightly more severe in contrast to [9] because of the DNL approach.

Compared to current technology capabilities, for CSA designs with small unit capacitances, obviously matching becomes a problem even for medium resolutions.

2) Calibratable Architectures: To face this problem, laser trimmig can be used to adjust the capacitors. However, this post-production process is expensive and not suitable for co-integrated CSAs. Furthermore, variations during the product lifetime cannot be compensated. Therefore, this paper proposes a CSA structure which can be calibrated in field. This section only describes the model.

A CSA consists of the smallest capacitances C_0 and C_{Dummy}, and larger cells with binary multiples of those capacitances, e. g. $C_1 = 2 \cdot C_0$ (see Fig. 2). Now then, the proposed structure consists of an array of unit capacitor cells which can be individually connected during an initial calibration as shown in Fig. 4. A cell can be used as a single capacitor (as C_0 or C_{Dummy}), or bigger capacitances can be created connecting 2 or more cells in parallel. This allows to compose binary weighted capacitances (as in the conventional design). The assignment of the unit cells is not fixed and determined during calibration.

While C_0 and C_{Dummy} are represented by only 1 of the unit cells, $C_{1\ldots N-1}$ are represented by $2^{1\ldots N-1}$ unit cells. Overall, 2^N unit cells are needed for this purpose, even if there may be more available for calibration redundancy. Assuming that the capacitances of the unit cells are normally distributed, it will be shown that it is possible to compose nearly perfect conventional capacitances. Energy-minimizing techniques as SC are also possible because of the flexible unit cell usage.

3) Simulation: A MATLAB® simulation has been set up to test different calibration algorithms for the capacitor array design mentioned before and to compare the achievable performance with conventional designs. The simulation creates an array of normal distributed unit capacitances with the mean value C_0 and the standard deviation σ_{C0}. For simulations of a conventional design with the capacitors $C_{0\ldots N-1}$, the capacitance of C_n is calculated by adding randomly 2^n of these unity capacitances. For the calibratable structure, the capacitances are created using different calibration algorithms which try to select the optimum unit cells. A so-called *simple algorithm* sorts the unit capacitances in increasing order and combines the smaller capacitances with the larger to generate the capacitances consisting of more then 1 C_0. C_0 and C_{Dummy} are selected from the middle, where the capacitors with the smallest deviations are supposed to be located. The algorithm selection for a 3-bit CSA is illustrated in Fig. 5. An *advanced algorithm* uses a recursive sorting function to allow an improved selection. Both algorithms are only used to identify the limits of calibratable structures in general and not considered to be realized in hardware. A suitable hardware realization approach, which works as described in Section III-B, has also been implemented.

TABLE I
SIMULATION RESULTS FOR $\sigma_{C0} = 2\,\%$ AND $N = 10$, WORST CASE

Architecture	SNR [dB]	$ENOB$ [bit]	INL_{max} [LSB]	DNL_{max} [LSB]
Conventional	48.88	7.83	1.85	1.66
Attenuation Capacitor	36.31	5.74	6.23	11.10
Simple Calibration	60.36	9.73	0.35	0.35
Advanced Calibration	61.97	9.99	< 0.01	< 0.01
Hardware Calibration	61.87	9.98	0.08	0.11

TABLE II
SIMULATION RESULTS FOR $\sigma_{C0} = 2\,\%$ AND $N = 10$, TYPICAL CASE

Architecture	SNR [dB]	$ENOB$ [bit]	INL_{max} [LSB]	DNL_{max} [LSB]
Conventional	58.17	9.37	0.71	0.62
Attenuation Capacitor	47.71	7.63	2.53	2.71
Simple Calibration	61.79	9.97	0.09	0.09
Advanced Calibration	61.97	9.99	< 0.01	< 0.01
Hardware Calibration	61.95	9.99	0.04	0.04

Capacitors are created exemplarily for 10 bit CSAs, because based on experience, mismatch becomes an issue for 10 bit and higher resolutions, and higher resolutions increase the simulation time. But for higher resolutions the impact of mismatch is even worse and the design benefits even more from calibration approaches.

With the composed capacitances created in these manners, analog-to-digital conversions are simulated using the conventional SAR algorithm as described in Section I-A. The resulting performance values integral non-linearity (INL), DNL and signal-to-noise-ratio (SNR)/effective number of bits ($ENOB$) are obtained using a ramp as input voltage over time. Unfortunately, with this approach a very slow ramp (and so a lot of conversions) are needed to get precise results. To minimize simulation time, hence a combination of this numerical and an analytical approach has been used with only a medium number of comparisions. After every conversion, the closest comparision and thus the most critical conversion phase is determined, allowing to analytically find the critical voltage when the output word toggles. A comparision between known cases [11] shows that this algorithm works very accurately ($ENOB$, INL and DNL divergence $< 10^{-6}$). The Monte Carlo worst case and typical case simulation results are shown in Tab. I and II for 10-bit ADCs with $\sigma_{C0} = 2\,\%$. The calibration algorithms use a unit cell overhead of about $20\,\%$.

Results show, that even in typical case and for 10 bit the performance of CSAs can be significantly improved with calibratable capacitances. The worst case results for the conventional architecture comply very well to the results presented in [9]. Comparative simulations between conventional and attenuation capacitor structures with an equal overall capacitance (instead of equal unit capacitance) substantiate the conclusion of [2], that attenuation capacitor designs do not provide an area or power advantage over conventional designs.

The simulation does not only provide an estimation of the performance for a given architecture, unit capacitance and technology, but also allows suggestions which standard deviations and thereby unit capacitances are required for a desired resolution as Fig. 3(b). If e. g. INL and DNL are claimed to be < 0.5 LSB, simulations show that σ_{C0} has to be $< 0.48\,\%$ for the conventional structure, which complies very well to the analytical approach plotted in the mentioned graph. With the advanced calibration algorithm, nearly all mismatch errors can be removed. Nevertheless, also the hardware calibration can handle a σ_{C0} of up to $5.21\,\%$, that makes calibratable structures highly promising for high resolution CSA designs which use low-area unit capacitors.

III. REALIZATION OF CALIBRATABLE CR SAR ADC

In Section II-B2, a calibratable CSA model has been described. In this Section, a feasible hardware realization is proposed.

A. ADC Structure

A fully-differential calibratable CSA hardware approach is depicted in Fig. 6 and consists of 2 arrays with each $35 \times 35 = 1225$ capacitor unit cells (for a 10-bit CSA at least $2^{10} = 1024$ are required) which are described in Section III-A1. Further, there are a variable offset comparator (see Section III-A3) and a digital control logic. The arrays are controlled via vertical column lines (3 per column) and horizontal programming lines (1 per row). The column lines are controlled by column decoders as in random access memory (RAM) arrays. The top plates of the capacitor cells are connected to the comparator input (*Out+/−*), while the bottom plates can be connected to V_{CM}/V_{in} (common mode, CM) and to $V_{ref+,-}$ (to handle negative input voltages) or can be shorted to the top plates.

1) Capacitor Unit Cell: Figure 7 shows the implementation of a unit cell. The unit capacitor C_0 is shown in the bottom left corner. The lower port of the capacitor, which is actually the top plate in layout, is connected to the comparator as in a conventional design. This net is named *Out*. The upper port of the capacitor, actually the bottom plate in layout, can be connected to the connection lines shown on the right. The connections are established via the pass transistors M_{Px} acting as switches. The *Outline* shortes the capacitor (it is externally connected to *Out*). The reference line V_{ref} and the *Multiline* (connected to V_{in} or V_{CM}) act as the suitable connections for the capacitors, realizing the switches S_n in the conventional design (see Fig. 2). *Out* and the connection lines are unique for the whole array.

On the left side, the column lines are shown, whereas the programming line *Prog* is shown on top. The column lines are used to select the whole column for programming the unit cell with the *Prog* line. Therefore, one of the column lines is set to HIGH potential opening one of the column transistors M_{Cx}, allowing the *Prog* line to charge or discharge the parasitic capacitance C_{parx} which anon establishes or removes the connection of the attached pass transistor M_{Px}.

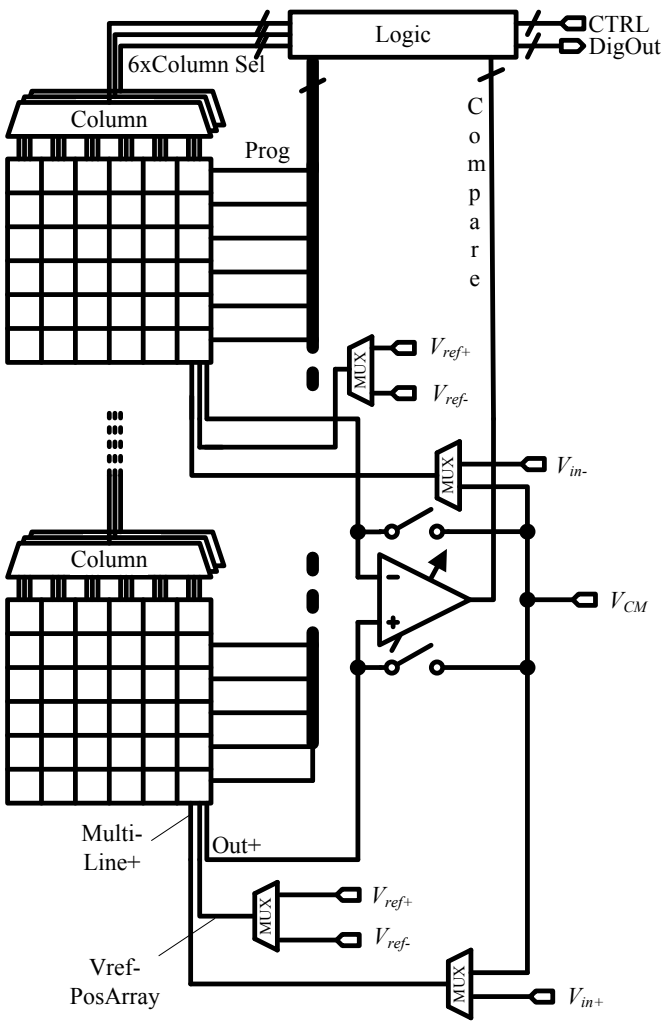


Fig. 6. Block diagram of a fully-differential calibratable array based CSA.

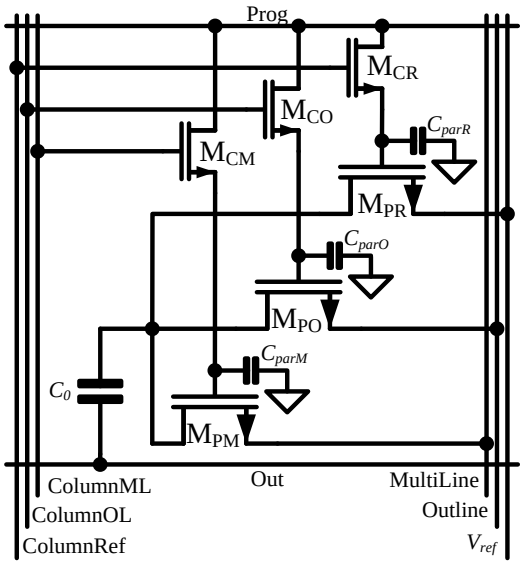


Fig. 7. Unit cell of the calibratable array based CSA.

With the grid of horizontal *Prog* lines and vertical column lines, the cells can be individually connected to V_{in}/V_{CM}, to V_{ref} or shorted. Although it is possible to open more then one pass transistor at the same time, this does not make sense for the normal operation.

All transistors can be regarded as transfer gates, which do not forward the full voltage from drain to source or vice versa, because the voltage is reduced by the threshold voltage. To overcome this voltage loss, the *Prog* lines and the column lines have to be driven with higher voltages than V_{ref} (known as bootstrapping). It is also important that the *Prog* high period overlaps the column line high period to avoid problems with a finite edge slope.

In the unit cell layout, the transistors and the lines are placed below a metal-insulator-metal (MIM) capacitor, so no area overhead is added.

2) Capacitor Array Operation: For the conversion operation, each used unit cell belongs to a capacitance $C_{Dummy,0\ldots N-1}$ as in a conventional approach, whereby e. g. C_{Dummy} and C_0 are represented by each only one unit cell and C_{N-1} by 2^{N-1} unit cells used in parallel. The unused unit cells are shorted by connection of *Out* with *Outline*. The employed unit cells can be connected either to $V_{in+,-}/V_{CM}$ (*Multiline*) or to $V_{ref+,-}$ as described before. The information which cells belong to which capacitance is saved in the digital control logic during calibration. This allows to run the ADC with the capacitor unit cells as a conventional CSA after an initial calibration.

In each conversion step (S&H, one step for sign detection and one step per bit form an analog-to-digital conversion) old connections (from the last step) are removed, and new connections are established. Therefore, each conversion step consists of 3 phases: *reset* phase, *set* phase and *comparator* phase. In the *reset* phase, now unused connections are removed, such as the V_{CM} connection of C_n for an up transistion. In the *set* phase, new connections are set, such as the required V_{ref} connections for the same up transistion. In the *comparator* phase, the comparator determines the current bit. In the *reset* and the *set* phase, the set of column lines of the connection, which has to be removed or established, strobe all corresponding columns from one side to the other, while the *Prog* lines reset or set the corresponding connections of the unit cells in the current column. The order of the *reset* and the *set* phase is important to avoid shorts, i. e. in the mentioned example in the *reset* phase the V_{CM} connections of the C_n cells are removed (the capacitors are floating for a moment), and the V_{ref} connections are established in the *set* phase, hence in the *reset* phase the *ColumnML* lines strobe, while the *ColumnRef* lines strobe in the *set* phase. This example is illustrated in Fig. 8 for a 2×2 array. The *ColumnOL* lines are not used during this conversion step, but for shortening the unused cells during S&H. For a down conversion, the order of the column line sets must be the other way round. Because there is no way of preserving the old connection, during the *reset* and *set* phases all connections are refreshed.

Because the strobe clock needs to be faster than the conversion step clock, this architecture is only suitable for low and medium speed CSAs. For 35 rows as in the proposed design,

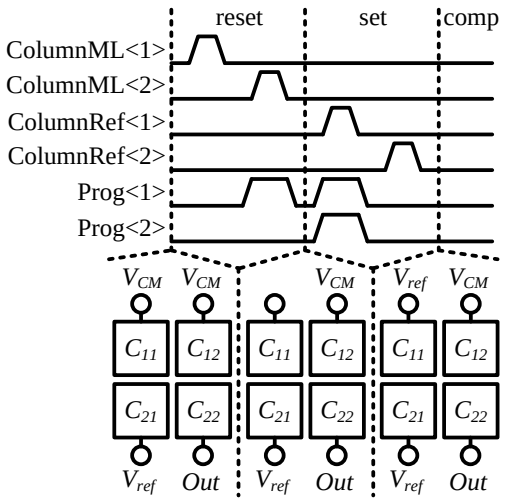


Fig. 8. Example programming of a 2×2 array for an up transistion: the C_{11} connection is changed from V_{CM} to V_{ref}, C_{12} stays connected to V_{CM} and C_{21} to V_{ref}, C_{22} is unused.

the clock strobes 35 times per phase.

3) Variable Offset Comparator: The variable offset comparator acts as a normal comparator (indicate which input is at higher voltage), when the variable offset is set to 0. During ADC operation, the comparator always works as a normal comparator. The comparator inputs can also be connected to V_{CM}.

For calibration, it is possible to vary the comparator input offset a little bit (about a few hundreds of µV). This can be done by connecting capacitors to one output node as an asymmetric load. If two voltages are compared, the comparator outputs HIGH potential if the positive input voltage is higher than the negative input voltage. If the difference is large enough, this output is always the same, independent of a small comparator input offset. But if the input voltages are close to each other, e. g. if the positive voltage is only a few hundreds of µV higher than the negative input voltage, the comparator output will toggle if a negative offset is applied and vice versa. In this way it is not only possible to determine which voltage is higher as with a normal comparator, but also if the input voltages are close to each other. For calibration, at first the input is compared with a positive offset and then with a negative offset. If the comparator toggles, the voltage difference is in a small window.

B. Calibration

The calibration of CSAs is nontrivial because of the limited accuracy of the comparator. If a conventional CSA is calibrated, the comparator needs to detect voltage differences which are much smaller than in normal operation, since the mismatch of the small capacitors leads only to small voltage changes at the middle of the capacitive divider which is connected to the comparator input. In this design, this problem can be avoided by shortening the other capacitors, hence only the current calibrated capacitors form the capacitive divider.

The calibration can be executed directly before conversion operation. Therefore, well-matching binary capacitances as in a conventional CSA have to be found. This is done using a capacitive voltage divider between V_{ref+} and V_{ref-} with 2 groups of 1 or more capacitor cells, C_{upper} and C_{lower}, as shown in Fig. 9. The divided voltage is compared to V_{CM} using the window technique described in Section III-A3. If the voltage is within the window, the upper and lower capacitances match each other well.

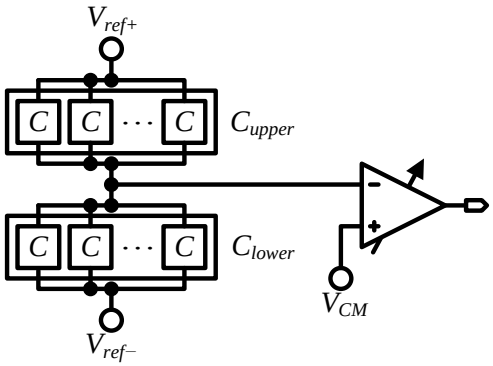


Fig. 9. Capacitive divider for calibration.

For calibration, at first C_{Dummy} is selected randomly and used as C_{upper}. Then, the logic seeks a cell with a good matching by selecting different cells for C_{lower}, one after the other using trial and error. If a good matching cell is found, it is assigned to C_0. Then, it is connected in parallel to the C_{Dummy} cell and the logic seeks for two cells which match well to $C_{upper} = C_{Dummy} + C_0$ and are then assigned to C_1. This algorithm continues until all capacitances up to C_{N-1} have been composed. For the proposed fully-differential design, this calibration has to be done for both capacitor arrays one after the other.

The proposed design uses an SC approach. Instead of one C_{N-1} capacitance group, binary single-controllable capacitances $C_{SC\_0} = C_0 \ldots C_{SC\_N-2} = C_{N-2}$ are required. Therefore, not only 1 matching capacitance group for C_{lower} is found for each capacitance C_{upper}, but 2. Together these capacitance groups C_{CS_x} form the MSB capacitance.

The calibration technique has also been implemented in the simulation described in Section II-B3.

IV. Outlook

A proof-of-concept prototype of the proposed structure with 100 kS/s sample rate has been designed and is currently still in fabrication due to fab problems. The prototype uses a common-centroid non-calibrated capacitance composition to test ADC operation only, and can also be calibrated as described in Section III-B. This will allow to evaluate the benefits of the calibration. The chip is expected for I/2013.

For an efficient and area- and power-competitive hardware realization, it is required to reduce the number of free configurable unit cells in order to reduce circuit complexity and the required clock speed, thus some capacitors must be hard-wired. The simulation has to be adapted finding the optimum number of free-configurable unit cells, representing a trade-off between accuracy and efficiency. It may also be

possible to use a modified unit cell design, e. g. with additional control lines which allow to select a whole column to simplify programming effort.

Additional to the proposed architecture, conventional CSA architectures employing trim capacitors for calibration are currently evaluated. This means that the calibration is not performed by selecting capacitors but connecting small capacitors in parallel to a bigger hard-wired capacitor. Especially for the higher capacitances, this approach may be more efficient then capacitor selection and allows also a more purposful calibration.

V. Conclusion

It has been shown that kT/C noise does not constitute a problem to conventional CSAs, but matching is a resolution limiting factor for a small C_0. An in-field calibration approach has been proposed which relaxes the matching reqirements by more then a factor of 10. Thereby, either the required area for the ADC can be minimized or the achievable resolution can be increased. The possible hardware realization has been proposed. Due to the higher CMOS integration in the future the design will even become more interesting.

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