Development of the NMOS-based THz Detectors and the Readout Systems for THz Spectroscopy and Imaging

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***Abstract*—This paper summarizes the work performed within the Polish applied research project THzOnLine aiming at multi-pixel THz detectors based on selective NMOS transistors and its application in biology, medicine and security systems, completed in 2016. It starts with presentation of techniques applied for increasing the efficiency of THz detectors, i.e. used to maximize the output voltage yielded from NMOS-based detecting devices when exposed to a THz radiation. In the second part of this work the authors focuse on issues related to development of the readout electronics for these devices, as well as present the collection of integrated circuits and two complete measurement systems constructed by them.**

***Index Terms*—NMOS-based THz detectors, readout system**

I. Introduction

THE terahertz range of electromagnetic spectrum, for many years referred as the last unexplored band, is increasingly gaining much attention for over the last decade. It is due to the fact, that terahertz waves can be utilized in many applications ranging from ultra-fast communication systems - because of the very high frequency of the carrier signal, to imaging and spectroscopy. The terahertz spectroscopy seems to be very promising technology from the security systems point of view for the following reasons: Firstly, many materials have characteristic fingerprint in this range - the low energy of THz radiation corresponds well with weak bonds and bending or rotational modes of molecules. Many explosives, like RDX, TNT, HMX, etc. have absorption peaks in (sub)THz band [1]–[4]. This gives an opportunity to detect many types of substances and to identify them. Secondly, many textile or wrapping materials used nowadays are transparent for THz radiation. At last, the low energy of THz radiation and its non-ionizing character makes it harmless for human beings. The factors mentioned above allowed people to think about the security scanners targeted for detection of hidden explosives, to be utilized in places like airports, as well as about the equipment allowing to detect the forbidden materials (e.g. drugs) in a paper mail. Measurements of biological samples (animal and human origin) preformed within this project confirmed that the dominant problem are the slightest traces of water. Moreover, most of the substances of biological origin does not show any characteristic spectrum below 1THz. Attempts are carried out to measure the samples dehydrated using various methods and at low temperatures (frozen) [5].

Two groups of activities were carried out in described project to develop the cost-effective solutions for the equipment dedicated to THz spectroscopy. First of them was related to optimization of design and manufacturing technology of the NMOS-based THz detectors, while the second one was dedicated to development of its readout electronics able to replace the typical expensive lock-in hardware used in laboratory experiments.

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II. THz Detector Development

The NMOS field effect transistors are considered as the most cost-effective elements utilized for THz detection at room temperature. The detection process is carried out in the non-linear region of the transistor channel, even though the operating frequency of mentioned device is several orders of magnitude lower than THz radiation frequency. There are two theories known, interpreting the mechanism of THz detection. First of them was published in 1996 [6] and is related to excitation of plasma waves in 2DEG of transistor channel. The second one is distributed resistive self-mixing theory [7], being a derivative of the resistive mixing model, assuming that the non-zero DC component appears on drain electrode of the FET while its gate and drain potential are simultaneously modulated by the AC signal.

In typical construction of THz detectors the receiving antenna is connected in-between the gate and source terminals, while the non-biased drain electrode is treated as DC signal output. The gate terminal is also used to provide the proper bias of the transistor, as the maximum photovoltaic signal at the output is yielded always when the device is in sub-threshold region, as shown in Figure 1. In this chart the photoresponse of several relatively small FETs (L = 3μm, W = 6μm) integrated with a patch antenna and fabricated on different substrates is shown. For sake of comparison one of the FETs (broken line) is bigger. Essentially, even if the FETs are electrically very reproducible, their THz detectivity may differ substantially. As a basic rule, however, it may be

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concluded that if the FETs are processed within the same lot on a similar substrate, their detectivity increases with decreasing size of the transistor. This may be linked with a growing role of parasitic elements of the transistor decoupling its channel from the antenna.

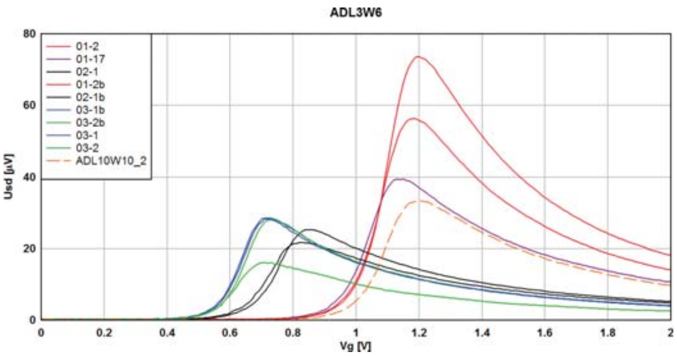

Fig. 1. The NMOS THz detector output signal vs. gate bias. Measurements performed in laboratory of the Institute of Optoelectronics of the Military University of Technology in Warsaw (IOE WAT) with VDI, Inc. terahertz source.

There were several studies performed to explore the ways of increasing the efficiency of NMOS-based THz detectors [8], [9]. One of them is related to the propagation of THz waves within the structure of IC substrate. Such a structure of silicon substrate can be treated as a dielectric waveguide allowing propagation of TE or TM waveguide modes for waves of THz frequencies. As it was proven in [8], [10] the thicker the dielectric structure (i.e. substrate) is, the bigger amount of energy is trapped there. For typical substrates (approx $400\mu m$ for 4' wafers) utilized in silicon technology, the dominating part of energy is propagated in the substrate structure, what significantly limits its reception by a receiving antenna. The remedy for this problem can be grinding of the final chip to achieve significantly lower thickness, so that the power lost to the substrate modes is minimized.

Another way to overcome the problem, is local backside etching of the substrate, to form a kind of cavity beneath the detector and antenna structure, so that the thickness of resulting substrate is less than $40\mu m$ (300GHz band). This option, not available in commercial silicon manufacturing technologies, was introduced into the modified version of the ITE proprietary CMOS process ($3\mu m$) [11]. Figure 2 shows the backside of the wafer after completion of the cavities etching process.

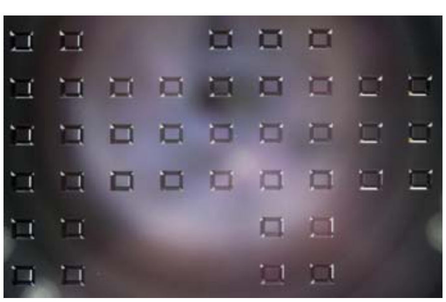

Fig. 2. Backside of the silicon wafer after cavities etching.

The responsivity curves of detectors manufactured on the SOI wafers with high resistive handle wafer, with local backside etching to $40\mu m$ are reproduced in Figure 3.

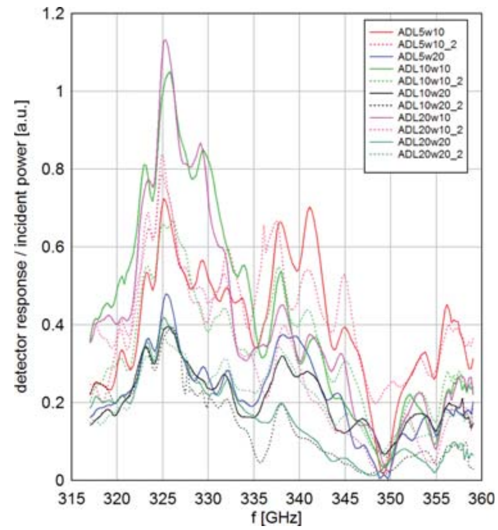

Fig. 3. The responsivity of THz detectors fitted with patch antenna. The indices denote channel length and width of detecting MOSFETs, the third index (if present) denotes the second copy of device under measurements. Measurements performed in IOE-WAT.

The alternative concept in respect to the local thinning of the substrate was to build a new form of antenna elevated above the silicon structure and separated from it by means of metal ground plane [12]. The layer of the SU-8 photoresist was used to form the pedestal - mechanical support for the antenna shape made of the second metalization layer. The thickness of the SU-8 was kept small to avoid propagation of substrate modes. The first metalization layer is deployed to shield the antenna from silicon substrate, as well as to provide the connections to the detecting NMOSFET. Direct contacting with antenna elements made of the second metalization layer deposited on the SU-8 photoresist would require extremely long vias to be manufactured, what in turn would negatively impact the responsivity of device. Instead, the coplanar lines and dedicated capacitive coupler are used to provide the connection between detecting MOSFET and antenna. The responsivity curves measured for detectors with different channel dimensions fitted with antenna manufactured on the SU-8 layer with $20\mu m$ and $50\mu m$ thickness are presented in Figure 4.

The comparison of measurement results collected above shows that the local backside etching technique allows to yield better detector responsivity than the construction of antenna deposited on SU-8 layer. This is probably due to the influence of parasitic devices onto the matching of detecting transistor and antenna [9]. In our experiments, three types of substrates were taken into account. Namely low- and high-resistive bulk substrates and SOI substrates with a high resistive handle wafer. The high-resistive substrates have the advantage that they could be illuminated by integrated lens from the bottom. The bulk low-resistive wafers were similar to those used in MPW services. Detectors illuminated from the top required thin substrates beneath their antennas to avoid aforementioned substrate modes (resulting in significant losses). It turned out,

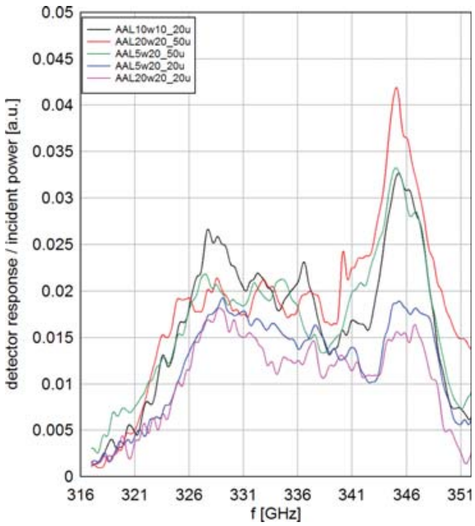

Fig. 4. The responsivity of THz detectors fitted with antenna manufactured on the SU-8 layer of two thicknesses: 20 and $50 \mu m$. The indices denote channel length and width of detecting MOSFETs, the third index denotes the SU-8 thickness. Measurements performed in IOE-WAT.

moreover, that even a very thin detector manufactured with use of low-resistive wafers gave a low response. The best detectors proved to be produced on high resistive bulk and SOI substrates. Comparing the responsivities of THz detectors of the same type, built of MOSFETS with different channel dimensions one can note, that the output response on the THz signal is inversely proportional to the width of a detecting transistor. It can be assumed, that this effect is related to the parasitic capacitance between the source area (implantation region) and the gate [13]. It can be avoided by moving the S-B junction away from the MOSFET channel, however this is possible only in device operating in depletion mode, instead of more common enhancement one. Otherwise, the region between S-B junction and the transistor channel, uncontrolled by gate potential would stop the current flow between source and drain electrodes. Proposed change, development of depletion mode transistors with separation between source region and channel area, was introduced in modified version of ITE proprietary silicon process.

In the scope of research on increasing the detector responsivity some experiments involving the integrated THz optics were also performed. In such an approach the incident THz beam is concentrated (focused) on a detecting transistor and antenna by the silicon lens attached to the backside of the detector wafer. Contrary to the previously discussed approach the silicon wafer before integration with a lens is neither entirely nor selectively thinned down, but it has to be deprived of the backside metalization. Construction of measurement setup required a specific detector-to-lens-alignment procedure and dedicated assembly technique to be developed.

The results of measurements, presented in Figure 5 confirmed the effectiveness of applied approach. The lack of selectivity observed for the detector integrated with silicon lens is an effect of the wide-band characteristic of the logarithmic-periodic antenna, shown in Figure 6 which is typically deployed for illumination with a focused THz beam. This can be overcome by utilization of filters.

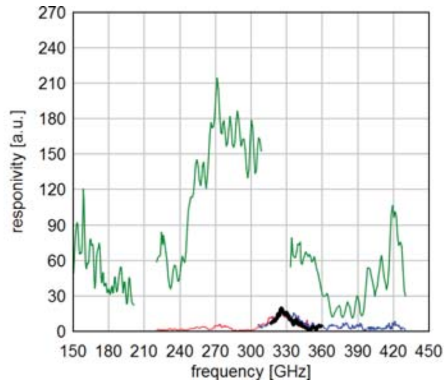

Fig. 5. The responsivity vs. frequency for THz detector integrated with silicon lens (green) and ones fitted with patch-type antenna. Measurements performed at IOE-WAT.

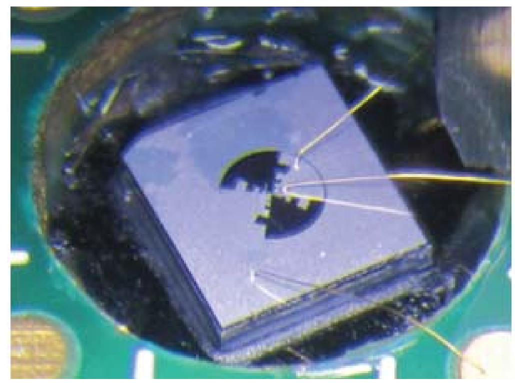

Fig. 6. Details of logarithmic-periodic antenna on-chip integrated with detecting NMOS, assembled on silicon lens.

Measurements as a function of frequency (Figs. 3, 4) show, in addition to the impact of antenna, numerous extremes. They are mainly related to interferences in the measurement optical setup and the detector itself (including bonds, package, etc.). This behavior is difficult to avoid since THz wavelength is comparable with size of components. To prevent signals outside the frequency to which the antenna is designed, it is planned to use filters in the form of a periodic structure made of a metal foil [14]. Such a filter has been already designed and tested.

III. Readout System Development

The essential issues in registering and recording the response of NMOS-based THz detectors come from the parameters of this output signal. The small voltage generated over the relatively high output resistance of a MOSFET device operating in the sub-threshold region requires the high gain and high input impedance of the readout circuit, while the DC nature of this response makes it necessary to pay the special attention to the 1/f noise components, as the most important while processing the low frequency signals. Moreover, special emphasis must be placed to minimize the reception of external interferences.

For a very long time, one of the commonly used methods for very low DC signal measurement is Phase Sensitive Detection

(PSD). Generally, in this technique the useful signal is extracted from the background noise by its modulation with some reference frequency and phase. Then, all remaining signals are filtered out (except one with mentioned reference frequency). With undisputed advantages of PSD, this technique is also limited by some fundamental restrictions. First - performing measurement is relatively slow. Second - there are THz sources that cannot be easily modulated. Third - the PSD method usually implicates single-channel architecture of the signal path. And fourth - phase sensitive detection requires constant link - synchronization, between the modulated signal source and the measurement circuit - selective amplifier. The fundamental aim of designing new readout circuit targeted for NMOS-based THz detectors was to replace the PSD equipment with dedicated electronic system, offering comparable parameters, but without necessity of modulating the THz wave. From the beginning it was intended to develop the most important part of this system in a form of an application specific integrated circuit (ASIC).

A. Chopper Amplifier Architecture

The architecture of all ASICs designed within the project is based on the chopper amplifier concept, schematically illustrated in Figure 7.

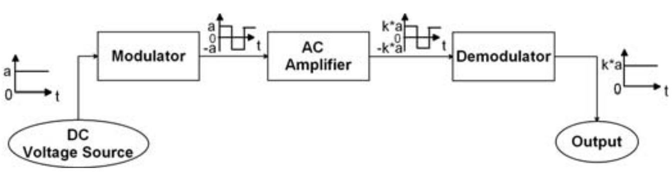

Fig. 7. The concept of applied chopper amplifier architecture.

Low DC voltage signal from a detector is modulated and converted to the square wave by the input circuit called a modulator. Then the next block provides amplification of the AC component of the modulated signal. Finally, circuit called a demodulator converts this amplified square wave again to the DC signal. One can notice, that the essential idea behind this circuit is to convert the small DC signal into its AC counterpart, amplify it with an AC amplifier, avoiding problems with DC offset and 1/f noise component, and final to rectify it to obtain the DC output.

B. Single Channel Integrated Readout Circuit

The development of the readout IC started with the simple chopper amplifier circuit implemented in ITE proprietary silicon process ($3\mu m$). It consisted of 3 main components: modulator, amplifier and demodulator. The first one was just a simple switching circuit, composed of four CMOS switches which were turning on/off alternately. This operation produced a square wave with an amplitude equal to one of the input DC voltage. The second block was an instrumentation amplifier of 40dB gain. At the end of the signal path the demodulator block (amplifier + sample&hold circuit) was placed providing 40dB gain and the second signal conversion (this time from square wave to DC voltage).

Figure 8 shows schematic and layout views of designed structure. The concept of readout circuit implemented in the same silicon technology as the THz detector was very promising in the context of sensors and electronics integration (i.e. in imaging and spectroscopy arrays etc.).

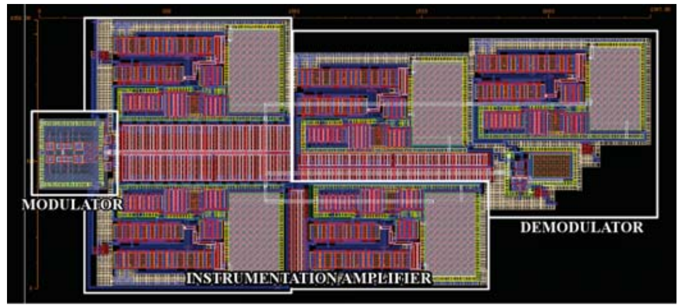

Fig. 8. First version of the readout IC - ITE silicon process ($3\mu m$).

The next step in the readout circuit design consisted in IC implementation and fabrication in standard AMS C35 process (350nm feature size) available by Europractice MPW Service. In comparison to the first circuit described above, chopper amplifier architecture has been improved by modification of the instrumentation amplifier structure. In general, three different versions of the readout circuit have been designed - they differed with respect to some minor functionalities (linear gain control, common mode voltage regulation etc.). Taking into account the significant ($7mm^2$) minimum payable chip area in AMS C35 process it was decided to add into the structure sent for manufacturing a detecting transistor equipped with dedicated antenna and connected to one of the readout circuits. The layout of designed structure is presented in Figure 9.

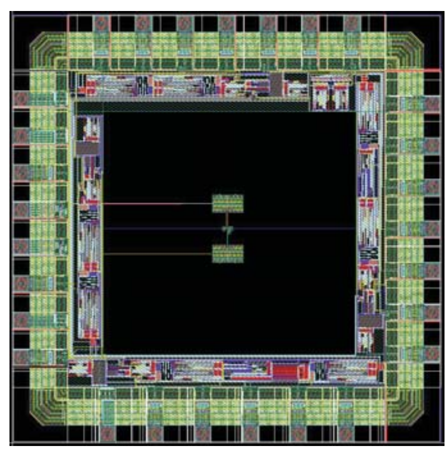

Fig. 9. Layout of the first readout IC implemented in AMS C35 process (detector and THz antenna placed in the middle of the structure).

The chip was fabricated and comprehensively measured using dedicated test setups. The entire design process, simulations and measurement results have been described in detail in [15]. Most of the achieved results matched the simulation predictions, but the demodulator circuit had a tendency to oscillate under some specific conditions. The proper circuit operation in test setups was achieved by addition of the PCB-level voltage followers, but this issue had to be addressed in the next version of the IC.

One of the most important results achieved during the measurements was confirmation of the proper operation of the designed readout IC with NMOS-based THz detector. However, it has been decided that the bandwidth of used amplifier must be limited to reach further improvement of the output noise parameters.

The conclusions mentioned above let the authors to design and fabrication of the second chip in AMS C35 process. In this readout IC the sample&hold circuit, formerly deployed as a demodulator, was replaced by a switching circuit, similar to the modulator, and a low-pass filter. The architecture of the AC amplifier has also been completely changed and in this version it was based on Gm-C filters which ensures significant bandwidth limitation. The chopping (switching) frequency was increased to 200kHz (previously 1kHz). Simplified architecture of this circuit and its layout implementation are presented in Figure 10.

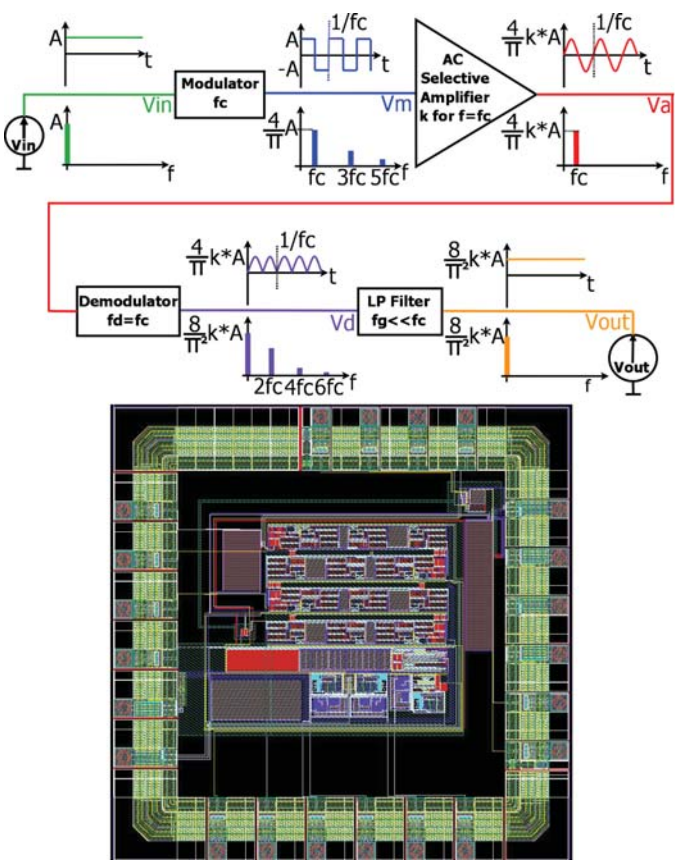

Fig. 10. Architecture and layout of the second readout IC implemented in AMS C35 process.

The design, simulations and measurements of the second AMS chip have been described in [16]. The measurements results matched almost perfectly the simulations and confirmed proper operation of designed chopper amplifier - in both test setups used for electrical characterization and target (THz) application. The output noise has been significantly reduced which proved the advisability of the AC amplifier bandwidth limitation. Input referred noise spectrum density has been evaluated as constant $20\frac{nV}{\sqrt{Hz}}$ for (0-3.8kHz) frequency range.

C. Multi-channel Integrated Readout Circuit

The positively verified architecture of the single-channel readout circuit based on selective chopper amplifier concept was chosen as a basis for design of its multi-channel extension.

This multi-channel IC is equipped with eight independent input gain stages - each based on the same bandpass Gm-C structure. Just after these blocks, the channel switching (multiplexing) is introduced and the next stages of the signal path are common for all channels. Unlike in single-channel circuit, each channel is fitted with a differential input pair: one pin connected to detecting FET, while the second can be driven by offset compensation network. This feature is intended for implementation of the autocalibration procedure allowing for automated compensation of the input offset voltage.

Figure 11 (next page) presents simplified architecture of designed multi-channel readout IC. More details about its functionality and main components can be found in [17].

This multi-channel IC, like the previous ones, was fabricated in AMS C35 and comprehensively measured using dedicated test setup. Figure 12 shows layout view of the designed structure while the exemplary measurement results - the input noise density curves are presented in Figure 13. This results proves the main advantage of this chopper amplifier readout IC - significant reduction of the 1/f noise component.

D. The First Readout System

The fundamental aim of the studies on readout circuits development, presented is subsections above, was to build the complete system supporting NMOS-based THz detectors, able to successfully replace the PSD (lock-in) equipment while providing comparable parameters. Since the beginning it was planned to extend the functionality into multi-channel architecture and to build the standalone measurement system based on designed integrated circuits. The first prototype of such a system has been designed basing on nine previously fabricated single-channel ICs and several off-the-shelf components, like operational amplifiers, octal multiplexers and passives.

The measurement unit contains the essential part of measurement system - detecting pixel line and analog front-end electronics with DACs and is intended to be placed into the THz optical setup. The most important parts of the measurement unit are nine single-channel readout ICs, assembled using chip-on-board technique and covered within common shield. Eight of them are deployed as selective entrant part of each channel - modulator and first gain stage, while the latter one is used as the second gain stage and the demodulator.

Monolithic detector lines are assembled on separate, removable PCBs. This allows the system to be easily adapted towards needs of performed experiments by simple replacement of arbitrarily chosen set of detectors.

The second component of the system - a control unit - supervises the operation of measurement unit, controls the analog signal by means of built-in DACs and gather and presents actual output data. The user interface is provided by two-lines character LCD and a keypad, allowing to influence the operation of embedded measurement program. The heart of control unit is 8-bits ATMega32 MCU (Atmel). The control

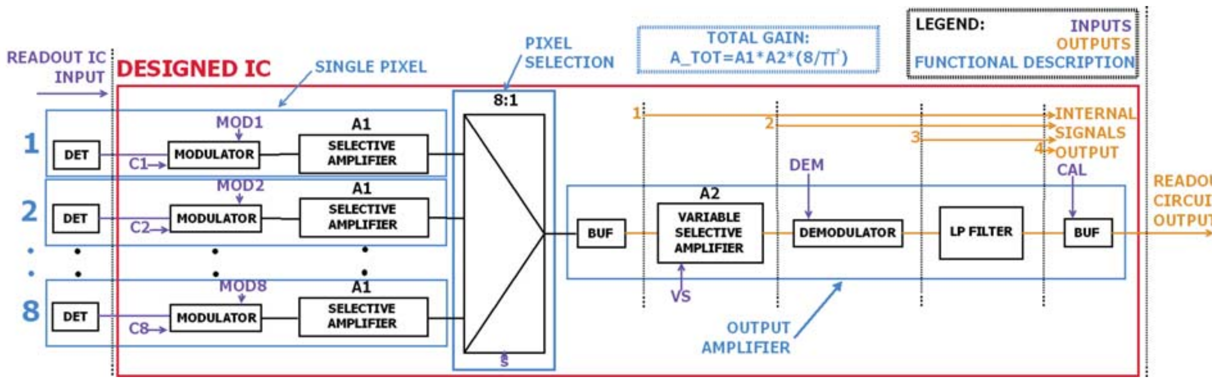

Fig. 11. Overall view of designed multichannel IC.

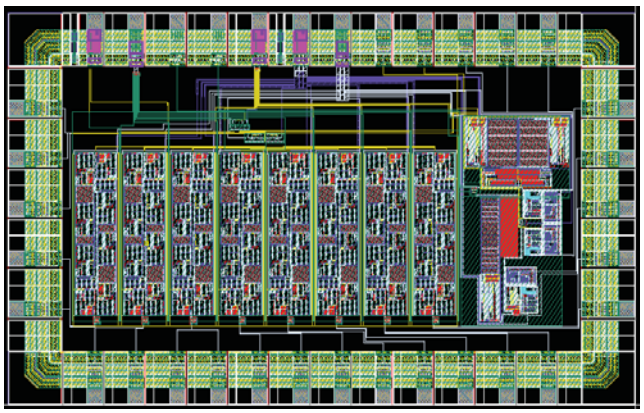

Fig. 12. Layout of the multi channel readout IC and exemplary measurement results presenting the noise input spectral density for chosen channel (with shorted input, 100kΩ and 200kΩ connected to the inputs).

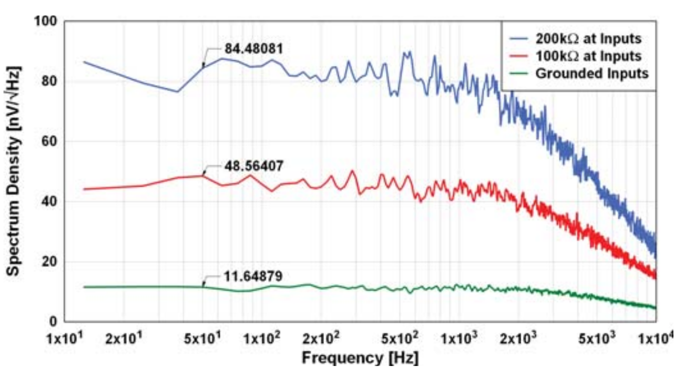

Fig. 13. The exemplary measurement results presenting the noise input spectral density for chosen channel (with shorted input, 100kΩ and 200kΩ connected to the inputs).

unit can be also used as an interface between PC running application developed for use with NI LabVIEW^{TM} and measurement unit.

The measurements performed in the laboratory of the Institute of Optoelectronics of the Military University of Technology proved that designed system can be successfully used as a replacement of standard lock-in equipment, moreover it offers the multi-channel functionality addressing the 8-elements pixel line.

Figure 14 presents results obtained in the automated pixel scanning mode (frequency set to 10Hz), with THz beam

Fig. 14. Measurement of 8-pixel line, THz beam centered in-between the fourth and fifth pixels.

(340GHz) centered in-between the fourth and fifth pixels. The upper waveform shows the output signals from subsequent pixels (detectors), denoted by numbers above the trace. In this way the power distribution within THz beam in vertical direction is illustrated. The lower, blue waveform in the figure is the triggering signal generated by measurement unit and synchronized with pixel switching, 5 times wider pulse indicates the first pixel.

More detailed description of the developed readout system has been presented in [17].

E. The Second Readout System

The first readout system presented in the previous subsection was constructed to check the design assumptions of the partially-parallel structure, which were next implemented in the aforementioned multi-channel readout IC. This latter integrated circuit became the central part of the second readout system developed by the authors. The hardware part of this device, presented in Figure 15 is assembled in the shielding enclosure fitted to the THz optical setup. It supports the same type of removable, 8-element pixel lines assembled on tiny PCBs, as its predecessor. The pixel line selected accordingly to the need of an experiment, is installed inside the shielding enclosure, in the socket of the upper PCB, just beneath the slot directing the THz radiation in. The hardware part of the system, designed in a modular way,

Fig. 15. The hardware part of the second measurement system. The top cover removed for better visibility of internal components. The installed pixel-line (small form factor PCB) can be seen in the center of the upper PCB.

comprises three PCBs with electronic components grouped according to their functions, as well as, taking into account the guidelines of interference minimization. The upper PCB with the pixel line socket at its center, contains the whole analog signal path of the system. Its most important component is the previously described 8-channel readout IC, complemented with the offset compensation network built of the signal relays and two quad-channel DAC providing the input offset compensation voltages, as well as a single DAC used for the output offset compensation. The fourth, octal DAC produces the bias voltages (VGS) for pixel-line elements. The DACs share two precise reference voltage sources. The lower PCB contains the 8-bits ATMega128 MCU, which supervises the operation of the hardware and communicates with the PC acting as measurement system controller by a means of the USB interface, which components are grouped at the third, front panel PCB. Taking into account the relatively low data processing rate required by either the THz spectroscopy or imaging, the serial link operating at 115200 baud is considered to be fast enough to handle the data and control transmission.

The hardware part of the system was designed with a special emphasis placed on minimization of interferences received from outside as well as ones generated inside, by the digital part of the circuit. First, the PCBs of the device were designed in a way to group the vast majority of their components and signal connections on their outer layers (top for the upper PCB and bottom for the lower one) and to keep the ground planes at their inner layers (bottom for the upper PCB and top for the lower one) to act as the shield against parasitic coupling between analog and digital circuits. Second, the analog and digital domains have their own, separate linear voltage regulators, with their inputs decoupled by inductors, and the output power tracks routed separately. Third, the SPI bus for data converters and all control signals generated by the MCU for the readout IC are separated from the digital domain by means of optocouplers, in similar manner the USB interface features full galvanic separation to minimize interferences produced by the circuits of PC. Finally, the rechargeable battery unit or dedicated, low-noise power supply can be used as a power source for the device.

The second readout system, unlike the first one, was designed not as a standalone device but as a part of larger laboratory setup deployed for THz spectroscopy or imaging. For that reason its user interface was implemented as a measurement application intended to be run under NI LabVIEW^{TM}. It provides the effective platform for setting the pixel scanning modes, the frequency and the gain of the measurement unit signal path and for the visualization of measurement results. It also allows to create the definition of processes pixel-lines and store them into a file as a collection of VGS for all their elements. The most sophisticated part of the measurement software is related to the offset cancellation. The procedure starts with acquisition of the output signals for each channel (i.e. the detector with its readout circuitry) in a state of THz radiation absence. Next, the offset compensation values are calculated by the software and fed, via the single channel digital to analog converter to the differential amplifier preceding the output of the signal path. Originally it was planed to use the input offset compensation network utilizing the negative input of each modulator, separate for each channel. In this way, the input offset compensated at the very beginning of the signal path would not limit the dynamics of succeeding gain stages. However, in spite of using the precise DACs, the calibrated reference voltage sources and high quality passive components, it was not possible to achieve the satisfactory thermal stability of the system. This problem was related to the excessive heat generation by the MCU. As a solution, it was decided to deploy only the output offset compensation circuitry, which is significantly less sensitive to the thermal drift due to the signal range it operates in. Another important functionality implemented within the measurement application is the autocalibration of the pixel-line bias. The procedure gradually increases the VGS voltage for a specific element of the detecting line and detects the global maximum, filtering out the encountered fluctuations. Such a result is automatically stored within a pixel-line definition file and can be fine-tuned by the user.

The Figure 16 presents the front panel of the discussed measurement application. The measurement results presented as bar graph correspond to the median value obtained for 2000 samples. In this case they were acquired for the substitute source of the low-voltage signal with a set of voltage dividers (1/4, 1/3, 1/2, 1, 1/4, 1/3, 1/2, 1) applied to subsequent inputs of the measurement unit, utilized during laboratory tests.

The results gathered during the measurement performed in the laboratory of the IOE-WAT with detecting pixel-line and THz source are shown in Figure 17. In this experiment the pixel-line consisted of the same type detecting elements - one intended for imaging purpose was deployed and the THz radiation was centered at the fourth element of the line. In this way the acquired result illustrates the power distribution across the vertical axis of the THz beam.

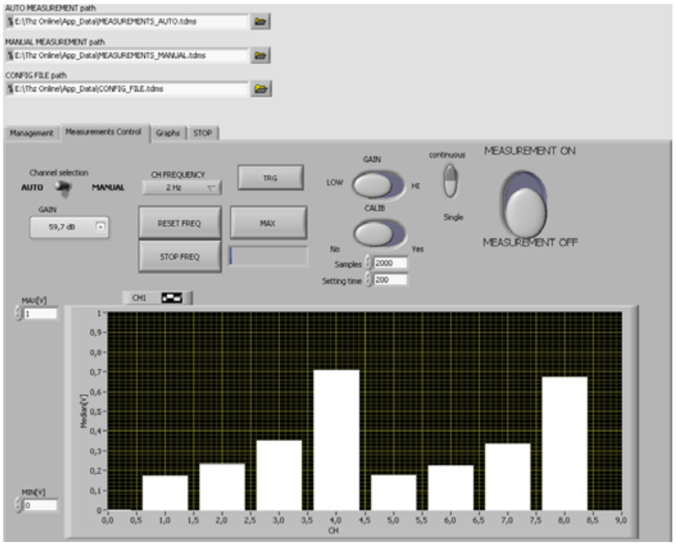

Fig. 16. Front panel of the dedicated measurement control application, intended for use with NI LabVIEW.

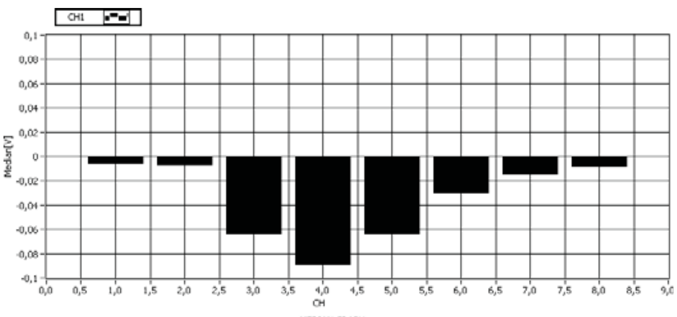

Fig. 17. Measurement results obtained for automated pixel scanning mode with a pixel-line used for imaging (the same type of pixels) and the THz beam centered on its 4th element.

IV. Conclusions

The research work on increasing the effectiveness of NMOS based THz detectors, as well as one addressing the readout circuits targeted for such devices has been described in the paper. The authors proved that modified version of the $3\mu m$ CMOS silicon process can be successfully used to manufacture the THz detectors on-chip integrated with receiving antenna. Moreover, the series of integrated circuit was designed, manufactured and tested, becoming the interesting replacement of the standard lock-in equipment, typically used in laboratory experiments performed with small, low-frequency signals. Besides, proposed solution addresses in comprehensive way the issues of multi-pixel detector lines, particularly important in THz spectroscopy applications.

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