

PERFORMANCE STUDY OF A NEW HIGH INSTANTANEOUS POWER IMPULSE CONVERTER WITH A SWITCHED CAPACITOR UNIT*

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Abstract: A new high instantaneous power impulse converter (HIPIC) with a switched capacitor unit has been presented. HIPIC generates very short impulses (hundreds of microseconds) of instantaneous power in megawatt range while the average power is much lower (tens of kilowatts). The presented topology is composed of step-down converters, an H-bridge converter and a switched capacitor, adjusted with a new current control. It allows one to achieve the output current impulses with very short rising and falling times and strict peak current control with low ripples.

Keywords: *high instantaneous power impulse converter, impulse converter, switched capacitor converter*

1. INTRODUCTION

High instantaneous power impulse converters (HIPIC) in contrast to traditional DC suppliers with same average power (1–20 kW) are characterized by high power in megawatt range delivered to the output in a very short time (Fig. 1). The impulse duration T_{IMP} delivered to the output lasts up to 1 ms with frequency f_{PULS} in the range of 1–10 kHz but a duty cycle of impulses is lower than 1%. HIPICs are used in many industrial applications such as Cockcroft–Walton (CW) generators (voltage multipliers), Marx generators and impulse lasers [1–4].

In HIPIC, a precise control of the output current during extreme short pulse including also rising and falling slopes has to be guaranteed by appropriate converter topology and advanced algorithm [5, 6]. Therefore a new HIPIC consists of few converter units including a step-down, a switched capacitor and an H-bridge, and also the algorithm that allows one to control the output current independently of the capacitor power bank discharge. The simulation results present proper operation of HIPIC, finally proven by experimental verification.

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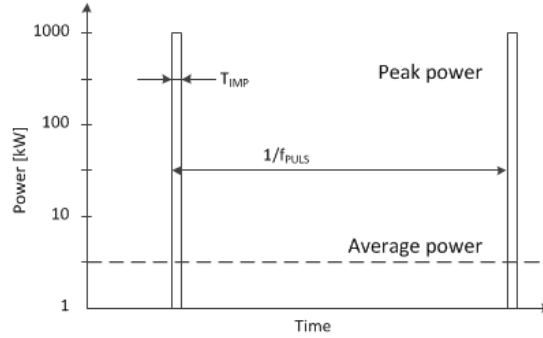


Fig. 1. Typical impulses of HIPIC (solid) and its average power (dashed)

2. BASIC ASSUMPTIONS

The following parameters describing instantaneous current were introduced to form the impulse that should be approximate square wave: the rising time (T_{RISE}), the tail time (T_{TAIL}) which is equivalent to the falling time and the current ripples (I_{RIPPLE}) during the impulse (Fig. 2).

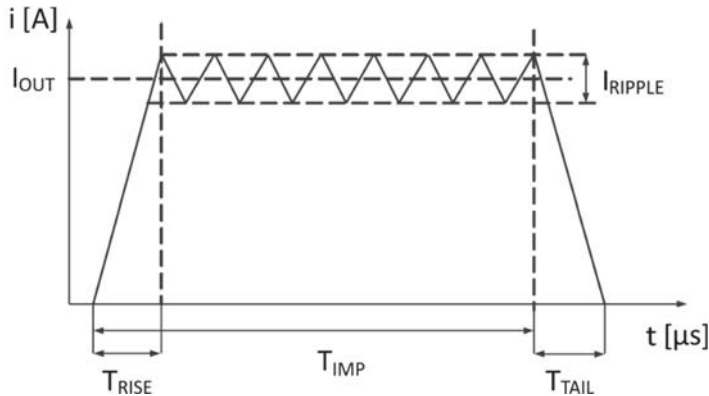


Fig. 2. Time and current parameters in impulse of the HIPIC

The main target is to minimize these parameters and force:

- the fastest output current rising (the shortest rising time, T_{RISE}),
- minimization of the peak current control and current ripples I_{RIPPLE} during the impulse (T_{IMP}),
- the fastest output current falling (the shortest falling time, T_{TAIL}).

The operation was divided into four stages: rising slope of output current impulse (I), peak current control (II), falling slope of output current impulse (III), and charging of

main and switched capacitors (IV) [5]. Additional functionality of the converter configuration is unipolar and bipolar mode of operation (Fig. 3).

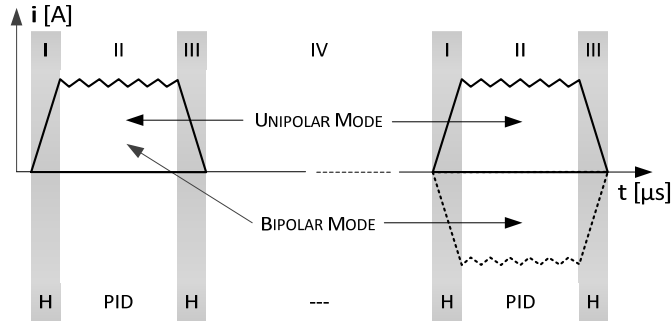


Fig. 3. Operation stages in the HIPIC: H – hysteresis controller, PID – PID controller

3. PROPOSED TOPOLOGY FOR HIGH INSTANTANEOUS POWER IMPULSE CONVERTER (HIPIC)

A HIPIC consists of three units (Fig. 4): a step down converter [7–11], a switched capacitor converter [12], and a H bridge converter. The step-down unit located in the input consists of 4 parallel converters (transistors S1–S4 and diodes D1–D4) interleaved modulated with a very high switching frequency, significantly decreasing output current ripples [13, 14].

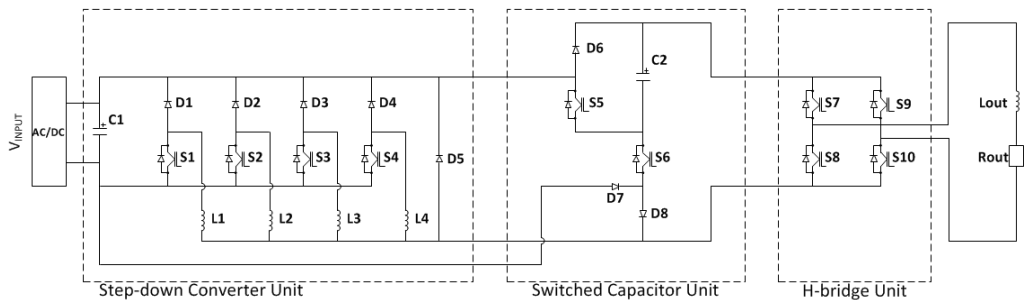


Fig. 4. Proposed topology for HIPIC

The main goals for output H-bridge converter (transistors S7–S10) is time minimization of the current impulse falling slope, and a possibility of selection between unipolar/bipolar mode of operation. Therefore transistors in this unit are switched with very low frequency that equals the frequency of output impulses shown in Fig. 1. The former goal is obtained simply when all transistors are switched off, which forces the output

current flow through the anti-parallel diodes embedded in switches S7–S10, and as a result the reverse voltage is applied to the output. The latter goal is obtained when pairs of transistors S7, S10 and S8, S9 are switched diagonally to change the output current polarization for bipolar operation.

A low frequency switched capacitor unit located in the middle of the device is used to improve performance during rising and falling slopes of the output current, which is especially important for very short current impulses, lower than 200 μs . A switched capacitor unit (capacitor C2, transistor S5 and diode D6) has a possibility of series-parallel connection to the main capacitor bank C1 [12]. It allows doubling of the output voltage to force faster rising and falling slopes of the output current. Thanks to this the current, the impulse shape is close to the square wave. The switched capacitor C2 is charged by the transistor S6 and diode D8. The applied diode D7 bypasses inductors during the falling slope of current.

4. PROPOSED CURRENT CONTROL METHOD FOR HIGH INSTANTANEOUS POWER IMPULSE CONVERTER (HIPIC)

The current control loop is a main part of the high instantaneous power impulse regulation [5]. A simplified control scheme presented in Fig. 5 is composed of the following blocks: signals settings ($T_{\text{IMP}}, f_{\text{PULS}}$), current control, initial value, compensation of capacitor voltage changes and duty cycle sequencer.

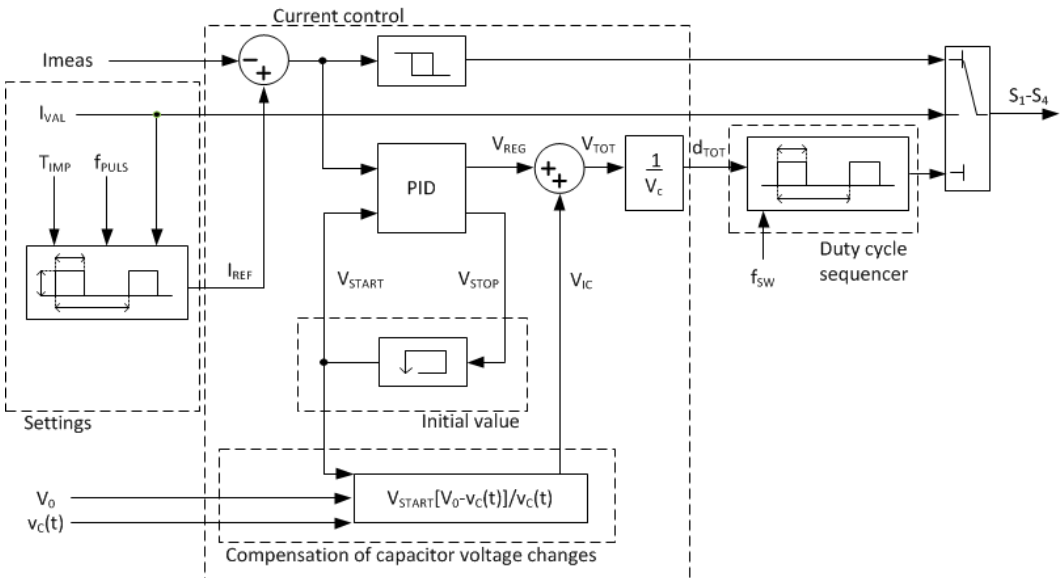


Fig. 5. Control algorithm scheme of the HIPIC

The reference value of the output current I_{REF} is determined in signals settings block and it is based on the set parameters: impulse time (T_{IMP}), pulsing frequency (f_{PULS}) and set output current value (I_{VAL}). Then in the current control block, the current control loop is composed of two different controllers (Fig. 3): a hysteresis controller, where states of transistors are set directly, and a PID controller, where the duty cycle is calculated (d_{TOT}) [15]–[17]. There are two inner blocks included in the current control block. In the former, an initial value for PID controller (integral part) is obtained. The latter is designed due to the big discharge of the main capacitor (C1) during the impulse so that the PID controller acts independently of the main capacitor voltage (v_{C1}) by introducing the compensation of changes of the capacitor voltage (CCVC). Finally, the duty cycle sequencer sets transistor signals (S1–S4) during the output peak current based on the calculated duty cycle.

In Table 1, possible states of all transistors in HIPIC depending on the impulse stage are presented: where 1 is on state, 0 is off state, 0–1 means that transistor is modulated, 1/0 – transistor is on during the positive impulse of bipolar operation, and 0/1 – transistor is on during the negative impulse of bipolar operation.

Table 1. Transistor states in HIPIC

HIPIC unit	Transistor	Rising slope	Peak current control	Falling slope	Capacitor charging
Step-down converter unit	S1	1	0–1	0	0–1
	S2	1	0–1	0	0–1
	S3	1	0–1	0	0–1
	S4	1	0–1	0	0–1
Switched capacitor unit	S5	1	0	0	0
	S6	0	0	0	1
H-bridge unit	S7	1/0	1/0	0	0
	S8	0/1	0/1	0	0
	S9	0/1	0/1	0	0
	S10	1/0	1/0	0	0

The switching frequency of a single transistor in a step-down converter (S1–S4) is 10 kHz and transistor signals are interleaved $T_S/4 = 25 \mu s$. In the described control method, the duty cycle is updated every $T_S/4 = 25 \mu s$ in the moments $T(S1)–T(S4)$ when transistors S1–S4 switch on, respectively. Moreover each of these transistors switches with the duty cycle which is last calculated while the specific transistor remains switched on (Table 2). As a result the duty cycle is divided into 4 parts:

$d_I \in <0; 0.25)$, the relevant duty cycle is calculated, when the transistor is switched on,

- $d_{II} \in <0.25; 0.5)$, the relevant duty cycle is calculated $0.25 T_S$ after switching on the transistor,

- $d_{III} \in <0.5; 0.75>$, the relevant duty cycle is calculated $0.50 T_S$ after switching on the transistor,
- $d_{IV} \in <0.75; 1.0>$, the relevant duty cycle is calculated $0.75 T_S$ after switching on the transistor.

Table 2. The time of duty cycle calculation vs. duty cycle value and the relevant transistor

d	Transistor			
	S1	S2	S3	S4
$<0.0; 0.25>$	$T(S1)$	$T(S2)$	$T(S3)$	$T(S4)$
$<0.25; 0.5>$	$T(S2)$	$T(S3)$	$T(S4)$	$T(S1)$
$<0.5; 0.75>$	$T(S3)$	$T(S4)$	$T(S1)$	$T(S2)$
$<0.75; 1.0>$	$T(S4)$	$T(S1)$	$T(S2)$	$T(S3)$

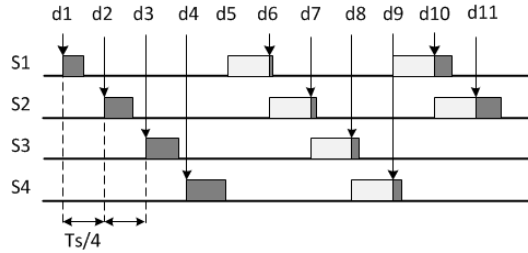


Fig. 6. Proposed control with the duty cycle calculated every $T_S/4$ and updated for every transistor

In Figure 6, the signals of four transistors (S1–S4) with interleaving are presented. For the first 4 pulse width modulation (PWM) signals, the relevant duty cycle value $d1-d4$ is less than $0.25d_i$ and it is calculated at the switch on of each transistor. Then for the 5th presented PWM signal, the duty cycle $d5$ is calculated, however as $d5 \geq 0.25$, the next duty cycle $d6$ becomes the relevant one for this transistor. In further steps, the duty cycle is calculated $0.25T_S$ after switching on the specific transistor (duty cycle d_{II} is between 0.25 and 0.50).

5. SIMULATION AND EXPERIMENTAL RESULTS

All the simulations in the Saber software (Figs. 7, 8) and experimental tests (Fig. 9, 11) have been carried out with parameters listed in Table 3. The most relevant variables of HIPIC are presented in Fig. 7. The output current consists of four currents i_{L1-L4} , where each of them has significant peak-to-peak ripples up to 200 A but thanks to interleaving operation of transistors, the output current i_{OUT} has ripples less than 10 A. The output

voltage v_{OUT} reaches its maximum during the current impulse rising time ($t1-t2$) to obtain as fast as possible the reference current value. During the falling slope ($t3-t4$), the maximum reverse voltage is applied. In the impulse peak ($t2-t3$), the output voltage depends on the duty cycle (d_{TOT}) which is calculated to keep the output current on its reference value [5]. Figure 8 presents a HIPIC bipolar mode of operation.

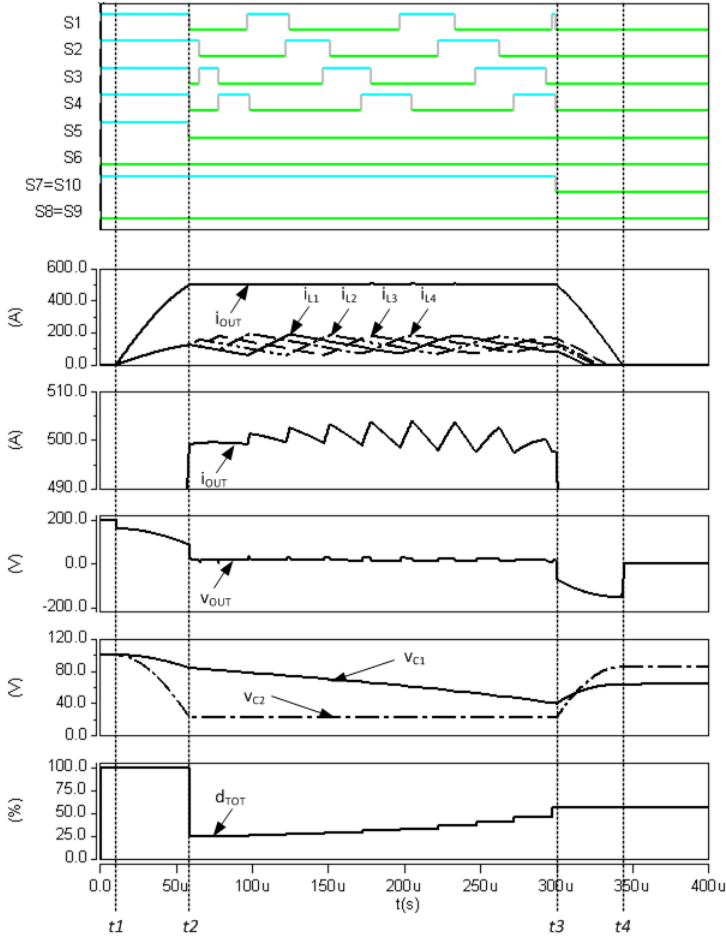


Fig. 7. Relevant variables of HIPIC, S1–S8 – transistor signals, i_{OUT} – output current, i_{L1-L4} – step-down converter currents, v_{OUT} – output voltage, v_{C1} – main capacitor voltage, v_{C2} – switched capacitor voltage, d_{TOT} – total duty cycle

Table 3. Parameters used in simulation and experimental study

Symbol	C_1	C_2	$v_{C1} = v_{C2}$	L_1-L_4	L_{OUT}	R_{OUT}	I_{OUT}	T_{IMP}	f_{SW}
Value	800 μ F	180 μ F	100 V	12 μ H	12 μ H	35 m Ω	500 A	300 μ s	10 kHz

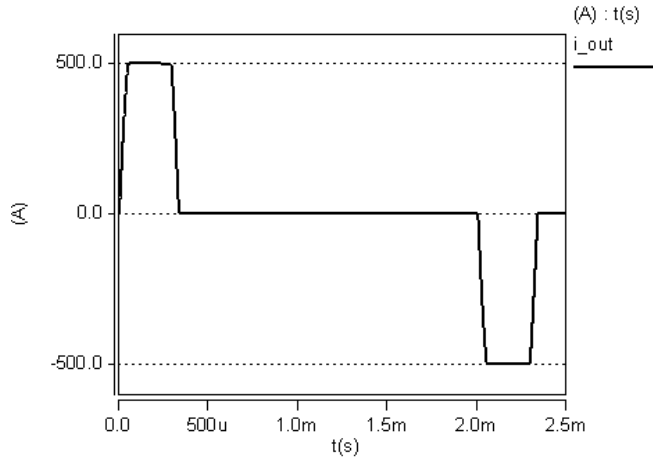
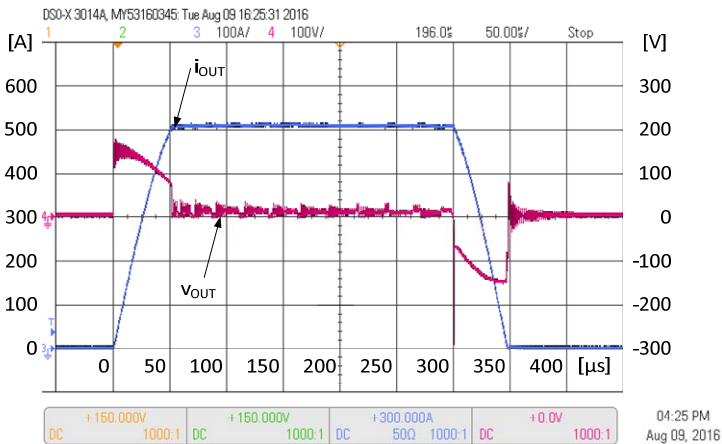


Fig. 8. HIPIC bipolar mode of operation

Fig. 9. HIPIC output current (i_{OUT}) and output voltage (v_{OUT})

The experimental verification confirms excellent performance of HIPIC (Figs. 9, 10). The output current obtains very short rising and falling times and it is controlled properly with very small ripples during the whole impulse, which was the main requirement of the project. Figure 10 shows that the switched capacitor C2 is discharged during the rising slope of the output current, then it is isolated from the output during the impulse, and finally charged back during the falling slope by energy recuperated from inductive load. During recuperation, the capacitor C1 is partly charged too. Moreover, as the output current keeps its value at 500 A in the whole impulse, the currents in step-down converters are much lower and do not exceed their peak values of 200 A (Fig. 11).

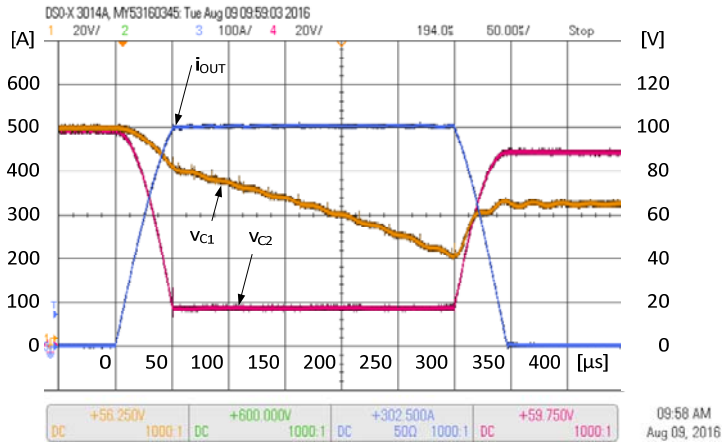


Fig. 10. HIPIC capacitor voltages: main capacitor voltage (v_{C1}) and switched capacitor voltage (v_{C2}) with the output current (i_{OUT})

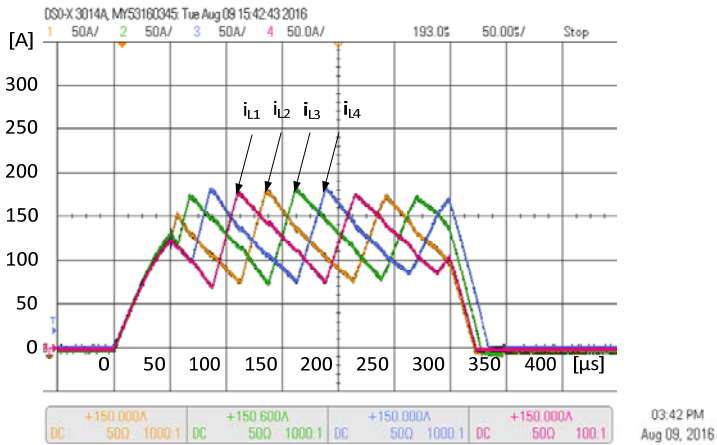


Fig. 11. Step-down converter currents (i_{L1} – i_{L4})

6. CONCLUSION

The paper presents a high instantaneous power impulse converter (HIPIC) with a switched capacitor unit. The improved HIPIC configuration based on a step-down converter unit, H-bridge converter unit and switched capacitor converter unit allows an accurate control of the output current impulse. Four step-down converters that are connected in parallel give an option of interleaving operation with very small peak current ripples. Applied H-bridge and switched capacitor units significantly shorten the output

current rising and falling slopes. The current impulses close to square wave are possible to achieve thanks to the applied current control method, where two types of controllers are used: a hysteresis controller for rising and falling slope and a PID controller for peak current regulation. The proposed topology and control method significantly increase the performance of output current impulses in the HIPIC which is presented in computer simulations and confirmed in experimental results. It gives an opportunity for application in many fields of industry.

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