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Design and Noise Analysis of a Novel Auto-Zeroing Structure for Continuous-Time Instrumentation Amplifiers

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***Abstract*—This paper introduces a low-noise, low-power amplifier for high-impedance sensors. An innovative circuit using an auto-zeroed architecture combined with frequency modulation to reject offset and low-frequency noise is proposed and analysed. Special care was given to avoid broadband noise aliasing and chopping in the signal path, and to minimize both the resulting equivalent input offset voltage and equivalent input biasing current. The theoretical noise analysis of the proposed topology covers most of the noise sources of the circuit. Simulations show that the input-referred noise level of the circuit is $13.4nV/\sqrt{Hz}$ for a power consumption of $85\mu A$ with a power supply from 1.8V to 3.6V.**

***Keywords*—Front-end, instrumentation amplifier, low noise, low power, chopper, auto-zero**

I. Introduction

THE constant miniaturization of the processes during the last decades promoted the increase of the digital functionalities on the System-On-Chip (SOC). Suitable interfaces between the analog and the digital domain (such as DAC and ADC) remain essential analog sub-circuits on SOCs. In most cases, however, the signals delivered by external or integrated sensors need to be preconditioned before being converted by an Analog-to-Digital Converter. In order to properly acquire signals from sensors with a small output voltage range and a limited deliverable current, front-ends with low noise levels (a few $nV/\sqrt{Hz}$) are used. Usually, additional constraints are put on front-ends, such as: a) a high input dynamic range and a high common mode rejection ratio (CMRR); b) a very high input impedance and c) a low power consumption.

In this paper, the most common low-frequency noise rejection methods are reviewed in Section II. Sections III and IV detail the selected implementation, with a circuit level noise analysis in Section V. The simulation setup and obtained results are in Section VII, while the last section concludes this paper.

II. Offset and Flicker Noise Reduction Techniques

In integrated circuits, the two main noise sources are the thermal noise and the flicker noise. The thermal noise, generated in the resistors and the transistors has a white noise spectrum, independent of the frequency. Lowering the white noise level is usually done increasing the power consumption. The flicker noise, also known as 1/f noise as its spectral density is inversely proportional to the frequency, is mostly generated in the active devices. The most straightforward way to reduce 1/f noise is to increase the device area.

There are several rejection techniques to reduce offset and 1/f noise. Even if most of them operate at circuit level, some physically reduce the noise generated in the transistors, de-correlating the samples [1]. The most common circuit techniques are briefly reviewed hereafter:

Correlated Double Sampling. CDS techniques sample during a first initialization phase the offset (and the 1/f noise) at the input of an amplifier, so that it can be further compensated during the active phase. These techniques are well-suited for discrete systems, such as switched-capacitors circuits where they are widely spread [2], [3], [4].

Another discrete time compensating method [5] is compensating the offset injecting a current at the output of an amplifier. During an initialization sequence, the offset is measured and compensated by successive approximations. This method requires the amplifier to be disconnected from the rest of the circuit during the measure phase.

Chopper Stabilization. In the CHS technique, the noise sources, usually amplifiers, are placed between a modulator and a demodulator to shift the 1/f noise outside the signal baseband frequency [4], [6], [7]. Due to their simplicity, choppers are usually preferred over pure single frequency (sinusoidal) modulators.

Auto-Zeroed Amplifiers. This method (Fig. 1), analysed in [8], stores a measurement of the offset in an auxiliary branch, in parallel with the main amplifier. The offset is then compensated through a secondary input located after the input differential pair of the main amplifier. Also called Ping-Pong auto-zeroing when two nulling paths are used in alternance, this method is well-suited for continuous-time circuits. Sometimes used alone is the past [9], it is nowadays often combined with chopper modulation techniques [7], [10], [11].

III. Proposed Circuit

The circuit presented in this paper is designed to be integrated in the front-end of a very high resolution (>16bits) AD converter. It has to fulfill the following specifications:

- Low noise: $10nV/\sqrt{Hz}$ input-referred in the $0-100Hz$ band.

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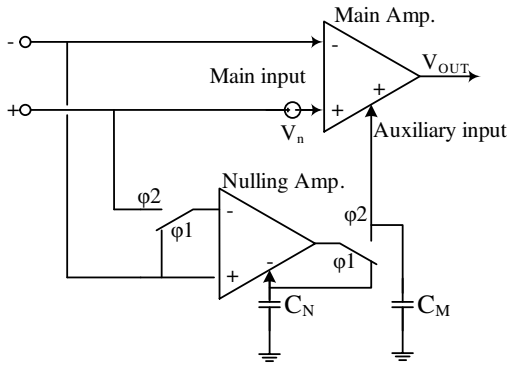

Fig. 1. Classic continuous time auto-zeroed amplifier.

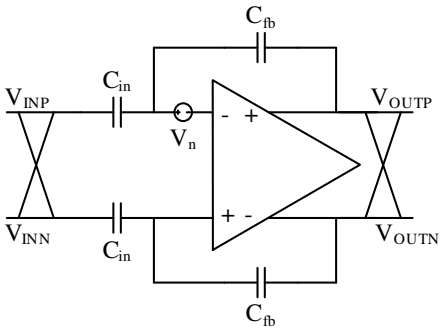

Fig. 2. Flicker noise rejection using chopper modulation.

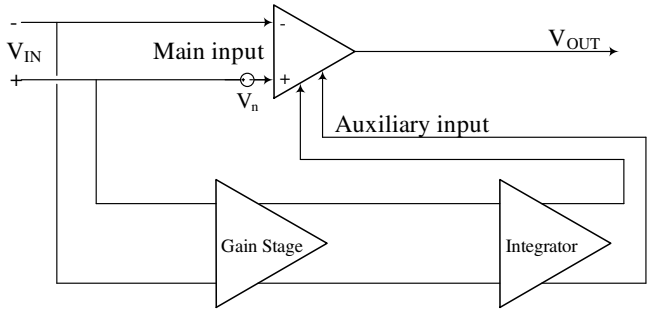

Fig. 3. Proposed auto-zero amplifier principle.

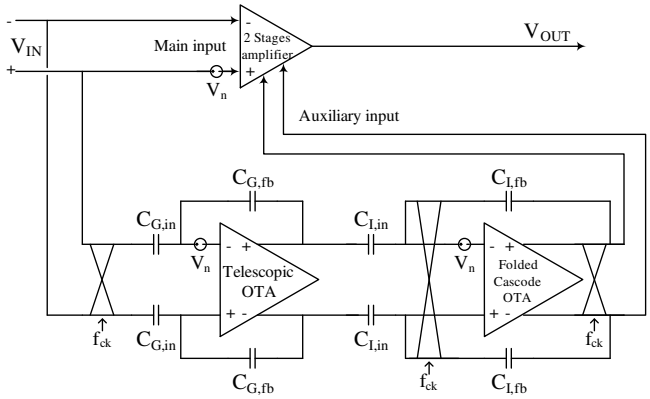

Fig. 4. Proposed auto-zero amplifier implementation.

- Low power: $< 100uA$
- Sensor output impedance range: 100Ω – $1M\Omega$
- Gain: programmable, 10 typ.
- Process: CMOS $0.18\mu m$, $1.8V - 3.6V$
- Input range: $Vss + 50mV$ – $Vdd - 50mV$

Sample-data systems are not suited for this application due to the wideband noise aliasing occurring in the sampling process, e.g. in a switched-capacitor circuit, the noise level is set by the input sampling capacitors: $V^2_{n,RMS} = kT/C$. As a result, an increased power consumption and large chip area can be expected.

Simple chopper stabilisation circuits using switched capacitors as the input stage (Fig. 2) are only applicable for low impedance sensors.

Classic continuous-time auto-zero amplifiers (Fig. 1) are not suitable either for very low noise circuits as the noise of the nulling amplifier is sampled and aliased down in the signal baseband during its own offset compensation phase.

Ping-Pong auto-zeroed amplifiers are neither suited for low-noise low-power applications as the duplicated nulling path is nearly doubling the power consumption.

The architecture of the proposed circuit is inspired by the classic auto-zero amplifier (Fig. 1), using a continuous-time main amplifier and a nulling branch connected to an auxiliary input. The new architecture (Fig. 3) of the auxiliary branch is made of a continuous-time low-noise first gain stage followed by a switched-capacitor integrator. This structure allows, as the classic auto-zero, a rejection of the 1/f noise in a continuous-time system. The fully differential architecture of the nulling branch has the following advantages:

- Very good rejection of the offset and 1/f noise of the main integrator, as the combined gain of the pre-amplification and of the integrator is used.
- Lower gain stage offset, compared with a single-ended structure. The offset is only created by the transistors mismatch. This lowers statistically the mean current delivered by the sensor.
- As the system is not having anymore two distinct phases (with different loads, and operating conditions), stability is easier to achieve.
- The sensitivity to external references (necessary in [8], Fig. 1 for the auxiliary inputs) is lowered. The only required voltage reference left is the one generating the common-mode. It is used to properly bias the input and output common-modes of the amplifiers.

Moreover, the equivalent DC input bias current due to the switching operation of the input chopper is proportional to the residual input offset. This architecture is designed for input bias currents in the $1 - 100pA$ range.

IV. Implementation

The implementation of the amplifier is shown in Fig. 4. The use of choppers and input capacitors allows firstly to reject the flicker noise of the amplifier and secondly to guarantee a zero DC input current during each phase of the chopper. This structure also allows decoupling the common-modes of the input and of the virtual ground of the gain amplifier. The input resistors of the integrator are emulated using switched-capacitors. In order to have symmetrical phases, the capacitors

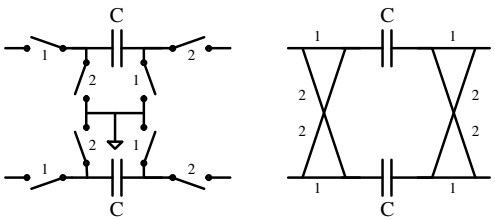

Fig. 5. Switched-capacitors resistor using left: standard implementation, right: symmetrical implementation with choppers.

are crossed instead of being connected to a reference potential (Fig. 5). The amplifier of the integrator is also placed between choppers to reject the flicker noise. If identical frequencies are selected for the modulation of the auxiliary chain amplifiers and for the switching of the integrator input capacitors, it is possible to reduce the number of extra switches. The one demodulating the gain stage is compensated with the one on the left of the integrator's input capacitors. The chopper on the right of the switched capacitors is combined with the one modulating the input of the integrator's amplifier to have only one chopper left on the feedback path. The three remaining choppers are shown in Fig. 4. For the sake of clarity, the circuits controlling the common-mode at the input and at the output of the amplifiers are not shown. They are implemented using switched-capacitor technique keeping in mind the noise constraints.

A telescopic structure is selected for the OTA of the gain amplifier to optimize the noise – power consumption ratio and to have a sufficiently high open-loop gain. The reduction of output voltage dynamic range induced by this cascode topology is acceptable as the input of the integrator is supposed to be low once the loop is settled. The OTA of the integrator should have a high DC gain, a large dynamic range and a power consumption much lower than the previous stage. A folded-cascode structure is appropriate here, as the noise contribution of this amplifier is much lower than the noise level of the gain stage (see noise analysis, Section V-C). The input capacitors of the amplifier and the gain of the first stage are sized to minimize the noise contribution of the integrator while keeping a reasonable surface for the capacitors.

V. Noise Analysis

Two noise effects are considered in the noise analysis:

- offsets and flicker noise are placed in the first category. Rejection techniques, auto-zero and frequency shift, are implemented to reduce these noises,
- the second category is dedicated to the wideband thermal noise. As this noise is covering the whole spectrum, it cannot be reduced using modulation or correlation techniques.

A. Auxiliary Chain Flicker Noise

As the two amplifiers in the nulling path are working around the modulation frequency f_{ck}, their offsets as well as their 1/f noise have only little impact on the global output noise. The remaining noise contribution of the flicker noise around the modulating frequency is reduced by increasing the gate area of the input differential pairs. Both the 1/f and the thermal noise due to these two amplifiers are evaluated in Section VII.

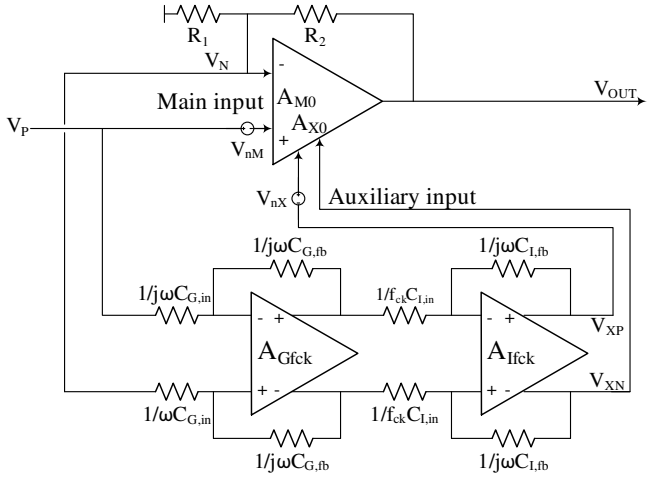

Fig. 6. Complex representation of the nulling amplifier in the signal baseband (low frequencies).

B. Main Amplifier 1/f Noise

To analyse the noise at low frequencies (in the signal baseband), the following assumptions are considered:

- the main amplifier open-loop DC gains are finite, A_{M0} for the main input and A_{X0} for the auxiliary input,
- the OTA open-loop gain at the chopper frequency of the gain stage is $A_{Gf_{ck}}$,
- the OTA open-loop gain at the chopper frequency of the integrator is $A_{If_{ck}}$.

The gains, node names and noise source names are shown on the complex representation, Fig. 6. The transfer function of the gain stage is given by:

$$H(j\omega) = -\frac{C_{G,in}}{C_{G,fb}} \frac{A_{Gf_{ck}}}{A_{Gf_{ck}} - 1 - \frac{C_{G,in}}{C_{G,fb}}} \cong -\frac{C_{G,in}}{C_{G,fb}} \quad (1)$$

For the integrator:

$$\begin{aligned} H(j\omega) &= \frac{A_{If_{ck}}}{1 + j\omega \frac{1-A_{If_{ck}}}{f_{ck}} \frac{C_{I,in}}{C_{I,fb}}} \\ &\cong \frac{A_{If_{ck}}}{1 - j\omega \frac{A_{If_{ck}}}{f_{ck}} \frac{C_{I,in}}{C_{I,fb}}} \end{aligned} \quad (2)$$

At low frequencies, below the pole of the integrator, the transfer function of the integrator is the open-loop gain: $H(j\omega) = A_{If_{ck}}$.

Referencing the offsets and 1/f noise to the input V_P of the instrumentation amplifier, the Flicker Noise Rejection Rate is, for the main (FNRR_M) and auxiliary (FNRR_X) inputs:

$$\begin{aligned} \text{FNRR}_\text{X} &= \frac{V_P}{V_{nX}} = \frac{C_{G,fb}}{C_{G,in}} \frac{1}{A_{If_{ck}}} \\ \text{FNRR}_\text{M} &= \frac{V_P}{V_{nM}} = \frac{C_{G,fb}}{C_{G,in}} \frac{A_{M0}}{A_{If_{ck}} A_{X0}} = \frac{A_{M0}}{A_{X0}} \text{FNRR}_\text{X} \end{aligned} \quad (3)$$

The previous equations show that it is possible to increase the signal over noise ratio, increasing the gain of the gain stage

or the integrator's OTA open-loop gain. The noise contribution of the main input can also be reduced balancing the main and auxiliary open-loop gains of the main amplifier. The equations (3) being the offset rejection rate, the equivalent offset at the input of the amplifier is:

$$V_{off,eq} = V_{offM}\text{FNRR}_\text{M} + V_{offX}\text{FNRR}_\text{X} \tag{4}$$

with V_{offM} and V_{offX} the offsets at the inputs of the main amplifier. The mean DC current delivered by the sensor is:

$$\begin{aligned} I_{sensor} &= \frac{V_{off,eq}}{R_{in,eq}} = V_{off,eq}C_{G,in}f_{ck} \\ &= \frac{f_{ck}C_{G,fb}}{A_{If_{ck}}}\left(V_{offM}\frac{A_{M0}}{A_{X0}} + V_{offX}\right) \end{aligned} \tag{5}$$

where $R_{in,eq}$ is the equivalent input resistance of the auto-zeroed amplifier. The designed amplifier input current is $3pA$, with an equivalent input resistance of $320k\Omega$ and an estimated equivalent offset of $1\mu V$.

C. Thermal Noise

Amplifiers: The thermal noise of the main amplifier is lowered in the signal baseband using the offset compensation provided by the auxiliary chain.

The thermal noise of the gain stage is not lowered. The thermal and flicker noise at the chopper frequency f_{ck} is shifted to the signal baseband. The 1/f noise can be attenuated increasing the size of the differential pair, while the thermal noise can only be reduced increasing the bias current I_0 of the OTA. For a single transistor, the noise spectral density is given by $NSD = (8/3)kT/g_m$. For telescopic and simple OTAs, the input referred noise is given by:

$$NSD_{IN,OTA} = \frac{16}{3}\frac{kT}{g_{m,dp}}\left(1 + \frac{g_{m,dp}}{g_{m,cm}}\right) \tag{6}$$

where $g_{m,dp}$ and $g_{m,cm}$ are the transconductances of the transistors of the differential pair and of the current mirror. If the differential pair is in weak inversion ($g_m \cong I_0/(2nU_t)$) and the current mirror is in strong inversion (assuming a reasonable ratio between $g_{m,dp}$ and $g_{m,cm}$ equal to 0.25 to keep some dynamic range at the output), it is possible to link the generated noise to the current consumption.

$$NSD_{IN,gain\_stage} = \frac{16}{3}\frac{kT}{g_{m,dp}}(1 + 0.25) = \frac{40}{3}\frac{nU_t}{I_0}kT \tag{7}$$

The input-referred noise power from the integrator is divided by the gain $C_{G,in}^2/C_{G,fb}^2$. The input-referred noise spectral density is thus given by:

$$NSD_{IN,integrator} = \frac{C_{G,fb}^2}{C_{G,in}^2}\frac{1}{f_{ck}}\frac{\alpha kT}{C_{I,in}}\left[\frac{V^2}{Hz}\right] \tag{8}$$

where α is a parameter depending of the amplifier topology. α is greater than one and lower than four for single stage OTAs.

Input chopper: The noise generated in the switches (with on-resistance R_{sw}) is first amplified by the gain stage and then sampled at the input of the integrator by the switched capacitors.

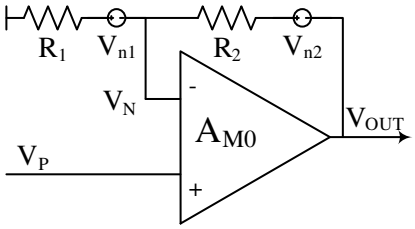

Fig. 7. Resistors noise.

The sampling aliases the whole noise spectrum into the frequency band between DC and the sampling frequency f_{ck}. The total RMS noise at the input of the integrator is given by

$$N_{RMS}^2 = \int_0^\infty 4kTR_{sw}\left|A(f)\right|^2 df\ \left[V^2\right] \tag{9}$$

where $A(f)$ is the transfer function of the gain stage. If the transfer function $A(f)$ has a single pole located in f_{cutoff}, the input-referred NSD of the input chopper is:

$$NSD_{IN,chopper} = 2\pi kTR_{sw}\frac{f_{cutoff}}{f_{ck}}\left[\frac{V^2}{Hz}\right] \tag{10}$$

This noise is lowered by decreasing the chopper switches' resistance R_{sw}.

Resistors: The thermal noise of the feedback resistors is not affected by the offset compensation. The equivalent circuit including the resistors' thermal noise is shown in Fig. 7.

The closed loop gain G of the main amplifier is defined by feedback resistors R_1 and R_2.

$$\frac{V_{OUT}}{V_P} = 1 + \frac{R_2}{R_1} = G \tag{11}$$

If the amplifier is ideal in the signal baseband, the output voltage is:

$$V_{OUT} = GV_P + (G-1)V_{n1} + V_{n2} \tag{12}$$

The output noise spectral density is, accounting for the resistors NSD $4kTR_{1/2}$:

$$\begin{aligned} NSD_{R,OUT} &= (G-1)^2 4kTR_1 + 4kTR_2 \\ &= 4kTR(G-1)\left[\frac{V^2}{Hz}\right] \end{aligned} \tag{13}$$

where R is the sum of the two resistances R_1 and R_2.

In the signal baseband, an open-loop gain much larger than the closed loop gain G can be assumed. The input referred noise spectral density then becomes:

$$NSD_{R,IN,baseband} \cong 4kTR\frac{G-1}{G^2}\left[\frac{V^2}{Hz}\right] \tag{14}$$

D. CMFB Contribution

Gain Stage CMFB: The input common-mode of the gain stage is set using the structure detailed in Fig. 8. The purposed topology sets the input common-mode to V_{cm} and forces the DC gain to zero.

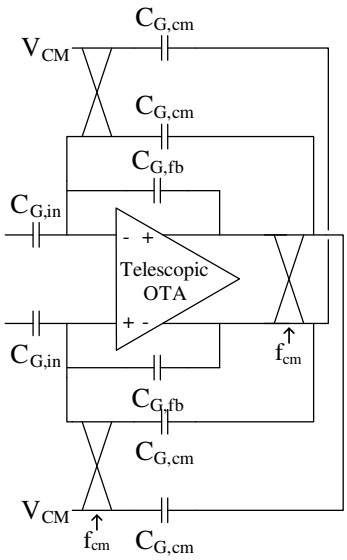

Fig. 8. Gain stage input CMFB.

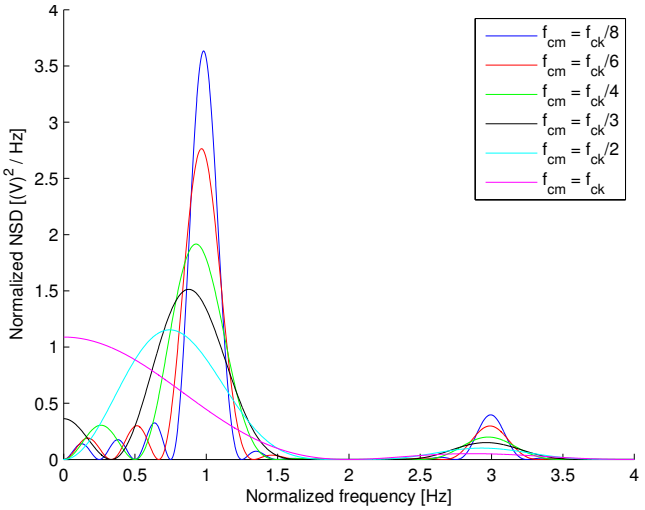

Fig. 9. Input-referred noise contribution of the gain stage CMFB circuit.

The switched-capacitors are modifying the gain stage transfer function to a high-pass filter with a cut-off frequency equal to:

$$f_{cut-off} = \frac{1}{2\pi R_{G,cm} C} = \frac{C_{G,cm}}{\pi C_{G,fb}} f_{cm} \tag{15}$$

where f_{cm} is the CMFB chopper frequency.

In order not to deteriorate the gain around the working frequency f_{ck}, the capacitor $C_{G,cm}$ should be much lower than the feedback capacitor $C_{G,fb}$.

The noise related to the input common-mode capacitors is created sampling capacitors $C_{G,cm}$ in a modulated environment (gain stage) before being demodulated and sampled (integrator). The noise analysis is decomposed in several substeps even if multiple operations are performed by a single component (ex: the demodulation and the sampling are performed by a unique set of switches at the input of the integrator). The mathematical steps are the following:

- A) Compute the RMS noise and the associated NSD without any (de)modulation
- B) Compute the demodulated noise
- C) Compute the sampled noise

A) The noise is first sampled on the capacitor $C_{G,cm}$:

$$N_{RMS}^2 = \int_0^\infty 4kTR_{sw} \left|H(j2\pi f)\right|^2 df = \frac{kT}{C_{G,cm}} \left[V^2\right] \tag{16}$$

As the capacitors $C_{G,cm}$ are holding the value during half of the period, the input-referred noise spectral density of this noise is:

$$\begin{aligned} NSD_{IN,mod} &= \frac{kTC_{G,cm}}{C_{G,fb}^2} \frac{\pi}{2f_{cm}} \left(\frac{\sin(f\pi/2f_{cm})}{f\pi/2f_{cm}}\right)^2 \\ &= \frac{kTC_{G,cm}}{C_{G,fb}^2} \frac{\pi}{2f_{cm}} \text{sinc}^2(f\pi/2f_{cm}) \left[\frac{V^2}{Hz}\right] \end{aligned} \tag{17}$$

B) The noise is generated in a modulated environment (between the input chopper and the output one included in the integrator block). The demodulated noise is obtained multiplying the modulated one with the chopping function:

$$\begin{aligned} NSD_{IN,demod} = &\frac{4}{\pi^2} \frac{kTC_{G,cm}}{C_{G,fb}^2} \frac{\pi}{2f_{cm}} \sum_{k=0}^{\infty} \frac{1}{(2k+1)^2} \\ &\left(\text{sinc}^2\left(\frac{((2k+1)f_{ck} - f)\pi}{2f_{cm}}\right) + \right. \\ &\left. \text{sinc}^2\left(\frac{((2k+1)f_{ck} + f)\pi}{2f_{cm}}\right)\right) \end{aligned} \tag{18}$$

C) The noise is finally sampled and held in the integrator. As the demodulation and the sampling are performed by the same set of switches at the input of the integrator, the sampling frequency is by construction twice the modulating one, $f_{sampling} = 2f_{ck}$.

$$\begin{aligned} NSD_{IN,SH} = &\frac{2kTC_{G,cm}}{\pi C_{G,fb}^2 f_{cm}} \text{sinc}^2\left(\frac{f\pi}{2f_{ck}}\right) \sum_{k=0}^{\infty} \sum_{j=-\infty}^{\infty} \frac{1}{(2k+1)^2} \\ &\left(\text{sinc}^2\left(\frac{((2k+1)f_{ck} - f + j2f_{ck})\pi}{2f_{cm}}\right) + \right. \\ &\left. \text{sinc}^2\left(\frac{((2k+1)f_{ck} + f - j2f_{ck})\pi}{2f_{cm}}\right)\right) \end{aligned} \tag{19}$$

The noise contribution of the CMFB circuit (19) is displayed in Fig. 9. The displayed graphs are normalized with the chopping frequency f_{ck} (x axis) and with the noise power (y axis) to have an unity integrated noise power ($RMS^2 = 1$). The parametric analysis in function of the common-mode frequency shows in particular that the f_{cm} frequency should be an even divider of the auto-zero frequency. If the signal bandwidth is located in much lower frequencies than the chopping one, the most suitable value is half of the chopper frequency, $f_{cm} = f_{ck}/2$.

The $C_{G,cm}$ capacitances should also be minimized to reduce their contribution to the noise of the auto-zero amplifier. Compared to the global noise budget, the contribution of these capacitors can be made negligible.

Integrator CMFB: The input common-mode of the integrator, Fig. 10, is set by a similar structure than the one for

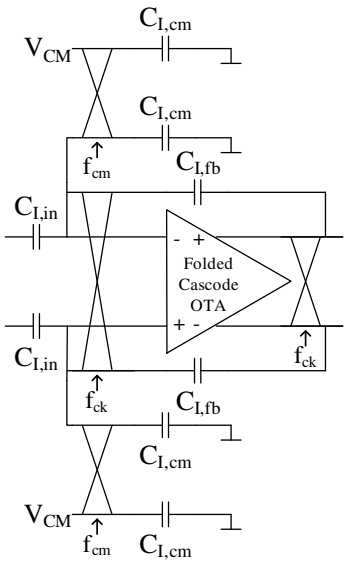

Fig. 10. Integrator input CMFB.

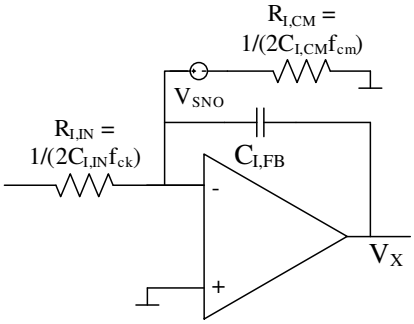

Fig. 11. Simplified (single ended) continuous-time representation of the noise contribution of the CMFB circuit in the integrator.

the gain stage, but the common-mode capacitors $C_{I,cm}$ are connected to the ground instead of a connection to the output nodes.

As in the gain stage, the noise is first sampled on the capacitors $C_{I,cm}$, and thus a continuous-time representation of the integrator can be derived, Fig. 11. As the noise is sampled, the noise power, $N_{RMS} = kT/C$, is folded into the choppers frequency band. The equivalent noise spectral density is thus, assuming an uniform distribution:

$$NSD_{V_{SNO}} = \frac{2kT}{C_{I,cm} f_{cm}} \tag{20}$$

The transfer function of the sampled noise source to the output of the integrator is:

$$H(j\omega) = \frac{V_X}{V_{SNO}} = \frac{2C_{I,cm} f_{cm}}{j\omega C_{I,fb}} \tag{21}$$

and the output-referred noise spectral density is:

$$\begin{aligned} NSD_{OUT,I,CM} &= V_{SNO} \left| H(j2\pi f) \right|^2 \\ &= \frac{2kTC_{I,cm} f_{cm}}{(\pi f)^2 C_{I,fb}^2} \left[\frac{V^2}{Hz} \right] \end{aligned} \tag{22}$$

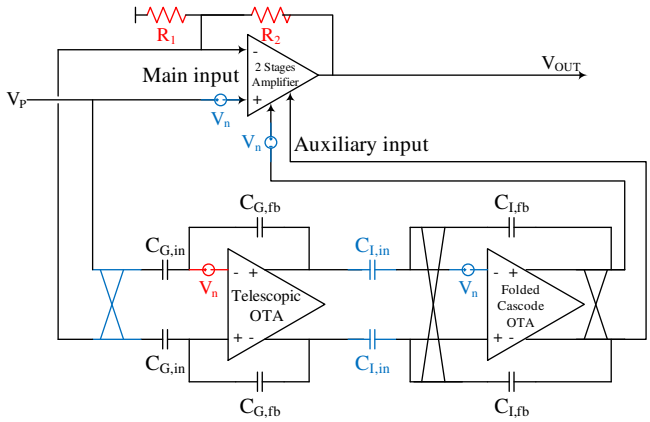

Fig. 12. Auto-zero main noise sources.

The input-referred noise spectral density is obtained, dividing the output-referred NSD by the transfer function of the integrator and by the gain of the first stage. In the signal baseband (around f_{ck}, as the signal is chopped), the input-referred noise spectral density is:

$$\begin{aligned} NSD_{IN,I,CM} &= NSD_{OUT,I,CM} \left(2\pi f R_{I,in} C_{I,fb}\right)^2 \frac{C_{G,fb}^2}{C_{G,in}^2} \\ &= \frac{2kTC_{I,cm} f_{cm}}{C_{I,fb}^2 f_{ck}^2} \frac{C_{G,fb}^2}{C_{G,in}^2} \left[\frac{V^2}{Hz} \right] \end{aligned} \tag{23}$$

This last equation shows that the noise contribution of the CMFB circuit of the integrator can be reduced without increasing the power consumption. The most straightforward way to minimize this noise contribution is to decrease the $C_{I,cm}$ capacitance.

E. Noise Analysis – Summary

To summarize, it is possible to sort the noise sources into two categories. The first ones, shown in red in Fig. 12 have a direct impact on the power consumption. These sources are:

- the thermal noise of the gain stage,
- the noise in the feedback resistors of the main amplifier.

The noise contribution of the second type of sources, in blue in Fig. 12, can be lowered without increasing the consumption:

- using an auxiliary chain for the main amplifier noise,
- lowering the switches resistor of the auxiliary chain input chopper,
- increasing the closed loop gain of the gain stage to reduce the sampled noise created on the input capacitors $C_{I,in}$ of the integrator (a high gain in the first stage also lowers the thermal noise contribution of the integrator),
- using frequency modulation to shift the flicker noise of the amplifiers of the auxiliary chain outside the baseband.
- setting the frequency of the input common-mode control of the gain stage to half of the chopping frequency.
- decreasing the switched capacitances of the CMFB circuits in the gain stage and in the integrator.

VI. Power Consumption

The previous analysis has shown that most of the power consumption should be used in the gain stage and in the feedback resistors. The amplitude at the main amplifier output is proportional to the input signal and to the amplifier closed-loop gain. In order to relax the requirements on a next stage (typically, an ADC), the full output range should be used. In order to explore the noise versus supply current trade-off, the current flowing into the resistors is evaluated here considering an output range covering half of the power supply voltage:

$$I_{R,max} = \frac{V_{DD,max}}{4R} \tag{24}$$

assuming a common-mode centred in the middle of the power supply. The input-referred noise spectral density of the resistors in the signal baseband is:

$$NSD_{R,IN,baseband} = \frac{4kTR(G-1)}{G^2} = \frac{kTV_{DD}}{I_R}\frac{G-1}{G^2} \tag{25}$$

This result, combined with the noise spectral density defined for the gain stage in section V-C (7), allows a sizing of the resistors and of the gain stage equalizing their respective noise-consumption ratio:

$$\frac{NSD_{R,IN,baseband}}{I_R} = \frac{NSD_{IN,gain\_stage}}{I_{0,gain\_stage}} \tag{26}$$

For the specific implementation simulated in the next section, a theoretical current consumption of $50 - 120\mu A$ is found for a noise spectral density of $75(nV)^2/Hz$. The noise contribution of the integrator (8) is $7(nV)^2/Hz$.

VII. Simulations and Results

This chapter presents the verification of the previous noise analysis using simulation tools. Classically, AC simulations are used to check the noise level of a circuit. These simulations provide extremely rapidly a frequency response of a noisy circuit. AC simulations are based on the fact that the system to analyse is linear around a given operating point as long as the variation of the signal is not significant (small signal hypothesis). It is not possible to use such AC simulations to validate the auto-zero amplifier, because it uses a frequency shift and is non-linear.

Two different types of simulation are thus used to check the noise level of the circuit. Firstly, AC simulations are used as much as possible inside the blocks of the auto-zero amplifier. It is possible to extract data on the noise level of the different blocs, as the low-frequency noise of the main amplifier (Fig. 13) or the noise level of the gain stage around the chopper modulation frequency (Fig. 14).

Secondly, to simulate the full system, transient simulations are used. The noise contribution of each component (transistors and resistors) is added by the transistor level simulator. The spectrum of each generated noise source is continuous (the noise model used is not a finite sum of sine waves at discrete frequencies).

The noise spectral density in the baseband is extracted from the discrete Fourier transform of a noisy transient signal of length T_{sim}. As a front-end is expected to be followed by an analog to digital converter, the output noise is sampled to take aliasing into account.

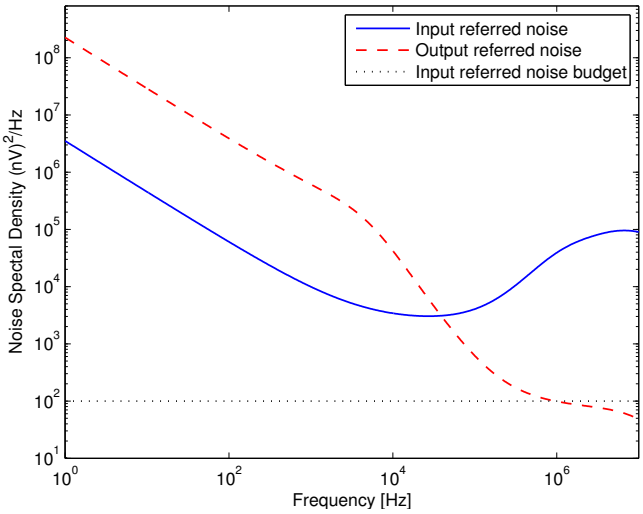

Fig. 13. Main amplifier noise.

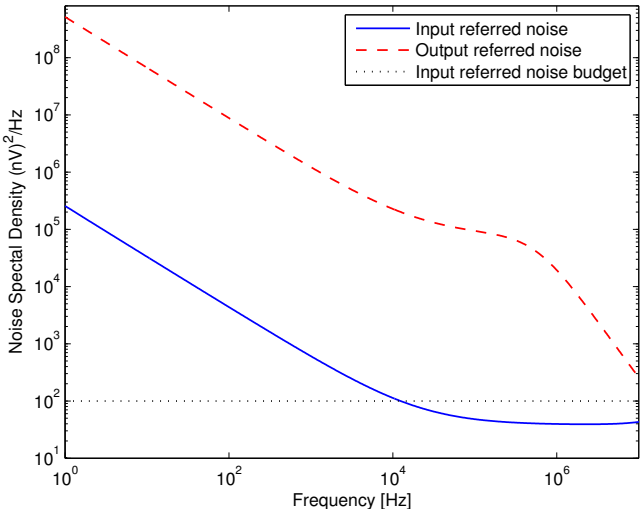

Fig. 14. Gain stage noise.

$$NSD_{output} = FFT(V_{out(t),sampled})\frac{1}{\Delta f}\left[\frac{V^2}{Hz}\right] \tag{27}$$

The input-referred noise at the input of the auto-zero amplifier is given by:

$$NSD_{input} = FFT(V_{out(t),sampled})\frac{1}{G^2}\frac{1}{\Delta f}\left[\frac{V^2}{Hz}\right] \tag{28}$$

where Δf is the interval between each spectral line of the discrete Fourier transform. The spectral resolution is given by the inverse of the simulation time: $\Delta f = 1/T_{sim}$.

The simulation results are given for the thermal noise and for the flicker noise in Fig. 15.

Table I shows the extracted noise levels in the baseband frequency and provides a comparison with the noise levels of the main amplifier and of the auxiliary chain's gain stage.

As expected, the flicker noise level is much lower than the thermal noise. The 1/f noise contribution to the global

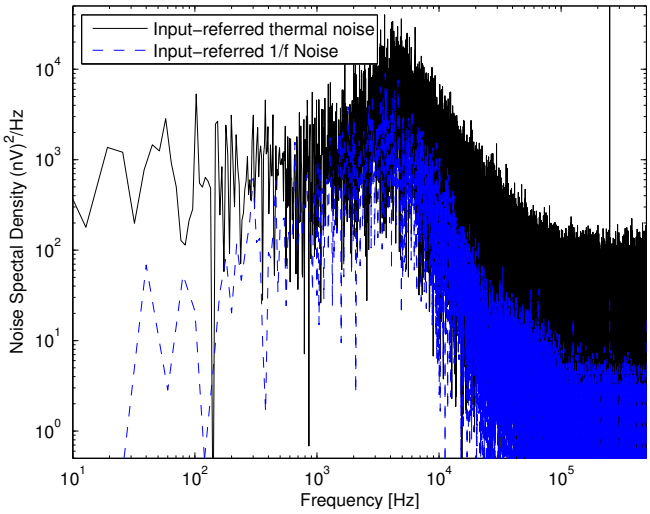

Fig. 15. Input-referred thermal and flicker noise of the amplifier.

TABLE I
NOISE SUMMARY AND AMPLIFIER KEY CHARACTERISTICS

Noise level	Theory	Simulated	Unit
Flicker	–	$<$ 1 at 12 Hz	$(nV)^2/Hz$
Thermal	75	180 at 12 Hz	$(nV)^2/Hz$
Main Amplifier at 100Hz	–	$>$ 60k	$(nV)^2/Hz$
Gain Stage at f_{ck}	45	47	$(nV)^2/Hz$
Power consumption	50	85	μA
Sensor output current	3	–	pA

noise budget (Table I) is negligible. The power consumption is higher than predicted, as the supply current of the main amplifier, of the integrator and of the bias generation was not taken into account in the simplified analysis.

VIII. CONCLUSION

This paper introduced a novel topology for low-noise low-power continuous-time instrumentation amplifier for sensor with limited output current. Both auto-zeroing and chopper techniques were exploited to define an architecture with a symmetrical behaviour in both phases, reducing constraints on amplifiers. The noise contribution of each block was analysed and a noise-to-supply current ratio was derived. The circuit performance was validated using transistor level simulations.

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