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VHDL-Ams Model of the Integrated Membrane Micro-Accelerometer with Delta-Sigma (Δσ) Analog-To-Digital Converter for Schematic Design Level

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Abstract. VHDL-Ams model of integrated membrane type micro-accelerometer with delta-sigma (ΔΣ) analog-to-digital converter for schematic design level was developed. It allows simulating movement of the sensitive element working weigh from the applied acceleration, differential capacitor and original signal capacity change, signal digitizing with the help of Delta-Sigma ADC with defined micro-accelerometer structural parameters, and analyzze an integrated device at the schemotechnical design level.

Key words: Micro-Electro-Mechanical Systems (MEMS), micromechanical sensitive element, integrated membrane micro-accelerometer, delta-sigma modulation, pulse-width modulation (PWM), delta-sigma analog-to-digital converter (ADC), one bit digital-to-analog converter (DAC), VHDL-AMS hardware description language, hAMSter software, schemotechnical design level.

INTRODUCTION

Integrated micro-accelerometers (Microelectromechanical inertial sensors) are devices for linear accelerations measuring (static, for example, local Earth gravitational field and dynamic caused by motion or stroke), which appeared due to development of micromachine (MEMS) technologies [1-3]. Nowadays integral micro-accelerometers [2, 4, 6] are widely used in different technology areas such as: car industry, (antiblocking and the antiskiding systems, active suspension bracket systems, theft defense systems), robotics, inertial navigation, domestic appliances (computer manipulators, smart phones, tablets), sports equipment (training equipment, pedometers), geophysical applications, aerospace industry, medical systems, navigation and others. Integrated accelerometers have the following types depending on the acceleration registration way: with the sensitivity axis perpendicular to the integrated device substrate (out-of-plane accelerometers) these include membrane type accelerometers; with plane registration (in-plane accelerometers) - accelerometers which have pectinated design, their sensitivity axis is parallel to the integrated device substrate. Accelerometers are also categorized by the external input acceleration registration mechanism, namely: capacitive, piezoresistive, piezoelectric, magneto-resistive, tunneling, optical, based on heat transfer, based on Hall effect, thermal, interferometric, etc. The membrane accelerometer with capacitive mechanism of external input acceleration registration was chosen for the investigation due to its simplicity, large manufacturing technology scale, high sensitivity and wide range of application.

Depending on the implementation areas companies design and manufacture accelerometers with different technical characteristics [3, 6, 7]. Among these characteristics are the following: measuring range, sensitivity, resolution, size, price – these are only some of the factors that determine their future application. Design and improvement of the integrated micro-accelerometers with the necessary technical and operational characteristics oversee creation of the behavioral models using the following hardware description languages – VHDL-AMS, Verilog-AMS [8 – 12] with the help of specialized software, for example, Virtuoso AMS Designer (developed by American company Cadence Design Systems), SystemVision (by American corporation Mentor Graphics), hAMSter (by Ansoft Corporation), SMASH Mixed-Signal Simulator (by French corporation Dolphin Integration) and others [13 – 18].

Therefore, development of the behavioral patterns using VHDL-AMS and Verilog-AMS languages which intends to describe such complex heterogeneous systems as integral micro-accelerometers is an actual task for their efficient design.

WOKING PRINCIPLE AND MATHEMATICAL MODEL OF THE INTEGRAL MEMBRANE MICRO-ACCELEROMETER

Fig. 1 shows the model of a micromechanical sensitive element (SE) for integrated membrane micro-accelerometer. [2]. micromechanical SE consists of the working weight and elastic elements that connect it with the integrated device substrate (fig. 2). External acceleration displaces the micromechanical sensitive element working weight from the equilibrium position. This displacement magnitude is proportional to the acceleration magnitude and inversely proportional to the elastic elements stiffness. Thus, the input sensor acceleration is converted into displacement of the sensor SE working weight. The cover (lid), lining and working weight from both sides of the integrated device is covered

with electrodes, which form differential capacitor binding. The created capacitor capacity changes with the working weight movement caused by the applied acceleration. Further on the capacity changes are logged and can be converted into voltage, frequency, current, or PWM signal with the use of according electric circuits [19]. As a rule, after conversion the signal is digitized using precision ADCs, which subsequently allows its investigation with a specialized microprocessor or microcontroller.

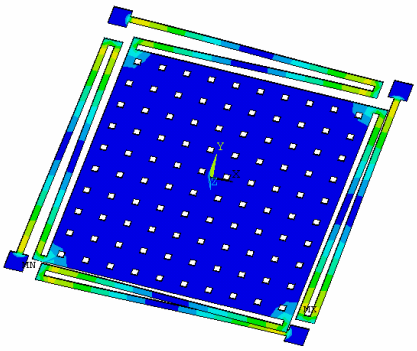

Fig. 1. Model of a micromechanical SE for integrated membrane micro-accelerometer

Movement of the integrated membrane micro-accelerometer can be described with following differential second-order equation:

$$M\frac{d^2x(t)}{dt^2}+D_x\frac{dx(t)}{dt}+K_x x(t)=F_{ext}\,, \quad (1)$$

where: M – sensitive element weight, D_x – attenuation coefficient, K_x – resilience coefficient, $x\ (t)$ –sensitive element movement along the x axis direction. $F_{ext} = M \cdot a_{ext}$, where a_{ext} – external acceleration [20, 21].

Measuring capacitors (C_1, C_2) are used for recording sensitive element movements are shown in Fig. 2. Their capacities vary depending on the external acceleration.

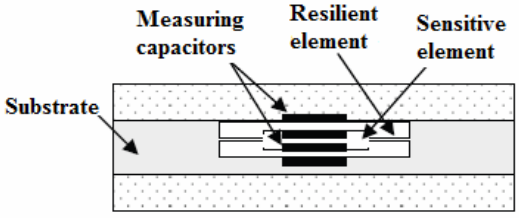

Fig. 2. Schematic view of the MEMS membrane accelerometer design

Capacities C 1 and C 2 of the differential capacitor can be calculated in the following way:

$$C_1=\frac{\varepsilon_0 A}{\delta-x}, \qquad C_2=\frac{\varepsilon_0 A}{\delta+x}, \quad (2)$$

where: A – membrane area; ε_r – dielectric environment penetrability between the capacitor electrodes; ε_0 – dielectric vacuum penetrability; δ – distance between the capacitor plates in case of external acceleration absence $a_{ext} = 0$; x – movement of the SE working weight.

Since:

$$C_1-C_2=\frac{2\varepsilon_0 Ax}{\delta^2-x^2}, \; C_1+C_2=\frac{2\varepsilon_0 A\delta}{\delta^2-x^2}. \quad (3)$$

Then the output signal value V_{out} is proportional to the carrier frequency and displacement of the SE working weight, when $a_{ext} = 0$ ($c_1 = c_2$, $V_{out} = 0$) and inversely proportional to the working weight displacement:

$$V_{out}=V_{sample}\left(\frac{x}{\delta}\right). \quad (4)$$

THE WORKIN PRINCIPLES AND BASIC TOPOLOGY OF THE DELTA-SIGMA ADC

Delta-Sigma analog-to-digital converters are perfect solution for signals conversion, for example once taken from inertial sensors in a wide range of frequencies from zero to several megahertz with a very high resolution [22 - 26]. Figure 3 shows the basic topology (core) of the Delta-Sigma ADC, it consists of the internal Delta-Sigma modulator consistently joined with the digital filter. Role of the Delta-Sigma ADC input signal is taken by constant or variable voltage. Input signal is signal taken from the integral micro-accelerometer SE. The internal modulator converter, shown in Fig. 3, samples the input signal, transforming it into a discrete output signal, using 1-bit ADC. The modulator converts the analog input signal into a high speed pulses sequence. Units to zeros appear in this pulses sequence corresponds to the input analog voltage size. Modulator actually returns noisy signal. This noise is created by the electrical circuit in the high-frequency region of the output signal spectrum. This enables getting transformation results with high resolution and low noise levels from the digital filter output. At the modulator output the digital filter generates high discretization frequency data from the high-frequency noisy signal. Since now this signal is digital the lower frequencies digital filter can be used for further suppression of high-frequency noise, and the filter/decimator can be applied to reduce data output frequency. Collectively, digital filter/decimator and modulator flow filters create from 1-bit codes slower sequence of multibit codes. Although most of transducers have only one discretization frequency, Delta-Sigma transducers have two: input discretization frequency and output data delivery frequency. The ratio of these two frequencies determines the system decimation coefficient. There is a strong dependence between the decimation coefficient and converter effective capacity [27-29].

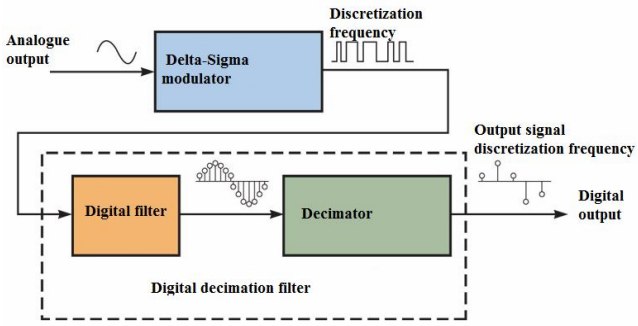

Fig. 3. Basic functional core of the Delta-Sigma ADC – Delta-Sigma modulator and digital filter/decimator

Delta-Sigma converter uses a large number of the modulator generated pulses for creating 1-bit codes sequences. In Delta-Sigma ADC this task is performed by the input signal quantization device of high frequency. In analogue to other quantization devices, Delta-Sigma modulator accepts an input signal and produces a numeric values sequence that reflects the input voltage value. The modulator performance can be observed from both time and frequency ranges. Time range allows illustrating operation principle of the first order modulator (fig. 4). The modulator measures difference between analog input signal and analog DAC reverse output signal. Then the integrator handles the original analog subtraction voltage and passes the signal to the 1-bit ADC. Single ranged ADC converts the integrator output signal into one unit or zero. Using the system stroke generator the ADC sends the 1-bit digital signal to the modulator output, and back by the feedback connection chain to the input of 1-bit DAC.

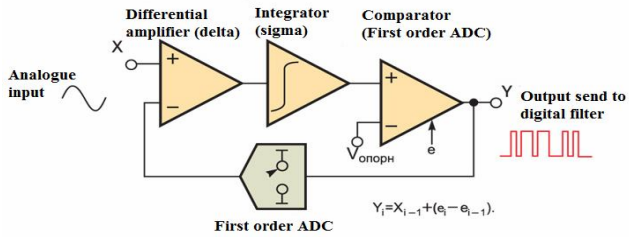

Fig. 4. Presentation of the first order modulator performance in time range

1-bit ADC converts the signal into the source code which also contains noise quantization (ei). Signal at the modulator output equals to the sum of input signal and quantization noise (ei-ei-1). As can be seen form the formula, quantization is represented by difference between the current (ei) and previous (ei-1) modulator faults. The output signal in the time range is a reflection of the input signal in form of pulses sequence with a discretization frequency, fS. If to average the output pulses string the input signal value can be got. The frequency range chart reveals the other side of the process (fig. 5). The time range output signal pulses in frequency range look as the input signal and noise, which has a characteristic shape. The noise characteristics in fig. 5 allow understanding the modulator performance in the frequency range. The noise spectrum at the modulator output is not flat. The most important fact in its frequency analysis is that the modulator generates noise in the high frequencies range making it easier to get high resolution results. The modulator output signal in Fig. 5 shows how modulator quantization noise, starting almost from zero frequency, fast grows and then leveled to maximum values at the of modulator frequency. The double integration with the use of the second order modulator is a better way to minimize low- quantization frequency noise comparing with single integration.

The digital filter suppresses noise and the decimator reduces output data frequency. In Delta-Sigma frequency after the modulator there is digital filter/decimator chain. It collects and filters sequence of 1-bit codes taken from the modulator output. There is an issue in high-frequency noise and high modulator source signal discretization frequency. Since now this signal is digital the digital filter function can be used for noise suppression, and the filter/decimator function can be applied to reduce data delivery frequency. These two functions are often combined into one module. Fig. 6 (a, b, c) shows how the signal passes through the digital filter/decimator. The digital filter performance occurs at the same frequency, as modulator discretization (fig. 6).

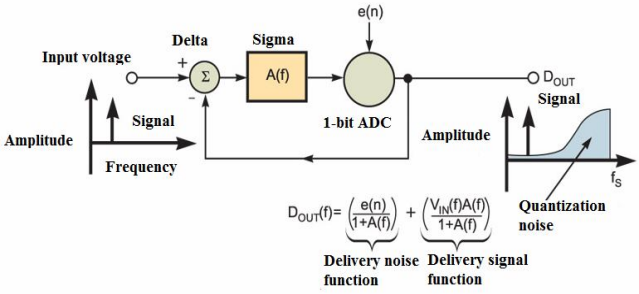

Fig. 5. Noise frequency characteristics are the key to the modulator performance representation at frequency the range

The digital filtering function provides digital representation of the input signal, however the data delivery frequency is still too high for practical application. While it may seem attractive to have a large amount of high quality multi-bit samples, produced with high discretization frequency, most of the data in this array is redundant. The second function of a digital filter/decimator is decimation (thinning). Decimation is frequency reduction of the digital signal delivery to Nyquist system frequency.

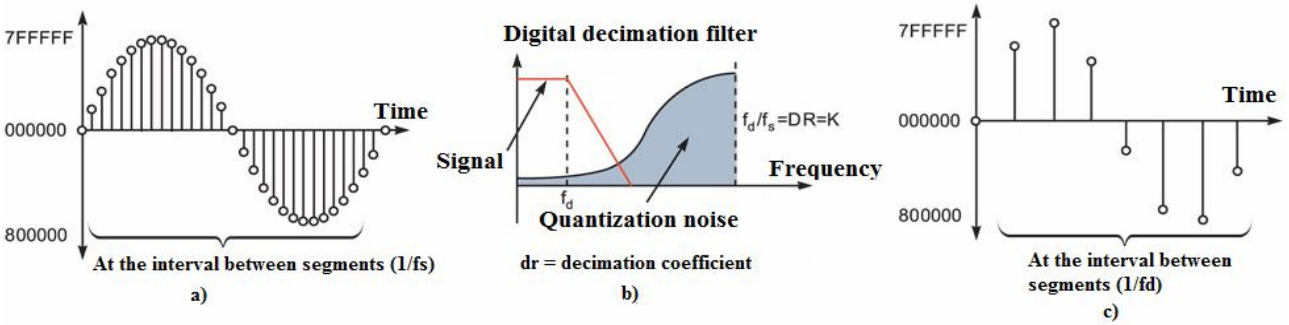

Fig. 6. The digital filtering function provides high resolution of the output data result (a) suppressing high frequency noise (b), the decimation function reduces the data delivery frequency (c)

One of the simple ways to realize decimation is to average 24-bit codes (fig. 6c). Decimator accumulates high resolution data words, averages them, gives averaging result and resets the accumulated data for the next average. More economical way of the decimation function low cost implementation is simple choice of 24-bit words from each K segment without its averaging (K is the decimation or thinning coefficient). Almost all of the Delta-Sigma converters contain averaging filters such as Sinc or FIR-filters (CIX-filter). A lot of Delta-Sigma devices use other filters together with Sinc-filters to ensure two staging decimation. In case of low-speed industrial Delta-Sigma ADC only Sinc filter is typically used. From the frequency range it can be seen that digital filter/decimator carries out only law frequency filtering of the signal (fig. 6 b). Meanwhile this digital filter/decimator suppresses high frequency quantization noise formed by the modulator. After the quantization noise suppression by filtering the signal develops over again in the time range.

VHDL - AMS INTEGRAL MEMBRANE MICRO-ACCELEROMETER WITH DELTA-SIGMA ADC

MEMS Design at the schemotechnical level oversees development of behavioral models. The fact that such models contain data from different areas of science and technology is their characteristic feature. In particular, in the integral membrane micro-accelerometer model contains mechanics, electricians and electronics values. The extension of the standard hardware description language (HDL) VHDL to VHDL-AMS allowed describing digital, analog, and mixed models of devices, which use not only electrical signals but also optical, chemical, thermal, mechanical and others [8-13]. Figure 7 shows a listing snippet of the behavioral model of the integral membrane micro-accelerometer with Delta-Sigma analog-to-digital converter developed in VHDL – AMS.

SIMULATION RESULTS AND THEIR ANALYSIS

The developed model simulations results conducted with the use of hAMSter software are graphically displayed in fig. 8-9. From the results it can be seen that the digitized signal varies in the range from 0 to 1.25 V. Further on the digital signal can be moved to processing by a specialized microcontroller or microprocessor.

```
...
architecture behav OF sdm2 IS
   terminal a1o : electrical;          terminal a2o : electrical;  terminal inter1o : electrical;
   terminal inter2o : electrical;    signal Qo : bit;     signal Q : bit;     terminal DACo : electrical;
begin
  ADDER1: entity adder generic map (A => 5.0, B => -5.0)
        port map (input1 => vin, input2 => DACo, output => a1o);
  INTER1: ENTITY inter PORT MAP(input => a1o, output => inter1o);
 --adder2 : entity adder generic map (A => 5.0, B => -5.0)
 --        port map (input1 => inter1o, input2 => DACo, output => a2o);
 --inter2 : entity inter port map (input => a2o, output => inter2o);
  Q: entity quantizer generic map (threshod => 0.0)
     port map (clk => clk, input => inter1o, output => Qo);
  D_FLIP_FLOP: entity d_ff_srss port map (d => Qo, clk => clk, reset => '0', set => '0', q => Q);
  DAC: entity DAC generic map (max => 5.0, min => -5.0)
      port map (input => Qo, output => DACo);   output <= Qo;
end architecture behav;
-- Testbench of Sigma-Delta Modulator
library ieee, disciplines;
use disciplines.electromagnetic_system.all; use ieee.math_real.all; use ieee.std_logic_1164.all;
entity t_sdm2 is end entity t_sdm2
architecture bhv of t_sdm2 is
   terminal A : electrical;
   --quantity xin across iin through A to electrical_ground;
   signal op : bit;     signal clk : bit; --std_logic;        quantity v across A to electrical_ground;
begin
   CLK: entity clock(v1) generic map (5us) port map (clk);
  --  xin == 5.0*sin(math_2_pi*1.0e6*NOW);
   --UUT1: entity Vsine(v1) generic map (Va => 5.0, freq=> 1.0e6) port map (A, electrical_ground);
   ACCEL: entity mems_accelerometer(top_level) port map(A);
   M_SDM2: entity sdm2 port map(vin => A, clk => clk, output => op);
end architecture bhv;
```

Fig. 7. Fragment of the behavioral model of the integral membrane micro-accelerometer with Delta-Sigma analog-to-digital converter

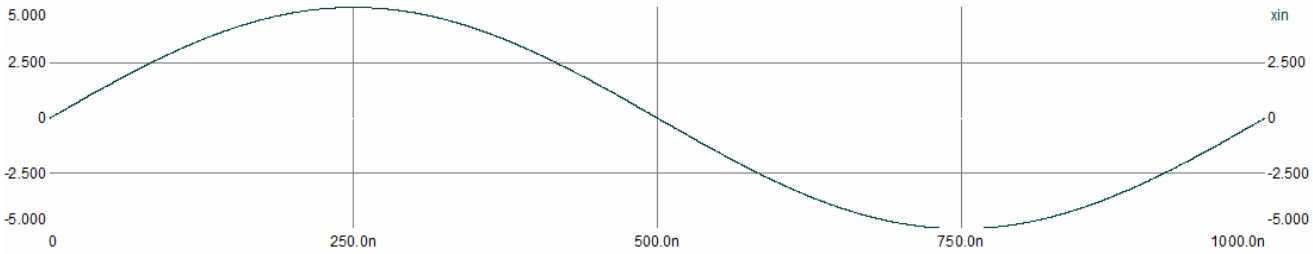

Fig. 8. The measured sensor analog signal (in case of sinusoidal change) resulted from the applied external acceleration aext

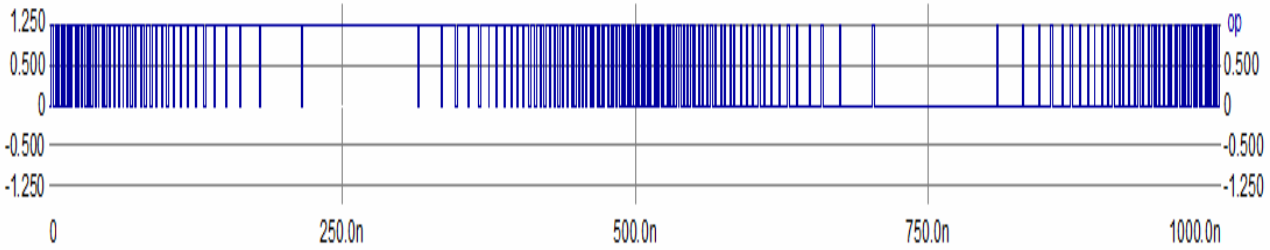

Fig. 9. The bits flow in the digitized sensor signal at the Delta-Sigma analog-to-digital converter output

CONCLUSIONS

The proposed VHDL-AMS membrane micro-accelerometer with Delta-Sigma analog-to-digital converter model allows simulating movement of the sensitive element working weigh from the applied acceleration, differential capacitor and original signal capacity change, signal digitizing with the help of Delta-Sigma ADC with defined micro-accelerometer structural parameters, and analyze an integrated device at the schemotechnical design level.

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REFERENCES

1. **Yazdi N., Ayazi F. and Najafi K. 1998**. Micromachined inertial sensors, Proc. IEEE, vol. 86, no. 8, 1640-1659.

2. **Maluf N. and Williams K. 2004.** An Introduction to Microelectromechanical Systems Engineering. Artech House Inc. 305 p.

3. **Teslyuk V., Pereyma M., Denysyuk P., Chimich I. 2006.** Computer-aided system for MEMS design “ProMIP”. Proc. of the 2nd Inter. Conf. of Young Scientists on Perspective Technologies and Methods in MEMS Design, MEMSTECH 2006, Lviv–Polyana, Ukraine, 49-52.

4. MEMS & Sensors for Mobile Phones and Tablets, 2014. Yole Developpment. 22.

5. **Akila Kannan. 2008.** Design and Modeling of a MEMS-Based Accelerometer with Pull In Analysis. Thesis, University of British Columbia, 149.

6. **Teslyuk V., Kushnir Y., Zaharyuk R. and Pereyma M. 2007.** A Computer Aided Analysis of a Capacitive Accelerometer Parameters. Proceeding of the 9th International Conference on The Experience of Designing and Application of CAD Systems in Microelectronics, CADSM’2007, Lviv – Polyana, Ukraine, 19-24 Feb. 548 – 550.

7. **Teslyuk V., Al Omari T., Alshavabkekh H., Denysyuk P. and Melnyk M. 2007**. Computer-Aided Design of MEMS at system level. Machine Dynamics Problems, Vol.31, 92 -104.

8. Standard VHDL Analog and Mixed-Signal Extensions. 2003. Packages for Multiple Energy Domain Support. 21.

9. **Ashenden P.J. 2004.** EDA CONSULTANT, ASHENDEN DESIGNS PTY. Elsevier Science, 84.

10. **Pavel V. and Richard Shi C.-J. 2005**. VHDL-AMS based modeling and simulation of mixed-technology Microsystems. 261.

11. Verilog-AMS Language Reference Manual Analog & Mixed-Signal Extentions to Verilog-HDL, Version 2.1. 2003. 279.

12. **Zaharyuk R., Teslyuk V., Farmaga I. and AlShawabkeh H.A.Y. 2008.** VHDL-AMS – Model for capacitive interdigital accelerometer. Proceeding of the 4th International Conference of Young Scientists on Perspective Technologies and Methods in MEMS Design, MEMSTECH, Lviv-Polyana, Ukraine. 134-137.

13. Virtuoso AMS Designer. Available online at <http://www.cadence.com/products/cic/ams_designer/pages/default.aspx>.

14. SystemVision. Available online at <http://www.mentor.com/-products/sm/system_integration_simulation_analysis/systemvision/>.

15. hAMSter Software for VHDL-AMS Simulations. Available online at <http://www.theoinf.tu-ilmenau.de/~twangl/VHDL-AMS_online_en/Home.html>.

16. SMASH Mixed-Signal Simulator. Available online at <http://www.dolphin.fr-/index.php/eda_solutions/products/smash/overview>.

17. **Napieralski A., Napieralska M., Szermer M. and Maj C.** 2012. The evolution of MEMS and modeling methodologies, COMPEL. The International Journal for computation and Mathematics in Electrical and Electronic Engineering. Vol.31, 1458 – 1469.

18. **Augustyniak I., Knapkiewicz P. and Dziuban J. 2012.** Modeling and tests of silicon-glass structure of dose high-energy radiation MEMS sensor. PRZEGLĄD ELEKTROTECHNICZNY. Vol.11b, 272-274.

19. **Fraden J**. **2010.** Handbook of Modern Sensors. Physics, Designs, and Applications (Fourth Edition). Springer Science+Business Media. 681.

20. **Kempe V.** 2011. Inertial MEMS Principles and Practice. Cambridge University Press. 492.

21. **Pelesko J. A. and Bernstein D. H. 2002.** Modeling MEMS and NEMS. Chapman & Hall/CRC. 384.

22. **Baker B. 2011.** How delta-sigma ADC work, Part 1. Texas Instruments Incorporated. Analog Applications Journal. 6.

23. **Baker B. 2011**. How delta-sigma ADC work, Part 2. Texas Instruments Incorporated. Analog Applications Journal. 5.

24. **Reiss J. D**. 2008. UNDERSTANDING SIGMA–DELTA MODULATION: The Solved and Unsolved Issues. – J Audio Eng. Soc., Vol. 56, No. 1/2. 16.

25. **Kozak M. and Kale I. 2003.** Oversampled Delta-Sigma Modulators: Analysis, Applications and Novel Topologies. Kluwer Academic Publishers, Dordrecht, The Netherlands.

26. **Zhao C. and Kazmierski T. 2007.** An efficient and accurate MEMS Accelerometer Model with sense finger dynamics for mixed-texnology control loops. IEEE Behavioral Modeling and Simulation Conference (BMAS), sep. 2007, San Jose, California, USA. 143 – 147.

27. **Bourdopoulos G. I., Pnevmatikakis A., Anastassopoulos V. and Deliyannis T. L. 2003**. Delta-Sigma Modulators: Modeling, Design and Applications. Imperial College Press, London, UK.

28. **Jespers P. A. G. 2001.** Integrated Converters: D to A and A to D Architectures, Analysis and Simulation. Oxford University Press, Oxford, UK.

29. **Schreier R. and Temes G. C. 2005.** Understanding Delta-Sigma Data Converters. John Wiley and Sons, Hoboken, NJ, USA.