Krzysztof RÓŻYC, Paweł KWIATKOWSKI, Marek SAWICKI, Zbigniew JACHNA, Ryszard SZPLET
MILITARY UNIVERSITY OF TECHNOLOGY, DEPARTMENT OF ELECTRONICS
2 Gen. S. Kaliskiego St., 00-908 Warsaw, Poland

A multichannel programmable distribution amplifier

Abstract

This paper presents the design, operation and test results of a multichannel programmable distribution amplifier. The distributor is based on a reprogrammable device Spartan-6 FPGA (Xilinx) and is intended to distribute a 10 MHz or 5 MHz frequency reference signal as well as 1 PPS pulses. It is built in a 2U, 19" rack-mount enclosure and is equipped with a single optical and seven electrical inputs, as well as two optical and fourteen electrical outputs The transition time and additive jitter of the distribution amplifier were tested and they did not exceed 14 ns and 4.5 ps RMS (for electrical inputs/outputs), respectively. In the case of optical input/outputs, the results depend on the parameters of converters involved. The values of delays and jitter introduced by the distributor are slightly larger than for dedicated integrated circuits, but the advantage of this solution is the possibility to build signal distributors with a larger number of inputs/outputs and the ease to modify and meet requirements of various applications.

Keywords: programmable device, distribution amplifier.

1. Introduction

Distribution amplifiers are used to deliver a reference signal of different forms to a number of receivers possibly without degradation of the signal. The presented multichannel programmable distribution amplifier is based on a Spartan-6 FPGA (Field Programmable Gate Area) device and is intended to distribute a 10 MHz or 5 MHz frequency reference signal (e.g. from any atomic clock or other reference source of excellent frequency stability) as well as 1 PPS (Pulse Per Second) pulses. Such frequency reference sources are used as timebase clocks for instruments involved in tests and measurements, broadcasting, telecommunication, nuclear science or basic research applications. A distribution amplifier in these applications should provide a very low additive jitter and a short transition time. There are only a few manufacturers, which offer such type of devices, e.g. Microsemi [1] and Stanford Research Systems [2].

2. Construction

The designed distribution amplifier is equipped with a single optical input and seven electrical inputs, as well as two optical and fourteen electrical outputs (Fig. 1). All the electrical inputs and outputs are on SMA connectors.

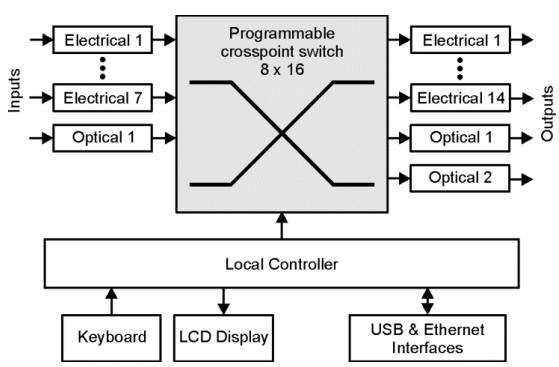


Fig. 1. Block diagram of the programmable distribution amplifier

The electrical inputs accepts sinusoidal or square waveform input signals of an amplitude within the range of ± 4 V. Each input has a 50 Ohm input impedance. All input signals are conditioned by fast comparators with adjustable trigger level. The design of optical input is based on an integrated optical receiver module HFBR-2316TZ (Avago). The receiver contains an InGaAs PIN photodiode and a low-noise transimpedance preamplifier that operates within the 1300 nm wavelength region. It receives an optical signal and converts it to an analog voltage. The buffered output is an emitter-follower, with the frequency response from DC up to 125 MHz. The electrical output signal is subsequently conditioned by a fast comparator.

The main module of the distribution amplifier is a programmable crosspoint switch. In general, several integrated circuits, such as ADN4604 or AD8150 (Analog Devices), can perform this function, but in order to increase the flexibility of the device and to reduce its cost, the general-purpose reprogrammable device Spartan-6 (Xilinx) can also be applied. The FPGA chip provides great flexibility in assigning input and output ports, which greatly facilitates the design of a printed circuit board. Moreover, signals can be conducted through wires on a PCB in a differential standard (LVPECL for input and LVDS for output signals). That makes them more resistant to distortion and in that way, reduces the risk of crosstalk. The crosspoint switch applied in the chip is controlled via an SPI interface. The configuration data are transmitted in the form of 72 bit words, where each first byte is a command, and the rest is a control word. Five commands and two control registers are involved. The first register is responsible for crosspoint switching, while the second one for activating outputs or setting them into high impedance state. The commands are used to set registers, read their actual state or reset the device.

All outputs of the amplifier are driven by separate fast output drivers to provide high electrical isolation and possible short rise and fall times of pulses. The design of optical outputs is based on an integrated optical transmitter module HFBR-1312TZ (Avago).The module converts an electrical signal from the crosspoint switch to its optical equivalent. The fiber optic transmitter contains a 1300 nm InGaAsP light emitting diode capable of efficiently launching optical power into a 50/125 μm and 62.5/125 μm diameter fiber. This allows for flexibility in choosing a fiber size. The 1300 nm wavelength is in the lower dispersion and attenuation region of the fiber, and provides longer distance capabilities than 820 nm LED technology.

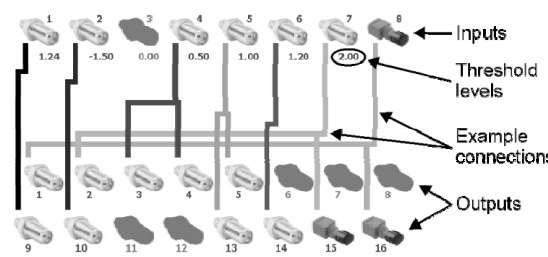


Fig. 2. Layout of the local user interface

A local controller is built based on two microcontrollers. The first one, STM32F407VGT6 (STMicroelectronic), besides controlling the crosspoint switch, is responsible for configuration through the USB and Ethernet interfaces. The primary user interface consists of an LCD display and a keyboard. It has been implemented as a subsystem and is connected to the main system by the internal UART interface. The local user interface is realized on the basis of a microcontroller STM32F429IIT6 (STMicroelectronic). It has a built-in graphical controller that provides a 24-bit parallel digital RGB signal and delivers all

signals directly to a broad range of LCD and TFT panels up to XGA resolution. Therefore, a 5" LCD panel with resolution 800 × 600 (Fig. 2) could be used in the distribution amplifier. The high enough rate with such high resolution and the need to prepare graphic elements depending on the current setup require at least the 2 MB system memory size. Therefore, the internal memory of the microcontroller is supplemented by an external DRAM memory.

The Ethernet interface allows for remote control of the distribution amplifier. Further, it is also used for updates of microcontrollers and FPGA contents. Such a process can be performed automatically, which is a valuable feature of the designed distributor, e.g. for distance recovery operation.

The designed amplifier is built in a 2U, 19" rack-mount enclosure. The local interface (keyboard and LCD display) is located on the front panel, while all signal connectors are located on the rear panel (Fig.3).

Fig. 3. The multichannel programmable distribution amplifier

3. Measurements

The parameters and implementation aspects of the designed distributor were verified in tests performed in two consecutive test setups dedicated for evaluation of: (1) transition time and additive jitter, (2) its temperature dependence.

The most important tests of the distribution amplifier concerning measurements of the pulse parameters were performed at the device outputs. The test setup is shown in Fig. 4. The test signals were generated by a pulse generator 81130 (Agilent) while a DSA70404 oscilloscope (Tektronix) was used for measurements. The chosen oscilloscope has a very low noise floor that does not exceed 340 fs, and a high precision of measurements, which is not worse than 1.48 ps for measuring delays in Delta Time mode [3].

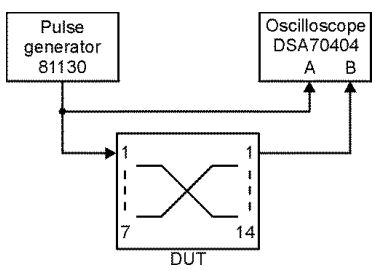


Fig. 4. Schematic diagram of the test setup 1

The pulses at the distributor outputs are characterized by the rise time t_r < 230 ps and fall time t_f < 130 ps (within the amplitude range of 20-80%) and the amplitude of 1.00 V ± 0.04 V at 50 Ohm load impedance. The measured values of delay time (Δt) and timing jitter (σ) of the signal which was attached to input 1 (IN1) and distributed to all outputs (OUT1÷OUT14) are presented in Table 1. The measurements were made at the room temperature and each obtained result was calculated as the mean value (Δt) and standard deviation (σ) of 1000 measurements.

The mean value of delay introduced by the distributor equals 13.442 ns. The spread of delays (min. 13.305 ns, max. 13.583ns) comes mainly from non-uniformity of delays of signal paths within the FPGA device that acts as the crosspoint switch. The other sources of minor importance are differences in PCB path lengths and differences in the propagation times of input comparators. The tested distributor is also characterized by the low timing jitter (below 4.5 ps RMS).

Table 2 presents the measurement results of the delays of signals attached to different inputs (IN1÷IN7) of the distributor and transmitted to one selected output (OUT1). The mean value of the delay introduced by the distributor is 13.320 ns. As previously, the spread of delays (min. 13.077 ns, max. 13.484 ns) is mainly due to the non-uniformity of delay pats within the FPGA device.

Tab. 1. Delay of the signal Δt (IN1, OUT1÷OUT14) and its timing jitter σ RMS

	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7
Δt (ns)	13.583	13.527	13.521	13.471	13.372	13.305	13.362
σ (ps)	4.08	4.20	4.14	4.07	4.12	4.00	4.22
	OUT8	OUT9	OUT10	OUT11	OUT12	OUT13	OUT14
Δt (ns)	13.401	13.430	13.402	13.344	13.539	13.499	13.439
σ (ps)	4.08	4.13	4.20	4.21	4.06	4.20	4.04

Tab. 2. Delay of the signal Δt (IN1÷IN7, OUT1) and their timing jitters σ RMS

	IN1	IN2	IN3	IN4	IN5	IN6	IN7
Δt (ns)	13.484	13.436	13.459	13.446	13.077	13.129	13.211
σ (ps)	4.16	4.06	4.20	4.01	4.00	4.07	3.97

For optical circuits (IN8, OUT15÷OUT16), each optical transmitter/receiver introduced the delay below 9 ns, and the RMS value of the timing jitter not larger than 40 ps. In this case, the results depended mainly on the parameters of electric-to-light and light-to-electric converters involved.

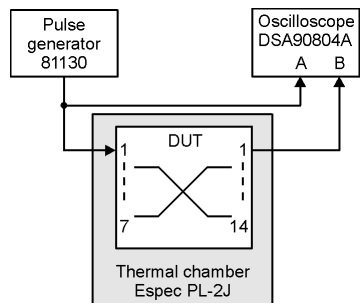


Fig. 5. Schematic diagram of the test setup 2

The next tests of the programmable distribution amplifier aimed at evaluation of its delay and timing jitter in the presence of changes in the ambient temperature. The temperature tests of the distributor were performed with the use of a thermal chamber PL-2J (Espec). The test setup is shown in Fig. 5. The temperature was varied from -10 up to +65°C. In this case, the test signals were generated by the pulse generator 81130 (Agilent) while the DSA90804A (Agilent) oscilloscope was used for measurements. The measured RMS values of delay time (Δt) and timing jitter (σ) were calculated as the mean value (Δt) and standard deviation (σ) of 1000 measurements.

Fig. 6 shows the observed changes in the delay time. Within the whole temperature range considered, the delay is increased by 400 ps.

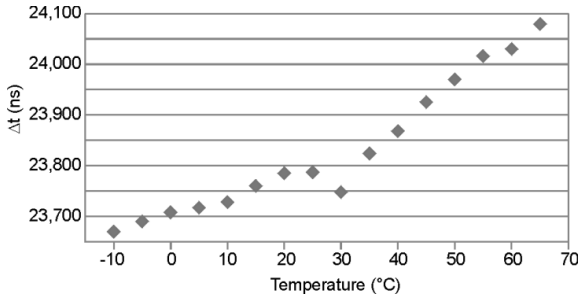


Fig. 6. The temperature dependence of the delay of signal (Δt) in the distributor

The RMS value of the timing jitter vary within the narrow window of 3.4 ps ± 0.3 ps (Fig. 7). It means that the programmable distribution amplifier can be successfully used within this temperature range.

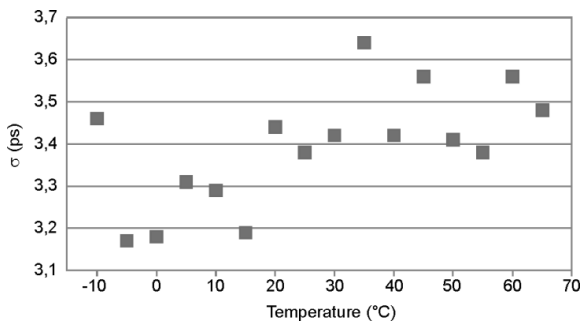


Fig. 7. The temperature dependence of the timing jitter (σ) in the distributor

4. Conclusions

The designed distributor proves that a low-cost FPGA device can successfully act as a precise crosspoint switch for clock signals. The values of delays and jitter introduced by the distributor are slightly larger than in the case of dedicated integrated circuits. However, the advantage of this solution is the possibility to build signal distributors with a larger number of inputs/outputs and the ease to modify and meet requirements of various applications.

This work was supported by the Polish National Centre for Research and Development under contract no PBS1/B3/3/2012.

5. References

[1] http://www.microsemi.com/products/timing-synchronization-systems/time-frequency-distribution/1u-distribution-amplifiers
[2] http://www.thinksrs.com/products/FS730-1.htm
[3] Digital and Mixed Signal Oscilloscopes DPO/DSA/MSO70000 Series Datasheet, Tektronix 2013.

Received: 02.04.2015 Paper reviewed Accepted: 02.06.2015

Krzysztof RÓŻYC, MSc

Krzysztof Różyc is a researcher in the Department ofElectronics at the University. He received his B.S. in 1999, and M.Sc. in 2008. He specializes in design andtesting of advanced timing instrumentation, especially for precise measurement and generation of time intervals.

e-mail: krozyc@wat.edu.pl

Paweł KWIATKOWSKI, MSc

Paweł Kwiatkowski was born in Rzeszów, Poland, in 1986. He obtained the B.S. and M.Sc. degree in electronic and communication engineering from Military University of Technology, Warsaw, Poland, in 2010 and 2011, respectively. His research activity focus on the precise time metrology systems implemented in the field programmable gate array devices.

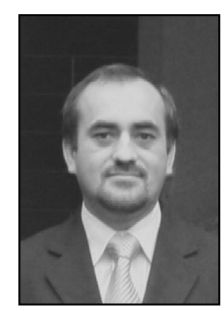
e-mail: pawel.kwiatkowski@wat.edu.pl

Marek SAWICKI, MSc

Marek Sawicki was born in Żuromin, Poland in 1985. He received the MSc degree in electronic engineering from the Military University of Technology, Warsaw, Poland, in 2005. He is a participant in PhD studies Faculty of Electronics MUT. Professionally engaged in the design of electronic devices and systems.

e-mail: marek.sawicki@wat.edu.pl

Zbigniew JACHNA, PhD



Zbigniew Jachna is an assistant professor at the University. He received his Ph.D. in 2003. His research interests include hardware and software design of precise timing instrumentation using the field programmable gate array devices.

e-mail: zjachna@wat.edu.pl

Ryszard SZPLET, PhD, DSc

Ryszard Szplet received the M.Sc. degree in electronic engineering, the Ph. D. and Habilitation degrees in applied sciences from the Military University of Technology (MUT), Warsaw, Poland, in 1989, 1997 and 2013 respectively. Since 1990, he has been with the MUT, where he has taught digital microelectronics and worked on the development of methods and instrumentation for precise time measurements and generation.

e-mail: ryszard.szplet@wat.edu.pl