POZNAN UNIVERSITY OF TECHNOLOGY ACADEMIC JOURNALS
No 95 Electrical Engineering 2018

DOI 10.21008/j.1897-0737.2018.95.0006

Pavel PAVLÁSEK[*], Matej MRÁZIK[**], Miroslav PAVELEK[*]
Branislav DOBRUCKÝ[*]

DESIGN AND VERIFICATION OF THE CHIP THERMAL MODEL: THE ASSESSMENT OF A POWER MODULES RESISTANCE TO HIGH CURRENT PEAKS

The paper is focused on creating a thermal model which provides information about the thermal conditions in the semiconductor devices. Increasing the current density and pressure on prices make the optimization of thermal systems an important part in the design process. Simulation analysis has become with development of computer technology an excellent equipment to achieve it. In creating the model, we take account of material and geometric parameters of bonded chips. By the simulation we obtain the necessary information about the components and thermal stresses, these results can be applied in the device design procedure and technology of production. Resistance to bonded diodes is determined by chip parameters and bonding parameters such as the number of bundles, their spacing, and material. Resistance in practice is determined by experimentally measuring IFSM, a peak permeable, unrepeatable current. Also, in the work we analysed voltage-current VA characteristics of power diodes such as threshold voltage, also the closing voltage we tested functionality and we observe changes in the behaviour of the component and, last but not least, the characteristics of thermal resistance and thermal impedance that served as elements for the construction of an equivalent model. In the next part of the paper, in the context of the works, the methods of bindings of PCB components are currently being extended and used in current technological processes and we also concentrate on the dimensional parameters of the modules used to create an equivalent electrical circuit. The presented assembled simplified model respects the chip size, number of bonding wires, and their layout on the chip. For the concept of nine bonds, we had two types of placement from a variety of bonds, so we also respected this factor in the design of the model. As an example, there is a diode module investigated (SKEE SEMIPACK® 2, 1600V/174A).

KEYWORDS: power modules, thermal model, simulation, finite element method.

[*] University of Žilina
[**] SEMIKRON s.r.o. Vrbové

1. INTRODUCTION

The main aim of this paper is to create a thermal model of a power semiconductor module. Power modules are designed by connecting the semiconductor components in proper processes to semiconductor modules [1, 2]. The produced module is able to withstand a higher current due to its sleeve and precision manufacturing technologies for its individual layers and larger chip areas. Integrated contacts serve to power supply the module to simplify customer handling. The copper plate at the bottom of the module provides the advantage of connecting the module to the heat sink. The area of this copper plate is determined by the transfer of the heat flow and hence the thermal model design. The dimension of this area is required to determine parameters such as thermal resistance R_{th} and thermal capacity C_{th}. The other outer dimensions are made of the plastic case of the model. The plastic case is an insulator and serves only to protect circuit against the negative effects of the surrounding environment. Another important parameter is the technology of connecting individual components, respectively chip on the board of the module. One of the most beneficial methods is bonding. The research aimed at changing the properties of copper conductors due to the diffusion of tinplate showed an extremely local increase in the electrical resistance of the driver and the consequent risk of a significant increase in the temperature at the connection point [3]. The bonding is the connection of the connecting wire and the plate. As connecting wires, thin aluminium, gold or copper micro wire, respectively with silver addition in power applications with a diameter of 100 µm to 500 µm is used. By using such thin wires, a greater number of parallel wires are used to increase the current load, which then distributes the current, and the resulting heat is evenly distributed over the entire surface of the chip. The surface of the pad or chip also affects the quality of the bonding. Preference is given to glossy surfaces before matte one to achieve better joint quality [4].

2. THERMAL MODELS OF POWER MODULE

This paper discusses two methods of a creation of a thermal model of a power semiconductor module for examining its current load. The first way is to use the principle of modeling by resistance/capacitance network (electric circuit → thermal circuit). Another way is to create a spatial model, which is solving system of partial differential equations for example in COMSOL environment [5]. As an example, there is a diode module investigated (SKEE SEMIPACK® 2, 1600 V/174 A). The experience made during practical laboratory activities with COMSOL Multiphysics used to solve some thermal problems of power

electronic devices, was helpful to setup the thermal design method of complex power module [6].

2.1. RC network model

In this case, it is necessary to know the thermal resistance of the individual parts of the module (Fig. 1), which influences the current load and the component integration density. In general, its value can be determined in two ways, based on the difference between the parts of the module and the heat output between these parts (1). The second method (2) is a direct calculation based on the geometry of the part of the module and its coefficient of thermal conductivity resulting from the material used.

$$R_{th(1-2)} = \frac{\Delta T}{P_v} = \frac{T_1 - T_2}{P_V} \tag{1}$$

$$R_{th} = \frac{l}{\lambda \cdot A} \tag{2}$$

where “l” is the layer thickness, “λ” is thermal conductivity coefficient, “A” is an area perpendicular to heat flux.

These parameters are known from the manufacturing process. In case of changes in technology or material (with better electro-thermal properties), the thermal resistance relationships can be easily modified.

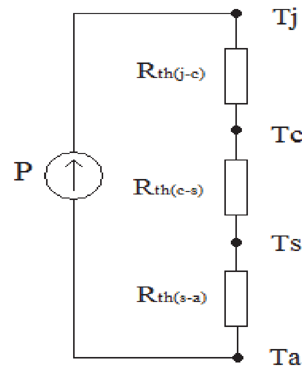

Fig. 1. Simplified thermal model of the component

However, parameter R_{th} is applicable just in case when module temperature is at constant value (constant current flow) or in steady state. Concerning the performance class of power component, the stead state usually occurs in time of 10 s. In our case will be experimental times in milliseconds and thus it is needed to consider the transient response or transient thermal impedance Z_{th}. If we

measure the component with low temperature the thermal resistance R_{th} may appear smaller than the steady-state catalog value. This phenomenon occurs due to the internal heat capacities of the power module. All layers begin as thermally "uncharged". They are gradually heated by losses from the current flow and due to that is the parameter R_{th} increased. In the moment the steady state is achieved and the heat losses are mostly emitted to the surrounding area the value of the thermal impedance given in catalog can be used [5]. For determination of Z_{th} is used following equation:

$$Z_{th} = R_{th} \cdot (1 - e^{\frac{-t}{\tau_n}}) = R_{th} \cdot (1 - e^{\frac{-t}{R_{th} \cdot C_{th}}}) \tag{3}$$

where "R_{th}" is thermal resistance and "C_{th}" is thermal capacity.
Thermal capacity is parallel element to thermal resistance in equivalent electrical circuit and is determined by equation:

$$C_{th} = c \cdot \rho \cdot V = c \cdot \rho \cdot l \cdot A \tag{4}$$

where "c" is heat capacity of material, "ρ" is density of the material and "V" is volume.

The parameter C_{th} needs to be determined for each layer of the module and this partial result are then included in calculation of thermal impedance. In addition of power module thermal parameters, it is necessary take to consideration also added thermal impedance in case of heatsink usage. Consideration should also be given to whether the passive or active cooling is used. Due to heatsink using the time constant of Z_{th} curve is also increased in other words the heat charging of heat capacitances take longer time. The continued fraction circuit reflects the real, physical setup of the semiconductor based on thermal capacitances with intermediary thermal resistances. The model can be set up where the material characteristics of the individual layers are known, whereby, however, the correct mapping of the thermal spreading on the individual layers is problematic. The individual RC-elements can then be assigned to the individual layers of the module (chip, chip solder, substrate, substrate solder, base plate). The network nodes therefore allow access to internal temperatures of the layer sequence [6].

2.2 Universal thermal model of power module

The geometry of created model is reconfigurable in a way of bond composition. This reconfiguration is possible due to the parametric position of each bond. As a reference, we chose a power module with 12 parallel bonds. It is most common arrangement with two sets bonding wires. There are of course more possibilities of bonds arrangement and the user of the created universal model determines wanted bond composition marked as B_C, L_B, S_B (Fig. 2.).

▾ Parameters

Name	Expression	Value	Description
B_C	12	12.000	number of all bondwires
L_B	3	3.0000	number of long wire bonds
S B	2	2.0000	number of short wire bonds

Fig. 2. Basic parameters of universal power module

In the model there are also defined boundaries conditions, such as thermal or electrical insulation. In addition to boundaries, material transition and thermal conductivity are set. In the examined physical samples, the area under the chip is warped by a solder with a relatively high thermal conductivity value and is many times more conductive compared to the top surface of the silicon-coated chip. The individual bonds have a different thermal conductivity value and therefore we have defined 3 transitions, which affect the heat dissipation from the power module. First transition "1" is the bottom of the power module with a high-conducting solder. Another transition is the top surface of the bondless power module which is silicone-coated and finally the bonding wires which also divert a portion of the heat from the chip. Basically, each planar geometrical element has its own boundary and material selection. The chosen material of the element then represents its electrothermal properties and the element is either conductor or insulator. The planar elements are then supplemented with a third dimension. In our case is a module with a thickness of 0.53 mm.

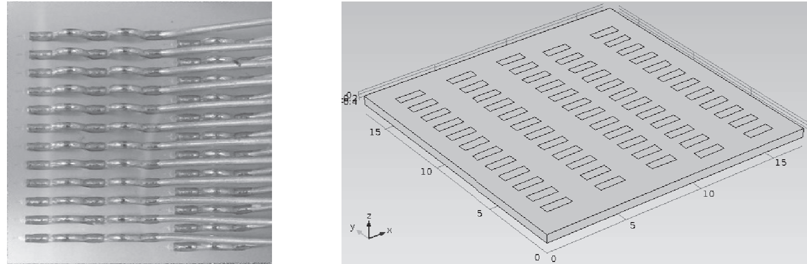

Fig. 3. The bond layout in physical sample (left) and in model (right)

For the source definition, it needs to be considered the number of bounding wires (based on the size of transmitted power). From the obtained values of the current I_{FSM}, we determined the relationship for the size of the applied voltage to maintain the power values at proportional level (Tab.1).

Table 1. Corresponding experimental currents measurements.

No. of bonds	No. of modules	Temp. [°C]	No.of chips	I_{FSMmin} [A]	I_{FSMavg} [A]	I_{FMSmax} [A]	Bond's current	Bond's voltage
12(3+2)	9-15	25	14	5464	5691,64	5979	474,30	100,00%
9(2+3)	38-44	25	14	5594	5879,86	6090	653,32	137,74%
7(2+3)	52-58	25	14	5022	5155,79	5416	736,54	155,29%
5(2+3)	67-73	25	14	3639	3796,64	3914	759,33	160,09%
12(3+2)	1-8	135	16	5214	5468,44	5588	455,70	100,00%
9(2+3)	30-37	135	16	4976	5293,31	5632	588,15	129,06%
7(2+3)	45-51	135	14	4185	4377,57	4490	625,37	137,23%
5(2+3)	59-66	135	16	3221	3299,81	3389	659,96	144,82%

The given values indicate that to maintain the magnitude of the transmitted current we must choose a higher voltage value:

For 9 bonds modules: $\frac{5879,86}{5691,64} \cdot \frac{12}{9} = 1,37$ times nominal

For 7 bonds modules: $\frac{5155.79}{5691,64} \cdot \frac{12}{7} = 1,55$ times nominal

For 5 bonds modules: $\frac{3796,64}{5691,64} \cdot \frac{12}{5} = 1,6$ times nominal

As can be seen on Fig. 4., maximal voltage (input) is set to right side of the bond and minimal voltage (ground) is set to left side of the bond. This way was each bond seat as heat source.

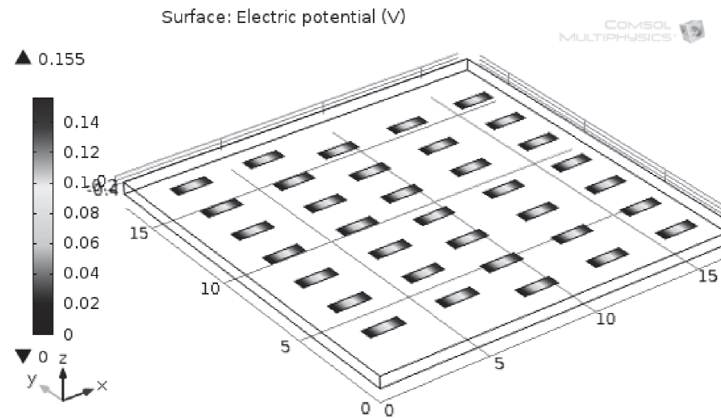

Fig. 4. Distribution of electrical potential on bonds

3. RESULTS OF THE UNIVERSAL THERMAL MODEL

The temperature distribution on the power module surface has, among other factors, a major impact on its life. When designing bonds placement, we try to make the difference between the maximum and minimum temperature on the chip face as small as possible. A simulation program can help us. In the following simulations (Fig. 5), we can monitor the chip temperature distribution for different bonds arrangement and their construction.

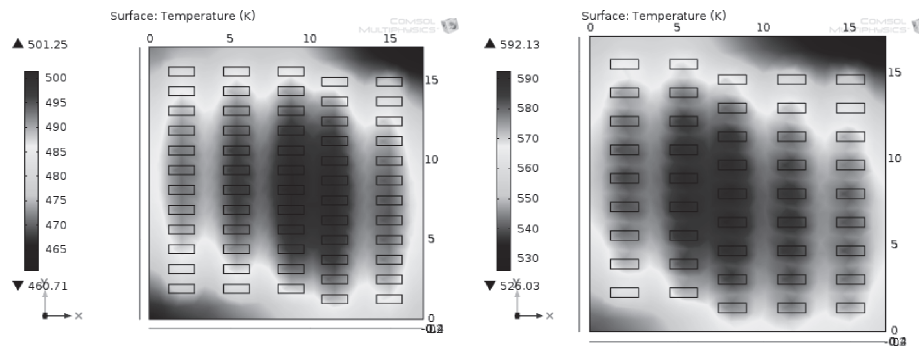

Fig. 5. Temperature distribution: 12 bonds: 3+2 (left), 9 bonds: 2+3 (right)

With layout of 12 bonds while the long bonding wire contacts the power module in 3 locations and short bonding wire in 2 locations, the most heat-stressed area has the maximum temperature of 228°C. This is probably because the horizontal distance of these bonds is less than 1.25 mm compared to

1.81 mm. The difference between maximum and minimum temperatures is 40.5°C. We have measured the highest I_{FSM} values for the 9 (2 + 3) bond spreads. This reflected even at higher temperatures on the power module. The horizontal distance of the bonds remained unchanged but the vertical distance is changed to 1.08 mm. Larger gap between bonds as well as different layouts had a positive impact on the life of the component, as we have reached the highest I_{FSM} values at this distribution. The difference between maximal a minimal temperature is 66 ° C. Heating is proportional to the electrical resistance of the bonding joint. High resistance, corresponding low thermal conductivity produces large amount of heat on the material. Due to above mentioned factors the important thing about chip heating is related to a very precise temperature distribution within 3D concept [8].

4. CONCLUSION

The high current peaks resistance of power semiconductor devices is important for predicting the reliability and performances of power electronics modules and ensuring their safe operation. The effect of exceeding the rated maximum safe bonding junction temperature can range from a change of electrical characteristics of the power module to terrible failure. Thus, this knowledge is critical for power modules reliability and performance prediction. The paper confirms the effective design and use of preferred concepts of thermal chips models along with the resistance problems and pitfalls encountered in applying concept to power modules. In addition, the advantages and disadvantages of the various configurations for models and simulation are clearly demonstrated, and a preferred technology is discussed in details for representative models of power modules which have been adopted as recommended standards on thermal measurements, modelling and simulation in real applications.

This paper was created in financial support to KEGA project No.: 071ZU-4/2017 "Key Competences Formation and Effective Support of Students Mobility at Technology Faculties: Modelling, Design and Assessment of Flexible Education Concept" and thanks to company SEMIKRON s.r.o. Vrbové, Slovakia for providing chips samples and collaboration in experiments.

REFERENCES

[1] Mrázik M., Design and verification of the model performance diode for the calculation of the resistance to high current spikes. Diploma Thesis, Supervisor: Pavlásek, P., Faculty of Electrical Engineering, University of Zilina, 28260620162022 (in Slovak), 2016.

[2] Delmonte N., Bernardoni M., Cova, P., Menozzi R., Thermal Design of Power Electronic Devices and Modules, In: Proceedings of the COMSOL 2009 Conference Milan.
[3] Pavlásek P., Analysis of the influence of additions of tin on the properties of copper wires. In: Proceedings of the 1st Science Conference, Faculty of Electrical Engineering, Slovak Technical University, Bratislava (in Slovak), 1987.
[4] Dobrucký B., Špánik, Modeling and simulation of power semiconductor structures. EDIS Zilina. ISBN 80-7100-575-4 (in Slovak), 1991.
[5] Wintrich A., el al., SEMIKRON: Application Manual Power Semiconductors. The 2nd revised edition. ISLE Verlag ISBN 978-3-938843-83-3, available: http://www.semikron.com, 2015.
[6] März M., Nance P., Thermal system modeling. Infineon, Technologies AG, Munich. Germany, 2016.
[7] AN 2015-10,Edition 2015-12-08 Published by Infineon Technologies AG 81726 Munich, Germany.
[8] Frivaldsky M., Donic T., Vavrus V., Pavelek M., Experimental research of optimization methodology for local, resistive-heating of thin molybnenum plates. Elsevier, Int. J. of Thermal Sciences, Vol. 121, pp. 111-123, ISSN 1290-0729, 2017.

(Received: 31.01.2018, revised: 02.03.2018)