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# Direct Digital Synthesizer based on Field Programmable Gate Array

**Abstract**

We present the principle (Chapter 2), implementation (Chapter 3) and test results (Chapter 4) of direct digital synthesizer (DDS) that most modules, i.e. phase accumulator, ROM memory and optional amplitude control module are implemented in a digital Field Programmable Gate Array (FPGA) device. To obtain smooth shape of analog output signals the FPGA device is followed by a digital-to-analog converter (DAC) and low-pass filter (LPF). The developed DDS allows for generating signals with frequency up to 50 MHz and amplitude up to 1 Vpp. The frequency adjustment resolution is 1.9 kHz, while the amplitude adjustment step equals 61.04 μV. The use of programmable device allows for changing the size of tuning words to adapt the DDS parameters to requirements of particular application.

**Keywords**: direct digital synthesize, programmable devices, FPGA.

## 1. Introduction

The generation of periodic electrical signals is crucial in many areas of scientific and industrial activities. With the spread of digital technology, particularly in measuring devices and tele-communication systems, a method of direct digital synthesis has been developed that allows for completely digital generating of custom waveforms within a wide frequency range. DDS systems can be realized with the use of digital signal processing system in a single programmable device. Such implementation reduces power consumption and makes the synthesizers simpler, smaller and cost effective.

The designed DDS was implemented in DE1-SoC [1] board (manufactured by *Terasic*) equipped with Cyclone V SoC FPGA (*Altera*) and THDB_ADA [2] daughter board (*Terasic*) with 14-bit dual transmit digital-to-analog converter AD9767.

## 2. Principle of DDS operation

Basic structure of DDS [3, 4] is shown in Fig. 1. The FPGA device contains phase accumulator and ROM memory that stores waveform samples. System can be extended with an optional amplitude control module. The DDS output signal is converted to analog form by DAC and shaped by low-pass filter.

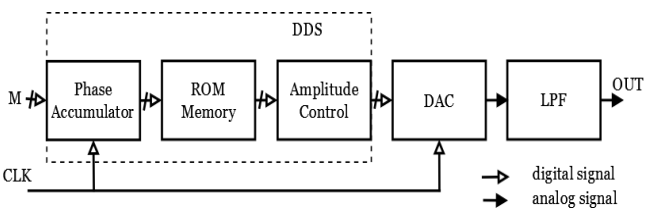


Fig. 1. DDS architecture

The phase accumulator counts clock cycles (actual value is the phase of signal) for $M = 1$ (frequency tuning word). The value of amplitude for specific sample with actual phase is read from ROM memory. After each overflow the counter starts from phase zero. Since the memory contains a single period of signal, the output frequency depends on clock frequency and stored number of samples:

$$f_{OUT} = \frac{f_{CLK}}{2^n}, \tag{1}$$

where $n$ – number of the memory address bits.

For $M > 1$ a part of samples is skipped, and a single period of waveform is represented by smaller number of signal samples. Thus less clock cycles are needed for each period of created signal. That increases signal output frequency:

$$f_{OUT} = \frac{M \times f_{CLK}}{2^n}. \tag{2}$$

When the frequency tuning word is longer than the address the word phase can assume fractional values.

## 3. Implementation of DDS

Designed DDS has been implemented in Cyclone V SoC [5] (*Atera*) using embedded modules in FPGA device. The frequency and amplitude tuning words can be selected by user. Last entered values are stored in 16-bit input register implemented with the use of embedded register elements.

The phase accumulator increases stored 16-bit phase in every clock cycle by value of the frequency tuning word. The output phase is described with the aid of 12 MSBs of stored value. The *phase accumulator* was implemented with *full adders* and r*egister* elements embedded in Altera's logic modules ALM.

The ROM memory was realized using M10K memory blocks. Each such block contains 10240 bits for data storage. They were configured as 512 16-bit cells in ROM mode and were initialized with a .mif (memory initialization file) file that contains samples of sine wave created with spreadsheet. To save 4096 samples 8 M10K blocks are needed. Samples are addressed with 12-bit word.

The amplitude control block was implemented using DSP block, that multiples two 16-bit numbers, i.e. amplitude tuning word and actual sample value. The output value is 14 MSB from 32-bits multiply result (DAC word length is 14-bits).

The input clock signal was multiplied in PLL block from 50 MHz to 125 MHz, due to the maximal speed of DAC (125 MSPS), although the system can work with maximum frequency 236.6 MHz.

All modules are placed automatically to provide the shortest connections between modules.

Implementing the system requires 62 registers, 1 DSP block, 1 PLL and 65536 memory block bits. The small amount of resources allows for the expansion of the system with additional functionality.

## 4. Test results

Measurements were carried out in the test setup shown in Fig. 2. It contains designed DDS implemented in Cyclone V device, DAC, low-pass filter with operation band B = 48 MHz, oscilloscope Infiinum DSA90804A (*Keysight*) and spectrum analyzer N9020A (*Agilent Technologies*).

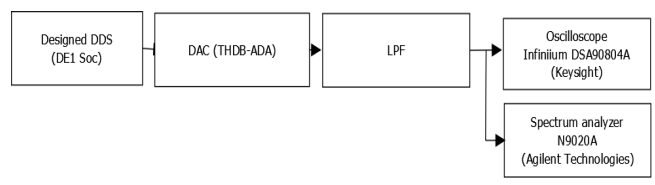


Fig. 2. Test setup

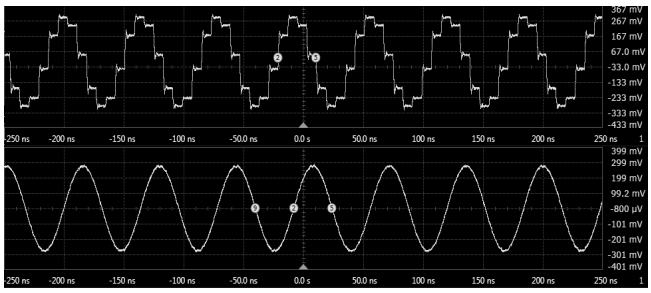

Fig. 3. Output signals obtained without filter (top) and with low-pass filter (bottom) for signal frequency $f$ =15.6 MHz ($M$ = 8192)

Figure 3 shows generated waveforms without and with low-pass filter for signal $f$ = 15.6 MHz. Filtering the signal allows to improve signal shape by reducing spurs. Figures 4 and 5 show spectrums of generated signal $f$ = 31.4 MHz ($M$ =16384) without and with filter, respectively. Spurs were reduced by 40 dB, while the primary signal was reduced only by 1.2 dB.

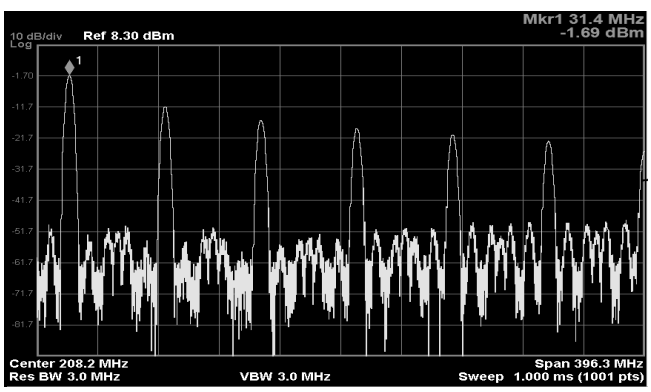


Fig. 4. Spectrum of generated waveform without filtering for $f$ = 31.4MHz

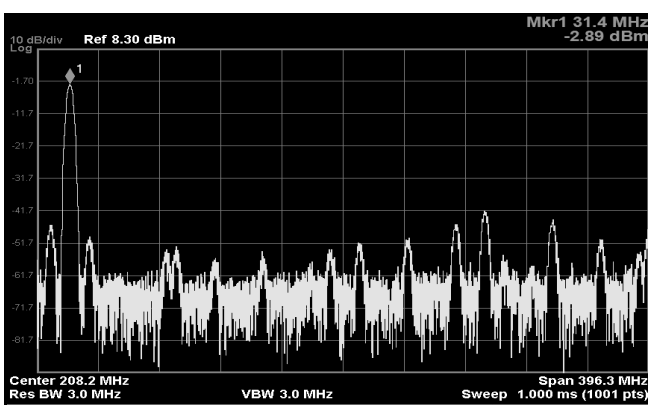


Fig. 5. Spectrum of generated waveform with filtering for $f$ = 31.4MHz

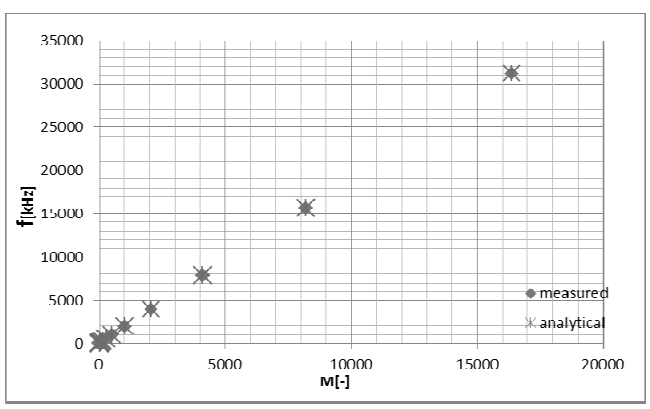


Fig. 6. Output frequency vs. frequency tuning word

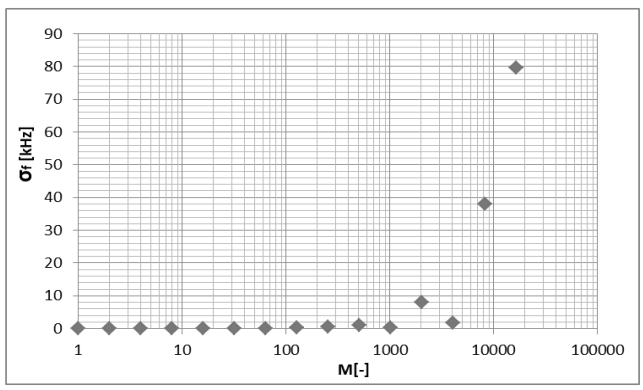


Fig. 7. Output frequency standard deviation vs. frequency tuning word

Measured output frequency corresponds with frequencies calculated analytically and increases linearly with increasing value of frequency tuning word (shown in Fig. 6). The frequency standard deviation (shown in Fig. 7) rises for $M \geq 2048$, if the period of signal is represented by 32 samples or less. For lower frequency values the standard deviation is lower than 1 kHz.

The DDS maximum output frequency is 50 MHz, however the signal amplitude was reduced (178 mV) by low-pass filter due to slightly too narrow operating bandwidth (48 MHz).

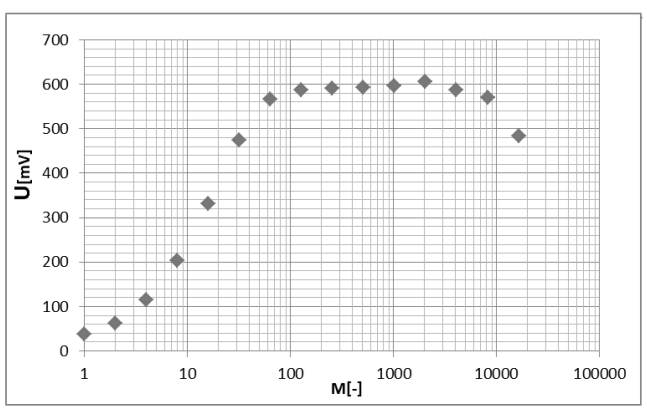


Fig. 8. Output amplitude vs. frequency tuning word

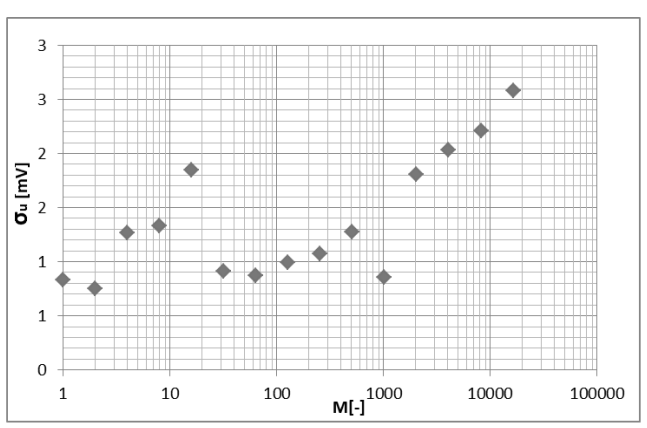


Fig. 9. Output amplitude standard deviation vs. frequency tuning word

Measured amplitude of output signal is shown in Fig. 8. It achieves large plateau value for frequency tuning words from 64 to 8192 samples. For higher frequency tuning words the amplitude

was reduced by low-pass filter, while for lower values of the word the amplitude was reduced due to the characteristic of DAC [6].

The amplitude standard deviation is shown in Fig. 9. Its value grows linearly, due to lower number of samples that describe a single period of generated signal. For frequency tuning word lower than 32 the standard deviation changes due the characteristic of DAC.

The amplitude tuning word allows for changing the amplitude of generated signal as it is shown in Fig. 10. The amplitude increases linearly with increasing value of the amplitude tuning word, however amplitudes are a bit higher than values calculated analytically. It is mainly caused by the noise mixed with the primary signal. Thus signals with amplitude lower than $0.1U_{max}$ are visibly deformed.

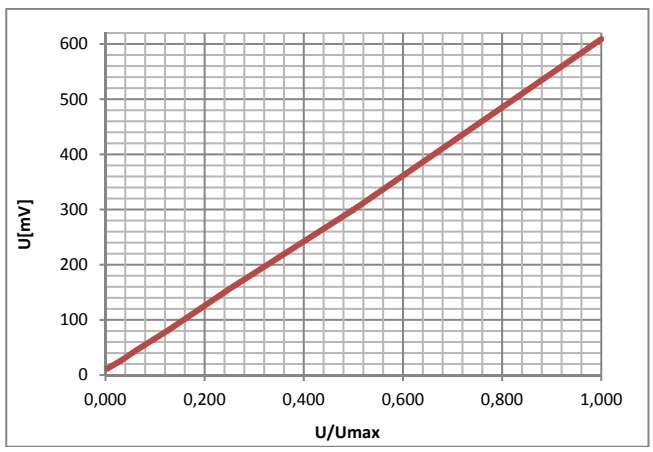


Fig. 10. Output amplitude vs. amplitude tuning word

## 5. Conclusions

The designed direct digital synthesizer has been realized with the use of a relatively cheap and easy accessible technology of programmable devices. The Cyclone V (*Altera*) device contains embedded memory, DSP blocks and PLL modules, that allow for implementing DDS structure and other digital signal processing modules involved.

The developed DDS allows for generating signals with frequency up to 50 MHz and amplitude up to 1 $V_{pp}$. It is recommended to adapt the maximum value of signal frequency to requirements of particular application, because signal quality is getting worse with increasing of frequency tuning word (less number of samples describes a single period of signal).

An important feature of the proposed solution is its ability to precise adjustment of frequency and amplitude of output signal. The frequency adjustment step is 1.9 kHz while the amplitude adjustment step equals 61.04 μV.

The digital-to-analog converter and low-pass filter have biggest influence on the quality of generated signal. The careful project of these modules is necessary to generate high quality signals with high frequency and in a wide frequency range.

## 6. References

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Ryszard Szplet received the MSc degree in electronics engineering and the PhD and Habilitation degrees in applied sciences from the Military University of Technology (MUT), Warsaw, Poland, in 1989, 1997, and 2013, respectively. He spent a one year research stay with the University of Oulu, Finland, in 2000/2001. He is currently an Associate Professor with MUT. His current research interests include fast digital electronics, especially precise time interval digitizers integrated in the field programmable gate array technology.

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