VHDL-AMS Models for Current Conveyor Based Monolithic Operational Amplifiers

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***Abstract*—This paper focuses on analysis and behavioral modeling of second generation positive and negative current conveyors (CCII+s, CCII–s), as well current-controlled current conveyors (CCCIIs). On the basis of the proposed CCII+ model improved behavioral models for three-terminal and four-terminal monolithic CFOAs are created. The models are developed by using VHDL analog and mixed-signal (VHDL-AMS) language and the descriptions are adapted to the SystemVision (version 5.5) simulation program, which is a part of the Mentor Graphics system. The proposed models simulate static and dynamic parameters for differential and common-mode input signals at room temperature, including the parameters input offsets, accurate input impedances, non-dominant poles at differential input signals, AC common-mode rejection, *PSRR* effects, output impedances, slew rate limiting and terminal voltage/current operating ranges. The modeling parameters are extracted for commercially available four-terminal CFOA AD844A and CCCII OPA860 by analyzing semiconductor data books or through characterization measurements. For the validation process simulation and experimental results for sample electronic circuits are given.**

***Index Terms*—Analog circuits, CCII, CCCII, CFOA, integrated circuit modeling, VHDL-AMS, circuit simulation**

I. Introduction

THE efficient design of analog and mixed-signal circuits using ECAD systems is determined by the use of adequate simulation models/macro-models of electronic components and ICs. This is particularly important for the various types of monolithic operational amplifiers (op amps) such as voltage-feedback operational amplifiers (VFOAs), operational transconductance amplifiers (OTAs), positive second generation current conveyors - CCs (CCII+s) [1] and current-feedback operational amplifiers (CFOAs) [2]. Since the late 1960s, when the first monolithic ICs have been put into series production for many years, VFOAs are used in 90% of the practical applications. At the same time, the progress of the microelectronic technologies over the past ten years has led to continuous development of new and improved types of op amps and more specifically of OTAs, CCIIs and CFOAs. In comparison with the OTAs and CCIIs, the main advantage of the CFOAs is that they are characterized with low output resistance. As a result, the CFOAs are more easily connected to low impedance loads. Also, in comparison with the conventional op amps (VFOAs) the CFOAs have very high slew rates (with typical value 1000 $V/\mu s$) and an ability to operate at cut-off frequencies higher than >1 *MHz*. One drawback of the CFOAs is that the feedback resistors have to be carefully selected, because the bandwidth can be limited despite the greater capabilities to provide high gain-bandwidth product of the amplifier.

A consistent practice of the semiconductor manufacturers, producing monolithic CFOAs, is the development and distribution of PSpice compatible macro-models [3-6] that are a part of the standard model libraries of any ECAD system. Moreover, in the literature there is a relatively large number of linear and non-linear PSpice compatible macro-models for bipolar and CMOS CCII+s [7-12] and CFOAs [5, 13-17]. These macro-models allow simulation of the more common small-signal effects, such as input impedance, small-signal frequency response according to the parasitic capacitances, noise, temperature effects, *CMRR* and output impedance. Also, non-linear transfer characteristic, short-circuit current and output slew rate limiting are modeled. Furthermore, in these macro-models the attention is focused on the simulation of a certain group of electrical parameters of the real devices.

In the standard PSpice model libraries the majority of the CCII+ and CFOA macro-models are presented as device-(transistor-) level models, called micro-models. Typically the input stage is a device-level model and other stages consist of an extensive number of passive elements, ideal controlled sources and several diodes. The simulation testing of analog circuits using CC-based op amps with transistor-level models is a difficult process that requires longer simulation time, and in some cases the simulation process can be interrupted due to a lack of convergence [18].

One of the methods to reduce the simulation time and increase accuracy and include certain specific effects is by using behavioral modeling techniques. The most effective Hardware Description Languages (HDLs) [19-20] of analog electronic circuits are VHDL-AMS (analog and mixed signal) [21] and Verilog-A [22]. The basic advantage of the VHDL-AMS is that the simulation models can be coded by using a style, combining structural and behavioral elements. The analysis of the literature shows that there are small group of VHDL and VHDL-AMS models of monolithic operational transconductance amplifiers (OTAs) [24], voltage-feedback operational amplifiers (VFOAs) [25], and CFOAs [26-27].

In [24], the authors present a method to build a behavioral OTA ageing model usable for fast reliability simulations of systems. The ageing of OTA circuits is due to the ageing of MOSFET transistors. The model is developed by using VHDL-AMS and accurately simulates input resistance, transconductance, output resistance and voltage/current limitations.

In 2006, H. Qin and F. Wang present a voltage-feedback operational amplifier simulation model based on VHDL-AMS [25]. This model simulates the input impedance for the differential and common-mode signals, one-pole frequency

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The current-feedback op-amps and current conveyors are all part of the same family. [2] C. Toumazou, A. Payne, and J. Lidgey

response, output impedance, output saturation and slew rate. The output voltage limitations is achieved by two clamp diodes connected between middle point of the second stage and terminals defines the highest and lowest output voltages.

In 2009, R. El-Queseny, S. Mahmoud and M. Ibrahim present a simplified model of CFOA based non-inverting amplifier using standard VHDL [26]. This interesting model is intended basically to simulate the small-signal frequency and transient responses for various voltage gains of non-inverting amplifier configuration.

In 2010, the author proposed a VHDL-AMS model [27] that simulates basic static and dynamic parameters of the three-terminal CFOAs suitable for general applications at low frequencies. To achieve simplicity of the mathematical equations describing the model, it neglects several specific effects found in the monolithic CFOAs, such as accurate input impedances, terminal voltage/current operating ranges, non-dominant poles, *PSRR* and frequency dependence of the *CMRR*.

In this paper VHDL-AMS models of CC based amplifiers, namely CCII+, CCII–, CCCII and improved non-linear behavioral models for three-terminal monolithic CFOAs (conventional CFOAs) and four-terminal CFOAs (CFOAs with available output *z* terminal (or compensation pin)) are presented. The developed CFOA model is based on the models reported in [26] and [27] and includes important specific effects of the behavior of the real devices for small and large input signal over wide frequency range.

The organization of the paper is as follows: in Section II the structure and relation between the input and the output voltages and currents for the commonly used CC based op amps are presented; in Sections III the structure, mathematical equations and the VHDL-AMS codes of the proposed models are described; the verification of the simulated electrical characteristics and parameters is given in Section IV; to illustrate the efficiency of the proposed models, in Section V examples of studying the frequency responses of two second-order active filters at certain parameters are shown. Finally in Section VI, the concluding remarks are given.

II. CC Based Monolithic Operational Amplifiers – Simple Linear Models

The first op amp, an object of analysis and modeling, is the CCII proposed by Sedra and Smith [2]. This op amp is based on the first generation CCs (CCIs) introduced by Smith and Sedra in 1968. An equivalent circuit of an idealized model for a CCII is shown in Fig. 1. The circuit consists of one voltage-controlled voltage source (VCVS) and only one current-controlled current source (CCCS) in comparison with CCI. If an input voltage v is applied to y terminal, a voltage will appear on the input x, i.e. $v_x = \alpha_{yx} v_y$. The α_{yx} is the voltage gain between y and x. The current in node y is equal to zero. The input y exhibits infinite input impedance. If an input current i being forced into input x, it will be conveyed to the z terminal – $i_z = \alpha_{xz} i_x$. The coefficient α_{xz} is the current gain between x and z. For the idealized model the parameters α_{yx} and α_{xz} are approximately equal to unity.

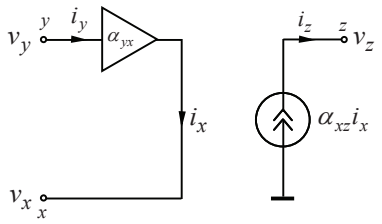

Fig. 1. A simple linear model for CCII.

The ideal relation between the input and output voltages and the currents for the CCII can be given by the following hybrid matrix

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \times \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \Rightarrow \begin{cases} i_y = 0 \\ v_x = v_y \\ i_z = \pm i_x \end{cases}. \quad (1)$$

The sign plus or minus in the third row of the hybrid matrix (1) defines the current direction of i_z.

The second monolithic op amp is the CCCII, obtained from the current-controlled current conveyor, given in [28]. This type of op amps is a bases for development of various of electronically tunable active filters and oscillators. The structure of the CCCII is similar to the CCII, but in the CCCII the value of the series resistance r_x can be tuned via the external bias current I_{bias}.

The ideal relation between the input and output voltages and the currents for the CCCII is given by the following matrix

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & r_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \times \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \Rightarrow \begin{cases} i_y = 0 \\ v_x = v_y + i_x r_x \\ i_z = \pm i_x \end{cases}. \quad (2)$$

The sign plus and minus in the matrix (2) denote positive and negative types of the current-controlled current conveyors (CCCII+ and CCCII–), respectively. The r_x represents the series input resistance of the op amp.

The CCCIIs can be implemented by using bipolar or CMOS technology. When using bipolar transistors for the basic structure of CCCII [29-30] the series resistance to input x versus the external bias current I_{bias} (at $i_x(t) << 2I_{bias}$) can be determined by the following principle formula

$$r_x \approx \varphi_T / 2I_{bias}, \quad (3)$$

where $\varphi_T = kT/q$ is the thermal voltage.

Also, the change of the bias current I_{bias} leads to a change of the output resistance r_z. The basic expression of this non-linear function for the bipolar CCCII [28, 31] can found by

$$r_z \approx \left(\frac{2I_{bias}}{\beta_p V_{AP}} + \frac{2I_{bias}}{\beta_n V_{AN}} \right)^{-1}, \quad (4)$$

where β_n and β_p are the forward current gains of the output complementary bipolar transistors of the circuit and V_{AN} and V_{AP} are the corresponding forward Early voltages.

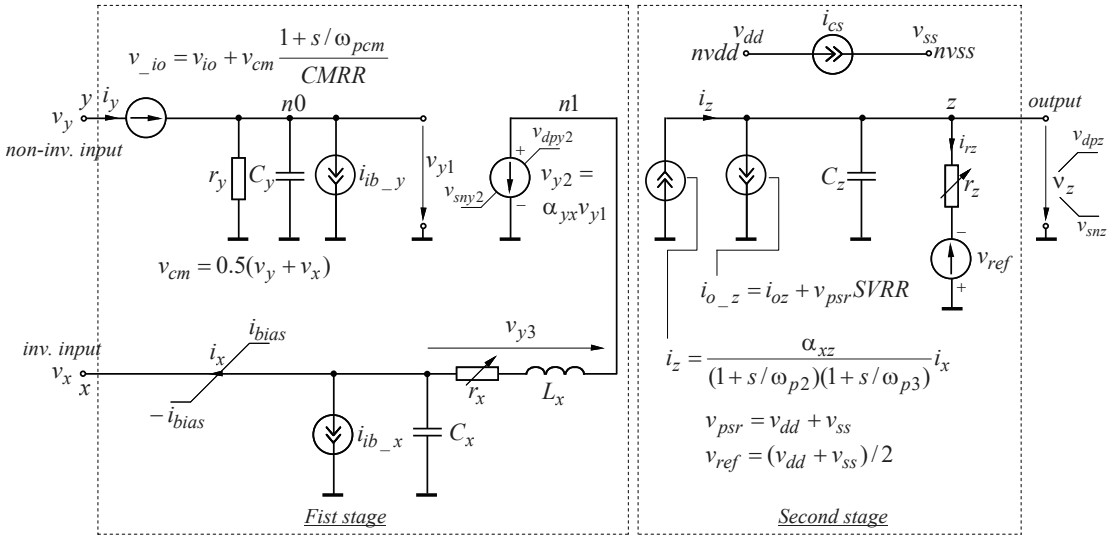

Fig. 2. Circuit diagram of the proposed CCII+ behavioral model.

For the CMOS CCCIIs the transistors operate in weak inversion (subthreshold region) with small currents I_{bias}. The value of the series resistance to input x can be obtained by $r_x \approx n\varphi_T / 2I_{bias}$, where n = 1.2 to 1.6 is the slope factor.

The expression output resistance as a function of the bias current is

$$r_z \approx \left(\frac{1}{\lambda_n I_{bias}} + \frac{1}{\lambda_p I_{bias}} \right)^{-1}, \tag{5}$$

where λ_n and λ_p are the channel-length modulation parameters of the output complementary MOS transistors.

The most common monolithic CFOA is equivalent to a CCII+ plus an output voltage buffer and is known as three-terminal op amp. In some of the CFOAs the z terminal, between the first stage (CCII+) and the second stage (voltage buffer), is defined as an external pin. As a result, a four-terminal op amp is obtained, known as a four-terminal CFOA. For this model the general relation between input and output voltages and the currents can be given as $i_y = 0$, $v_x = \alpha_{yx} v_y$, $i_z = \alpha_{xz} i_x$ and $v_z = \alpha_{zo} v_o$.

III. Behavioral Modeling with VHDL-AMS

The proposed behavioral models for the CC based op amps are developed following the design method based on a Top-Down analysis approach [32]. Based on theoretical analysis of monolithic electronic circuits [23, 29, 31], a set of mathematical equations are obtained describing the electrical input, output and transmission characteristics. The parameters in those equations are the physical parameters, which corresponds to certain region of operation. The concrete numerical values are valid only for the chosen bias point.

The complete set of equations is implemented using VHDL-AMS language, combining both structural and behavioral elements. The structural description is the "net-list" of the model and includes of a list of the electronic components and a list of the nodes to which they are connected. The behavioral description basically consists of simultaneous statements and some event-driven operators. This style of the model can simplify the description of the real devices and in some cases improve the model efficiency, as well the DC convergence of the computation process.

A. CCII simulation model

The model for CCII+ is the primary proposed structure. The complete circuit diagram of the model, which corresponds to the VHDL-AMS code, is shown in Fig. 2. The core of this diagram is the structure of the linear model, shown in Fig. 1.

The first and second stages are separated by a dotted line. The terminals of the circuit are designated as follows: y – non-inverting input, x – inverting input, *nvdd* – positive power supply, *nvss* – negative power supply and z – output. The negative types of the CCII (or CCII–) can be obtained by modification of the second stage of the circuit.

The description of the equivalent circuit components is presented in Table I. The complete mathematical equations of the model are

$$v_{y1} = v_y - v_{\_io}, \tag{6}$$

$$i_y = v_{y1}\left(r_y^{-1} + sC_y\right), \tag{7}$$

$$v_{\_io} = v_{io} + v_{icm}\frac{1+s/\omega_{pcm}}{CMRR}, \tag{8}$$

$$v_{icm} = 0.5(v_y + v_x), \tag{9}$$

$$i_{ib\_y} = i_{ib} + i_{io}/2, \tag{10}$$

$$v_{y2} = \alpha_{yx} v_{y1}, \tag{11}$$

$$v_x = \frac{v_{y2} + (r_x + sL_x) i_x}{1 + sr_x C_x + s^2 L_x C_x}, \tag{12}$$

$$i_{ib\_x} = i_{ib} - i_{io}/2, \tag{13}$$

$$i_z = \frac{\alpha_{xz}}{(1+s/\omega_{p2})(1+s/\omega_{p3})} i_x \tag{14}$$

($\omega_{p2} = 2\pi f_{p2}$ and $\omega_{p3} = 2\pi f_{p3}$),

$$i_{o\_z} = i_{oz} + v_{psr} SVRR\,, \tag{15}$$

$$v_{psr} = v_{dd} + v_{ss}\,, \tag{16}$$

$$v_{z1} = i_{rz} r_z + v_{ref}\,, \tag{17}$$

$$v_z = v_{z1}\ (\Delta v_{z1}^{+} \approx SR^{+}\Delta t \text{ and } \Delta v_{z1}^{-} \approx SR^{-}\Delta t\,), \tag{18}$$

$$i_{z1} = v_{z1} s C_z \text{ and} \tag{19}$$

$$v_{ref} = 0.5(v_{dd} + v_{ss})\,. \tag{20}$$

TABLE I
CIRCUIT COMPONENTS DESCRIPTION

Component	Description
First stage	
$v_{\_io}$	Voltage-controlled voltage source (VCVS) – input offset voltage U_{io} and the frequency dependence of the common-mode rejection ratio (*CMRR*) (DC value for *CMRR* and upper cut-off frequency f_{pcm})
v_{icm}	Free quantity – VCVS, determines the input common-mode voltage $v_{icm} = 0.5(v_y + v_x)$
r_y and C_y	Resistor and capacitor, modeling input impedance to the non-inverting input (y - terminal)
i_{ib_y} and i_{ib_x}	Independent current sources, modeling input bias current I_{iB} and input offset current I_{io}
v_{y2}	VCVS - determines transmission between y - and x - terminals $v_x = f(v_y)$ (α_{yx} is the DC voltage gain between y and x). y – input voltage range $U_{omy}^{+(-)}$.
i_{x_h}	Free quantity – represents the i_x current limiting $\pm I_{biasx}$
r_x, C_x and L_x	Resistor, capacitor and inductor, modeling the input impedance to the inverting input (x - terminal)
Second stage	
i_z	Current-controlled current source (CCCS) – frequency response of the $i_z = f(i_x)$ (α_{xz} is DC current gain second pole at frequency f_{p2} and third pole at frequency f_{p3})
i_{o_z}	Voltage-controlled current source (VCCS) – output offset current and form supply voltage rejection ratio (*SVRR*)
v_{psr}	Free quantity – VCVS, determines the power supply offset and supply voltage rejection ratio
r_z and C_z	Resistor and capacitor, modeling the transimpedance and dominant pole at frequency $f_{p1} = 1/2\pi r_z C_z$ for CCII
v_{z1}	Free quantity – represents the v_z voltage limiting $U_{omz}^{+(-)}$ and the slew rate rising and falling slope (SR^{+} and SR^{-})
v_{ref}	Free quantity – VCVS, determines the power-supply common terminal for CCII
i_{cs}	Independent current source – quiescent current between power supplies

The voltages v_{y2} and v_z are limited by the saturation voltages, as shown in Fig. 2 and given by

$$v_{sny2} \le v_{y2} \le v_{dpy2} \text{ and} \tag{21}$$

$$v_{snz} \le v_z \le v_{dpz}\,, \tag{22}$$

where v_{sny2} (and v_{snz}) is the negative saturation voltages and v_{dpy2} (and v_{dpz}) is the positive saturation voltages.

Also, the current i_x depends on the applied signal amplitude between y – and x – terminals. On condition that in the linear region of operation the current i_x is constant, for the limitation can be written

$$-I_{bias} \le i_x \le +I_{bias}\,. \tag{23}$$

The most of the model parameters, used in the above mathematical equations, can be obtained either by analyzing manufactured datasheet or through physical experiment using the corresponding test conditions. For the coefficient α_{yx} and α_{xz}, that do not include measuring procedure, it has to follow the testing conditions given in [16]. The gain α_{yx} is measured by applying a voltage at y terminal and measuring the resulted voltage at x terminal. The gain α_{xz} is measuring by injecting a current at x terminal and measuring the output current at z terminal. The current limiting $\pm I_{biasx}$ is obtained at the saturation of the input stage at x terminal.

The resistor r_y and capacitor C_y, modeling the input impedance to the non-inverting input, can be determined applying input voltage at y terminal, as x open (without doted wire) and port z grounded (Fig. 3). The resistance r_y is then measured at low frequency and the parasitic capacitance C_y obtained from the $-3dB$ cutoff frequency of the magnitude of the input impedance at y [7], [16].

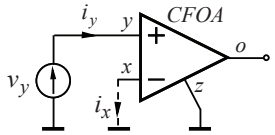

Fig. 3. Test circuit used for measuring of r_y, C_y and r_x.

The series parasitic resistance r_x is the output resistance at x terminal and is measured at low frequency with x and z grounded (Fig. 3). The value of r_x is found as a relation v_y / i_x [16].

Assuming a second-order low-pass response for the transmission between y - and x - terminals the values of L_x and C_x can be calculated according the formulas for the resonant frequency and quality factor given as

$$\omega_o = 1/\sqrt{L_x C_x} \text{ and} \tag{24a}$$

$$Q = r_x^{-1}\sqrt{L_x / C_x}\,. \tag{24b}$$

At quality factor (Q-factor) greater than $1/\sqrt{2}$ a peak occur in the transmission between y and x. These are related to the measured magnitude $\alpha_{yx_{\max}} = \alpha_{yx} Q\sqrt{1-1/(4Q^2)}$ at frequency $\omega_{\max} = \omega_o\sqrt{1-1/(2Q^2)}$. On the basis of these two formulas it can be found the resonant frequency and Q-factor.

The resistor r_z and capacitor C_z, modeling the transimpedance can be determined applying input voltage at z terminal, as x and y grounded (Fig. 4). The values of r_z and C_z can be determined in a similar manner as r_y and C_y [7], [16].

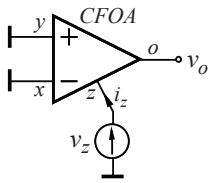

Fig. 4. Test circuit used for measuring of r_z and C_z.

Fig. 5 shows the VHDL-AMS model code of a CCII+. The description of the model is adapted to the simulator of the SystemVision – SV (version 5.5) program, which is a part of the EDA system Mentor Graphics. The library clause and the use clause in the code make all declarations in the packages `IEEE.electrical_systems` and `IEEE.math_real` visible in the model. This is necessary, because the model uses nature `electrical` from package `IEEE.electrical_systems` and constant `math_2_pi` for the value of 2π from package `math_real`. The proposed CCII+ model is composed by an *entity* and an *architecture*, where bold text indicates reserved words and upper-case text indicates predefined concepts. The entity declares the generic model parameters and specifies five interface terminals of nature `electrical`. For the model parameters concrete numerical default values have to be given. Then, in the process of modeling a particular CCII+, using SV program, in interactive mode of operation the new parameter values are set.

The proposed CCII model includes five electrical terminals: `y`, `x` , `nvdd`, `nvss` and `z`. Furthermore, the model has two inner terminals: `n0` and `n1`. They are used to specify the internal voltages `vy1` and `vy2`, respectively. The architecture of the model is subdivided into two parts: *input stage* and *transfer stage*. It contains the implementation of the model.

```
   library IEEE;
   use IEEE.math_real.all;
   use IEEE.electrical_systems.all;
   ENTITY CCII__model IS
   GENERIC (
   --generic constants here);
   PORT (terminal y, x, z, nvdd, nvss : electrical);
   END ENTITY CCII__model;
   ARCHITECTURE arch_CCII_model OF CCII_model IS
   -- inner terminals
     terminal n0, n1: electrical;
   -- inner branch quantities
     quantity vy across iy, icy through y to electrical_ref;
     quantity v_io across i2 through y to n0;
     quantity vy1 across n0 to electrical_ref;
     quantity vy2 across iy2 through n1 to electrical_ref;
     quantity vy3 across ix through x to n1;
     quantity vx across iib_x, icx through x to electrical_ref;
     quantity iib_y through n0 to electrical_ref;
     quantity iz, irz, icz, io_z through z to electrical_ref;
     quantity vz across z to electrical_ref;
     quantity vdd across nvdd to electrical_ref;
     quantity vss across nvss to electrical_ref;
     quantity ics through nvdd to nvss;
   -- inner free quantities
     quantity vicm:VOLTAGE;
     quantity vpsr:VOLTAGE;
     quantity vz1:VOLTAGE;
     quantity vref:VOLTAGE;
     quantity ix_h : current;
   -- constants
     constant wp2: REAL := fp2 * math_2_pi; -- second pole
     constant wp3: REAL := fp3 * math_2_pi; -- third pole
     constant num_DM: REAL_VECTOR := (0 => wp2 * wp3 * axz);
     constant den_DM: REAL_VECTOR :=(wp2*wp3, wp2+wp3, 1.0);
     constant wpcm: REAL := fpcm * math_2_pi; -- -3db pole
frequency in radians
     constant num_CM: REAL_VECTOR := (wpcm, 1.0);
     constant den_CM: REAL_VECTOR := (wpcm, 0.0);
   begin
   --***input stage***--
     iy == vy/ry;
     icy == cy * vy'dot;
     iib_y == iib + iio/2.0;
     vicm == 0.5*(vy+vx);
     vpsr ==(vdd+vss);
     v_io == vio + (vicm'ltf(num_CM, den_CM))/CMRR;
   --limitation of the Y2-terminal voltage--
     if vy2'above(vdpy2) use vy2 == vdpy2;
     elsif not vy2'above(vsny2) use vy2 == vsny2;
      else vy2 == ayx * vy1;
     end use;
     vy3 == ix_h * rx + lx_h * ix_h'dot;
   --limitation of the Ix current--
     if ix_h'above(ibias) use ix == ibias;
     elsif not ix_h'above(-ibias) use ix == -ibias;
       else ix == ix_h;
    end use;
     icx == cx * vx'dot;
     iib_x == iib - iio/2.0;
     ics == SUPPLY_CURRENT;
   --***transfer stage***--
     io_z == ioz + vpsr*SVRR;
     iz == ix'ltf(num_DM, den_DM);
     vz1 == irz*rz + vref;
     vref ==(vdd+vss)/2.0;
   --limitation of the output voltage--
     if vz1'above(vdpz) use vz == vdpz;
     elsif not vz1'above(vsnz) use vz == vsnz;
      else vz == vz1'slew(SRp, SRn);
   end use;
   break on vz1'above(vdp), vz1'above(vsn);
   icz == cz * vz'dot;
   END ARCHITECTURE arch_CCII_model;
```

Fig. 5. VHDL-AMS model of a CCII+.

B. CCCII simulation model

The created novel model for CCCII is built based on the CCII model and the structure of bipolar CCCII op amp, presented in [27]. The model is built according to the equivalent circuit for the CCII+, shown in Fig. 2. The variable resistances r_x and r_z simulate the functional dependence on the external bias current. Moreover, the CCCII model simulates the same electrical characteristics as CCII+ model.

The mathematical description of the model is supplemented with formulas (3), (4) and (5) valid for op amps using bipolar transistors or MOSFETs, operating in weak inversion. Thus, without considering the specifics of the various structures of op amps, control of the r_x and r_z are obtained.

In Fig. 6 only the new lines in the VHDL-AMS model for the CCCII are given compared with the code for the CCII. Also, in the VHDL-AMS description the packages `IEEE.fundamental_constants`, `IEEE.thermal_systems` and `MGC_AMS.conversion` are included.

For the CCCII model the parameter `rx` and `rz` are removed from the list of the parameters. The resistances `rx` and `rz` are declared as a free quantities. The values of the `rx` and `rz` are obtained by the algebraic formulas in the architecture. The bias current `Ibias` can be declared as a generic model parameter or as an external quantity. In the created model the current `Ibias` is declared as a generic parameter. This manner of declarations is effective especially for complex electronic circuits of active filters.

```
GENERIC (
.....................
   temp_ambient : real := real'LOW;  -- Ambient temperature [C|K]
   temp_units   : temperature_units := celsius; -- Temperature
Units
   BETAN : real := … ;-- Forward current gain of the output NPN
transistor
   BETAP : real := … ;-- Forward current gain of the output PNP
transistor
   VAN : VOLTAGE := … ;-- Forward Early voltage of the output NPN
transistor
   VAP : VOLTAGE := … ;-- Forward Early voltage of the output PNP
transistor
.....................
  Ibias : CURRENT := value); -- bias current
   PORT (terminal y, x, z, nvdd, nvss : electrical);
   END ENTITY CCII_model;
   ARCHITECTURE arch_CCII_model OF CCII_model IS
   -- inner free quantities
     quantity rx : resistance;
     quantity rz : resistance;
     constant TempK : temperature :=
ambientTempFromGeneric(temp_ambient, temp_units); -- Temperaure [K]
     constant vt : real := PHYS_K*TempK/PHYS_Q; -- Thermal Voltage
  --PHYS_K = Joules/Kelvin - Boltzmann constant
  --PHYS_Q = coulomb - electron charge
   begin
   rx == vt/(2.0*ibias);
   rz == 1/((2.0*ibias)/(BETAN*VAN)+ (2.0*ibias)/(BETAP*VAP));
.....................
   END ARCHITECTURE arch_CCII_model;
```

Fig. 6. New lines used in the VHDL-AMS model of a CCCII.

C. Improved CFOA simulation models

The behavioral models of a three-and four- terminal CFOA are obtained from the CCII+ model (Fig. 2) by adding a VHDL-AMS description of an output stage. Also, in the construction of the model the structure of the transfer stage is modified and some of the mathematical equations, describing the modeling of the *SVRR* and the slew rate rising and falling slopes are changed.

In the structure of the transfer stage (Fig. 2) the VCCS i_{o_z} is removed. According to the conventional op amp macro-modeling the input parameters, such as the offset voltage, one-pole approximation of the *CMRR* and *PSRR* are defined in the VCVS $v_{\_io}$ of the input stage as

$$v_{\_io} = v_{io} + v_{icm}(1 + s/\omega_{pcm})/CMRR + v_{psr}/PSRR, \quad (24)$$

where *PSRR* is the DC power supply rejection ratio with dimension $V/\mu V$.

The corresponding code has the form, shown in Fig. 7.

```
vicm == 0.5*(vy+vx);
vpsr ==(vdd+vss);
v_io == vio+(vicm'ltf(num_CM, den_CM))/CMRR + vpsr/PSRR;
```

Fig. 7. VHDL-AMS description for the VCVS $v_{\_io}$, modeling input offset voltage and the frequency dependence of the *CMRR* and *PSRR* of CFOA.

In the second stage the description for the rising and falling slopes of the v_z is removed. In the model for the CFOA in the code, z is defined as an inner terminal. The VHDL-AMS description of the z terminal limitation is presented in Fig. 8.

```
--limitation of the Z-terninal voltage--
  if vz1'above(vdpz) use vz == vdpz;
  elsif not vz1'above(vsnz) use vz == vsnz;
   else vz == vz1;
  end use;
```

Fig. 8. VHDL-AMS description of the z-terminal voltage swing of CFOA.

For the real CFOAs the output stage can be represented as voltage follower with complex output impedance. As a result, the output stage can be modeled as one grounded VCVS and series connection of resistor and parasitic inductance. The equivalent circuit of the created behavioral model is shown in Fig. 9. The terminals of the circuit are designated as follows: z – output of the transfer stage, $n2$ – inner terminal and o – output terminal. The proposed model contains one linear controlled source `vo1` and series connection two passive components ($z_o = r_o + j\omega L_o$).

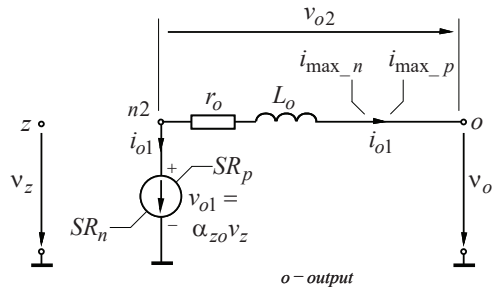

Fig. 9. Circuit diagram of the implemented output stage for CFOA model.

The mathematical equations that describe the model are

$$v_{o1} = \alpha_{zo} v_z \ (\Delta v_z^+ \approx SR_p \Delta t \text{ and } \Delta v_z^- \approx SR_n \Delta t), \quad (25)$$

$$v_{o2} = i_{o2\_h}(r_o + sL_o) \text{ and} \quad (26)$$

$$i_{o2\_h} = \begin{cases} i_{\max\_p} & at \ \ i_{o2\_h} > i_{\max\_p} \\ i_{o2} & at \ \ i_{\max\_n} \le i_{o2\_h} \le i_{\max\_p} \\ i_{\max\_n} & at \ \ i_{o2\_h} < i_{\max\_n}. \end{cases} \quad (27)$$

Then, the frequency response at active load R_L is

$$\dot{A}_{U,out} = \frac{v_o}{v_z} = \frac{A_{U,out0}}{1 + j(f/f_{pL})}, \quad (28)$$

where $f_{pL} = L_o/2\pi(R_L + r_o)$ is the frequency of the pole caused by the L_o and load R_L, $A_{U,out0} = \alpha_{zo} R_L/(R_L + r_o)$ is the voltage gain at low frequency and α_{zo} is the DC voltage gain of the output stage.

The VHDL-AMS code, adapted to the SV program for the output stage is shown in Fig. 10.

```
--***output stage***--
  vo1 == azo * vz'slew(SRp, SRn);
  vo2 == io2_h*ro + lo * io2_h'dot;
--limitation of the output current--
if io2_h'above(i_max_p) use io2 == i_max_p;
  elsif not io2_h'above(i_max_n) use io2 == i_max_n;
    else io2 == io2_h;
end use;
```

Fig. 10. VHDL-AMS model of a CFOA output stage.

The gain α_{zo} is measured by applying a voltage at z terminal and measuring the output voltage at o terminal. The positive and negative voltages (v_{dpz} and v_{snz}) to node $n2$ is measured as maximum and minimum voltages at which the output stage become in saturation mode of operation (Fig. 4).

The output impedance r_o and L_o can be measured by applying a varying current source i_o to the o port, as x and y grounded (Fig. 11) [16]. The r_o is then measured at low frequency and the L_o obtained from the $+3dB$ cutoff frequency of the magnitude of the output impedance at o.

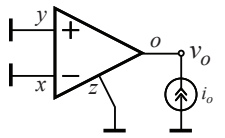

Fig. 11. Test circuit used for measuring of r_o and L_o.

For the model of a three-terminal CFOA there are five external and four internal electrical terminals. The external terminals are: y, x, $nvdd$, $nvss$ and o (*output*) (Fig. 12). The inner terminals are: $n0$, $n1$, z and $n2$. They are used to specify the voltages v_{y1}, v_{y2}, v_z and v_{o1}, respectively. For the model of the four-terminal CFOA pin z is defined as an external terminal.

```
.....................
port (terminal y, x, output, nvdd, nvss : electrical);
END ENTITY three_terminal_CFOA;
ARCHITECTURE arch_three_terminal_CFOA of three_terminal_CFOA is
-- inner terminals
  terminal n0, n1, n2, z: electrical;
.....................
```

Fig. 12. VHDL-AMS code, describing the terminals of a three-terminal CFOA.

Based on the analysis of the complete equivalent circuit for the amplitude-frequency and phase-frequency responses is obtained

$$|\dot{A}_U| = \frac{A_{U0}}{\sqrt{\left[1+\left(\frac{f}{f_{p1}}\right)^2\right]\left[1+\left(\frac{f}{f_{p2}}\right)^2\right]\left[1+\left(\frac{f}{f_{p3}}\right)^2\right]\left[1+\left(\frac{f}{f_{pL}}\right)^2\right]}} \quad (29)$$

and

$$\varphi_{A_U} = -\sum_{i=1}^{3}\arctan\left(\frac{f}{f_{pi}}\right) - \arctan\left(\frac{f}{f_{pL}}\right), \quad (30)$$

where $A_{U0} = \alpha_{yx}\alpha_{xz}\alpha_{zo}r_z R_L/(R_L + r_o)$ is the open-loop DC open-loop voltage gain, $f_{p1} = 1/2\pi r_z C_z$ is the frequency of the dominant pole, and f_{p2} and f_{p3} are the frequencies of the second and third pole (non-dominant poles), respectively.

As can be seen at resistive load the open-loop voltage gain of the CFOAs is represented as a fourth-order transfer function with four real poles (dominant pole and three non-dominant poles).

IV. Verification of the Proposed Models

The verification of the proposed models is performed for the four-terminal CFOA model, because its structure contains all functional blocks and stages of the most common CC based op amps. In the process of verification a comparison analysis between the developed model and PSpice compatible macro-model for CFOA, reported in [14], is performed. The two models without external elements are tested under same conditions and electronic circuits. For the purpose of the verification the CFOA AD844 from Analog Devices is chosen [33]. For AD844 the z terminal is an external pin, which allows the op amp to be used as a four-terminal CFOA. The computer simulations of the AD844 is performed with AD844A/AD PSpice macro-model (version 1.0 (07/1991)). This version of the AD844 macro-model simulates the parameters of an 'A' grade, in the semiconductor data book. Actually, the AD844 macro-model is based on the macro-model structure for CFOAs, presented in [14].

All the modeling parameters for the proposed CFOA model that give good agreement with the experimental results related to the AD844A model at $V_{DD}^{+} = -V_{SS}^{-} = 15V$ (typical values), $R_L = 500\Omega$ and $T_A = 25°C$ are given in Table II. The last column in Table II gives the parameter extraction procedure, where EXP is obtained from experimental test, DS is a datasheet typical value, and E is a typical estimated value from device design. To demonstrate the non-linear behavior of the four-terminal CFOA, the voltage and current DC transfer characteristics obtained from OrCAD PSpice with AD844A/AD and from SV with the proposed model are illustrated in Fig. 13, Fig. 14 and Fig. 15.

TABLE II
VHDL-AMS Modeling Parameters for Four-Terminal CFOA

Parameter	Name	Value	Unit	Ext. by
v_{io}	Input offset voltage	50×10^{-6}	V	DS
i_{io}	Input offset current	50×10^{-9}	A	DS
i_{ib}	Input bias current	187.5×10^{-9}	A	DS
α_{yx}	DC voltage gain between y and x	1		Exp
r_y	Parallel input resistance of the y-terminal	10×10^{6}	Ω	Exp
C_y	Parallel input capacitance of the y-terminal	2×10^{-12}	F	Exp
v_{dpy2}	Input positive saturation voltage	13.5	V	DS
v_{dpy2}	Input negative saturation voltage	–13.5	V	DS
$CMRR$	Common-mode rejection ratio	10^5		DS
f_{pcm}	Upper cut-off frequency	10^5	Hz	E
r_x	Series parasitic resistance of the x-terminal	65	Ω	Exp
L_x	Series parasitic inductance of the x-terminal	10×10^{-9}	H	Exp
C_x	Parallel parasitic capacitance of the x-terminal	2×10^{-12}	F	Exp
$\pm I_{biasx}$	i_x current limiting	7.5×10^{-3}	A	Exp
α_{xz}	DC current gain between z and x	1		Exp
r_z	Parallel output resistance of the z-terminal	2.2×10^{6}	Ω	Exp
C_z	Parallel output capacitance of the z-terminal	5.5×10^{-12}	F	Exp
f_{p2}	Second pole frequency	50×10^{6}	Hz	E
f_{p3}	Third pole frequency	500×10^{6}	Hz	E
v_{dpz}	Positive saturation voltage to z - terminal	10	V	Exp
v_{snz}	Negative saturation voltage to z - terminal	–10	V	Exp
r_o	Output resistance	15	Ω	Exp
L_o	Output inductance	60×10^{-9}	H	Exp
$i_{\max p(n)}$	Short-circuit output current	80×10^{-3}	A	DS
SR_p	Slew rate rising slope	2	V/μs	DS
SR_n	Slew rate falling slope	–2	V/μs	DS
$SVRR$	Supply voltage rejection ratio	4×10^{-6}		DS
i_{cs}	Quiescent current between power supplies	6.5×10^{-3}	A	DS

To obtain the DC transfer characteristic $v_x = f(v_y)$ through simulation, a DC sweep analysis is performed within OrCAD PSpice and SV. The DC sweep analysis in both programs causes a DC sweep to be performed on the op amp. For the DC sweep analysis the level of an ideal voltage source v_y applied to y terminal is swept from 0 to |15| volts by steps of 0.1 V. This means that the voltage v_y has $[(0 + |15|)/0.1] \times 2 = 300$ steps (or simulation points). The transfer characteristics $v_x = f(v_y)$ for the two models at open-circuited terminal x (without load at x terminal) are given in Fig. 13. The voltage clipping limits is obtained at $U_{omy2}^{+} \approx 13.5V$ and $U_{omy2}^{-} \approx -13.5V$. The gain (or slope) α_{yx} for both model between y and x is obtained approximately equal to 1.

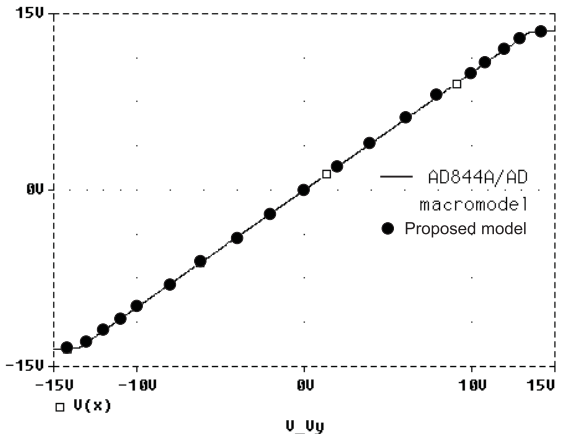

Fig. 13. Voltage transfer characteristics $v_x = f(v_y)$ for open-circuited terminal x – obtained from OrCAD PSpice with AD844A/AD and obtained from SV with the proposed model.

Fig. 14 shows the DC voltage transfer characteristics $v_z = f(v_y)$ for open-circuited terminal z and short-circuited terminal x. The voltage clipping limits is obtained at $U^+_{omx} \approx 10V$ and $U^-_{omx} \approx -10V$. The voltage gain between y and z is $\alpha_{zy} \approx r_z / r_x >> 1$. The α_{zy} obtained from simulation with SV taking into account the parasitic effects has value 33 846 and the value obtained from the simulation of the AD844A/AD macro-model with the OrCAD PSpice program has a value 33 966 (with relative error equal to 0.355%).

Fig. 15 illustrates transfer characteristics $i_z = f(v_y)$ for short-circuited terminal x. The maximum and minimum values of the i_z are determined as $I_{z\max} \approx 7.5mA$ and $I_{z\min} \approx -7.5mA$. The slope defines the transimpedance between z and y and is obtained approximately equal to $1/r_z$.

Finally, the transfer characteristics $v_o = f(v_z)$ of the output buffer is simulated for open-circuited terminal o and short-circuited terminal x. The maximum and minimum values of the v_o are determined as $U^+_{o2m} \approx 10V$ and $U^-_{o2m} \approx -10V$. The slope defines the voltage gain α_{zo} between z and o of both models and is obtained value approximately equal to 1.

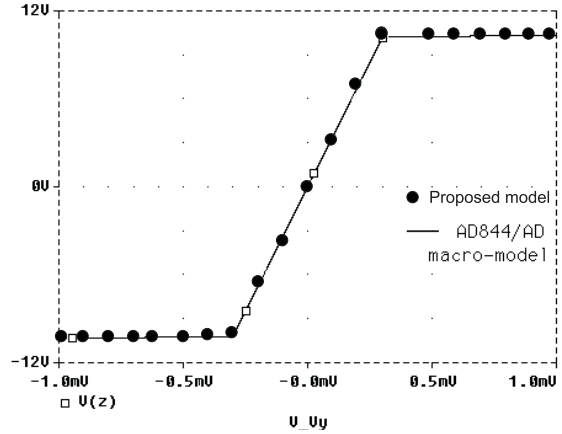

Fig. 14. Voltage transfer characteristics $v_z = f(v_y)$ for open-circuited terminal z and short-circuited terminal x – obtained with AD844A/AD and obtained with the proposed model.

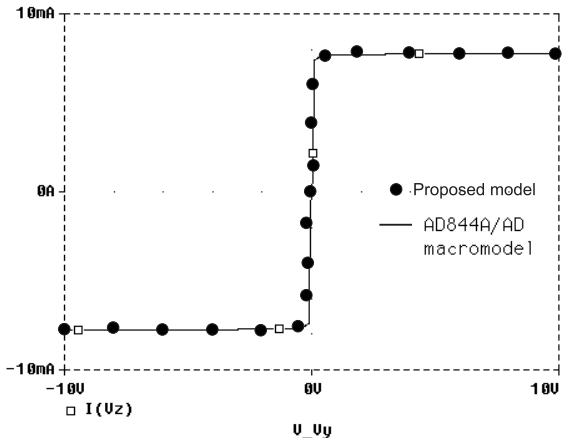

Fig. 15. Transimpedance characteristics $i_z = f(v_y)$ for short-circuited terminal x – obtained with AD844A/AD and obtained with the proposed model.

To obtain the frequency responses $\dot{A}_U = \dot{v}_o / \dot{v}_y$ at $V_{DD} = -V_{SS} = 15V$, $R_L = 500\Omega$ and $T_A = 25°C$ through computer simulations, an AC sweep analysis is performed within OrCAD PSpice and a frequency analysis within SV. The AC analyses cause an AC sweep to be performed on the op amp. AC sweep is a frequency response analysis. In both ECAD systems the simulation programs calculates the small-signal response of the op amp to a combination of inputs by transforming it around the operating point and treating it as a linear circuit. For the AC analysis the tested op amps are without negative feedback and the inverting input is connected to ground. The input sinusoidal signal is applied to the non-inverting input. The frequency of the signal is swept from 10 *Hz* to 100 *MHz* by decades, with 100 points per decade. The input signal is with amplitude $10\mu V$ (the initial phase is equal to zero), to ensure that the output voltage v_o will be with values lower than the $U^{+(-)}_{o2m}$.

The frequency responses $\dot{A}_U = |\dot{A}_U| e^{j\varphi_{A_U}}$ of the two models are plotted in Fig 16. For low frequencies, the $|\dot{A}_U|$ is constant and is approximately equal to $90dB$ (or 31622), and the phase shift φ_{A_U} between the input and output signals is about 0°. For the frequency of the first pole (dominant pole) f_{p1}, approximately equal to $13kHz$, the gains is reduced by 3 dB or (≈ 0.7), as the phase shift is $\approx 45°$. For $f > f_{p1}$, the $|\dot{A}_U|$ decreases with the slope around -20 *dB* per decade, and the phase of the output voltage decreases, as at frequency equal to 1 *MHz*, the φ_{A_U} is about 90°. At a frequency $f_{p2} \approx 50MHz$ the slope of the frequency responses is increasing, as for $f > f_{p2}$ the slope of the $|\dot{A}_U|$ is approximately equal to $-40\,dB$ per decade. The phase decreases, as at frequency around 80 *MHz*, the φ_{A_U} is about 180°. It is notable that for both models the phase continues to increase due to the influence of the third pole f_{p3} and parasitic input capacitances (C_x and C_y).

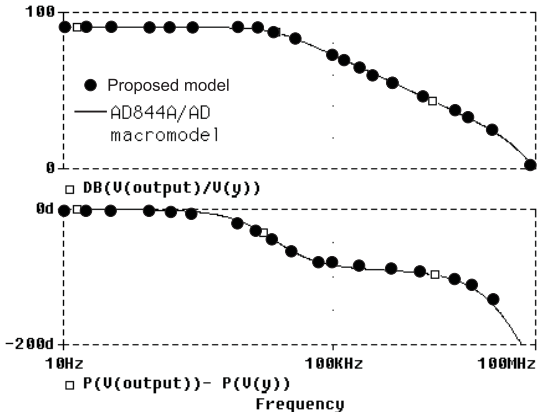

Fig. 16. Frequency response $\dot{A}_U = |\dot{A}_U| e^{j\varphi_{A_U}}$ obtained with AD844A/AD and with the proposed model.

In comparison with the conventional op amps for the CFOAs the inverting and non-inverting input ports are with different impedances. To obtain the non-inverting input impedance ($Z_y = r_y \| C_y$) and inverting input impedance ($Z_x = r_x,\ L_x,\ C_x$) an AC input voltage source v_y is applied to the *y* terminal and an AC sweep (of frequency) analysis is performed within frequency range from 10 *Hz* up to 10 G*Hz*, by decades, with 100 points per decade.

The input resistance r_y and input parasitic capacitance C_y is determined with *x* open and terminal *z* grounded. $r_y \approx 10M\Omega$ is then measured at low frequency and $C_y = 2pF$ deduced from the $-3\,dB$ cutoff frequency ($\approx 8kHz$) of the magnitude of the input impedance at *y* terminal. For the further increase of the input frequency the impedance Z_y decreases.

At low frequency the input resistance at *x* is measured with *x* and *z* grounded. An AC voltage source v_y is applied and an AC sweep (of frequency) analysis is performed. The value of r_x is approximately equal to 65Ω. By increasing the frequency of the input signal the Z_x reached a maximum with value approximately equal to 110Ω at resonant frequency around 1 G*Hz*. The values of $L_x = 10nH$ and $C_x = 2pF$ are calculated from the parameters of the resonant frequency and quality factor, given in (24a) and (24b), respectively.

For verification of the created models in a time domain the small-signal and large-signal transient responses are investigated. To obtain the small-signal transient response at $V_{DD} = -V_{SS} = 15V$, $R_L = 500\Omega$, $C_L = 10pF$ and $T_A = 25°C$ through computer simulations, a transient analysis within OrCAD PSpice and a time-domain analysis within SV is performed. According to the semiconductor data book, both models of four-terminal CFOA are connected in a electronic circuit of inverting amplifier with a voltage gain equal to -1 with resistances in the negative feedback equal to $1k\Omega$. The input pulse signal u_G is with amplitude $\pm 10V$ and rise and fall time equal to $1ns$. The pulse width is $1\mu s$. The time interval for simulation starts at zero and proceeds up to value of final time equal to $10\mu s$ (equal to five periods). As a result of the computer simulations in the form of the time response peaks are caused, and the amplitude reaches approximately $\pm 10.5V$. For the both circuits, the steady-state value of the output signal is reached after damped oscillations. The value of the settling time t_s for the created behavioral model is 93.4 *ns*. In comparison with this value for the PSpice macro--model the t_s is approximately 60 *ns*. According to the data book the typical value of the time setting for the real device is 100 *ns*, determined at a level 0.1 % of the steady-state value. Moreover, the achieved relative error between the semiconductor data book and the simulation results for the proposed model is below 10 %.

The basic parameter associated with large-signal pulse response is the rising and falling slope of the output voltage or the positive and negative slew rates. It is defined as the average time to change the output voltage of the op amp with closed-loop feedback and pulse signal: $SR^{+(-)} \approx \Delta v_o^{+(-)} / \Delta t$.

According to the semiconductor data book to obtain the large-signal transient responses an inverting amplifier with voltage gain equal to -10 is used. The input pulse signal is with the same amplitude $\pm 10V$ and rise and fall times equal to $1ns$. The values of the positive and negative slew rates are obtained as $SR^+ \approx 2000V/\mu s$ and $SR^- \approx -2000V/\mu s$.

Although both simulation programs using similar iterative analysis methods in comparison with the AD844A/AD PSpice macro-model the proposed CFOA model runs about three times as fast on transient analysis. The analysis showed that the CPU time for the proposed model is below 1*s*, while the simulation for the PSpice macro-model is performed for about 3*s*. This is due to the smaller number of controlled sources and passive elements, which contains the behavioral model.

Table III summarizes the comparison of the simulation results and datasheet typical values for AD844A. The analysis of the obtained results shows a relatively good agreement. The maximum value of the relative error is below 5%. For some of the parameters in the semiconductor data book the typical values are missing or for some of them approximate values are given. In these cases, the parameters of the PSpice macro-model are the basis for comparison. In other cases, only the datasheet typical values are used for comparative analysis because there are electrical parameters that are not modeled on the PSpice macro-model.

Table IV and V presents a comparison of the created CCII and CFOA models with known simulation models, reported in the literature.

In Table IV, the available simulation CCII macro-models, proposed in [7] and [9], have linear structures and simulate basic small-signal parameters. The CCII model, presented in [8], is implemented in the PSpice – based circuit simulation platform using standard components, ABM blocks and ideal diodes models. It's created as a sub-circuit and simulate *y* to *x* and *x* to *z* non-linear DC transfer responses. The output voltage excursion is limited by series combination of voltage sources and ideal diodes connected between power supply nodes and y, x and z terminals. For the macro-model, presented in [10], the nonlinear properties are described using nonlinear controlled sources. Also, the model represents the noise effects by two current sources and one voltage source, connected to the CCII terminals. The proposed model is adapted for simulation with SV and does not simulate the

noise effects. The models, reported in [8], [11] and [12] (in Table IV), didn't simulate the input bias currents, non-dominant poles of the frequency responses, *CMRR* versus frequency, *SVRR* versus power supply, z – output voltage limiting [12] and large-signal transient response ([8] and [11]).

According to the output parameters and the number of passive and active components, represented in Table V, the CFOA models generally can be divided into two groups. On the one side, there are relatively simple models suitable for simulating certain characteristics in specific applications [5], [15], [16], [26]. Moreover, these models contain a small number of passive elements and controlled sources. As a result, the computer simulations are performed for a shorter period with good convergence of the computation process. These models are suitable for simulation of complex (multiple-stage) electronic circuits. On the other side is the group of complex models and macro-models containing a large number of controlled sources and passive elements [13], [14], [17], [27]. In particular interest is the macro-model, presented in [14], for which the input stage largely representing the structure of actual device. This model with good accuracy simulates the main DC and AC parameters for small and large input signal. The behavioral model proposed in this work contains a much smaller number of elements, providing the same detail of the analysis.

TABLE III
COMPARISON BETWEEN THE SIMULATION RESULTS AND DS PARAMETERS

Parameter	This model for CFOA	AD844A/AD (Ref. [14])	Datasheet typical value	Units
v_{io}	187.5×10^{-9}	425×10^{-9}	187.5×10^{-9}	A
i_{io}	50×10^{-9}	50×10^{-9}	50×10^{-9}	A
i_{ib}	50×10^{-6}	300×10^{-6}	50×10^{-6}	V
r_y	10×10^{6}	9.67×10^{6}	10×10^{6}	Ω
C_y	2×10^{-12}	2×10^{-12}	2×10^{-12}	F
r_x	65	65	65	Ω
C_x	2×10^{-12}	2×10^{-12}	2×10^{-12}	F
$\pm I_{biasx}$	7.5×10^{-3}	7.46×10^{-3}	7.5×10^{-3}	A
α_{yx}	0.99	1	-	-
v_{dny2} (v_{sny2})	13.51	13.48	13.5	V
α_{zy}	33 846	33 966	-	-
v_{dpz} (v_{snz})	9.98	10.5	10	V
$r_z \parallel C_z$	$2.2 \times 10^{6}\Omega \parallel \parallel 4.5 \times 10^{-12}$	$2.2 \times 10^{6}\Omega \parallel \parallel 5.5 \times 10^{-12}$	$2.2 \times 10^{6}\Omega \parallel \parallel 4.5 \times 10^{-12}$F	-
α_{xz}	0.96	1	-	-
f_{p1}	13×10^{3}	13.43×10^{3}	$\approx 12 \times 10^{3}$	Hz
f_{p2}	50×10^{6}	50×10^{6}	-	Hz
f_{p3}	500×10^{6}	500×10^{6}	-	Hz
CMRR	10^{5}	no	10^{5}	-
f_{pcm}	96.6×10^{3}	no	100×10^{3}	Hz
SVRR	4×10^{-6}	no	4×10^{-6}	-
i_{cs}	6.5×10^{-3}	7×10^{-3}	6.5×10^{-3}	A
SR_p	1.97×10^{3}	1.95×10^{3}	2×10^{3}	V/μs
SR_n	-1.95×10^{3}	-1.93×10^{3}	-2×10^{3}	V/μs
r_o	15	15	15	Ω
L_o	60×10^{-9}	60×10^{-9}	60×10^{-9}	H
$i_{maxp(n)}$	80×10^{-3}	80×10^{-3}	80×10^{-3}	A
t_s	93,4	60	100	ns
CPU time	≈ 1 (0.96 s)	3	-	s

TABLE IV
COMPARISON WITH OTHER CCII MODELS

Parameter	This CCII model	Ref. [7]	Ref. [8]	Ref. [9]	Ref. [10]	Ref. [11]	Ref. [12]
Input characteristics							
Bias current	Yes	No	No	No	No	No	No
Offset current	Yes	No	No	No	No	No	No
Input offset voltage	Yes	No	Yes	No	No	No	No
Input resistance r_y at *y* terminal	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Input capacitance C_y at *y* terminal	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Input resistance r_x at *x* terminal	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Input capacitance C_x at *x* terminal	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Input inductance at *x* terminal	Yes	Yes	Yes	Yes	Yes	Yes	No
x –current, limiting	Yes	No	Yes	No	No	Yes	Yes
Voltage transfer characteristic $v_x=f(v_y)$ for open-circuited x terminal							
y – input voltage range	Yes	No	Yes	No	Yes	Yes	Yes
DC gain α_{yx}	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Voltage transfer characteristic $v_z=f(v_y)$ for open-circuited z terminal and short-circuited x terminal							
z – output voltage range	Yes	No	Yes	No	Yes	Yes	No
DC gain α_{zy}	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Transimpedance characteristic $i_z=f(v_y)$ for short-circuited x terminal							
Transimpedance $r_z \parallel C_z$	Yes	Yes	Yes	Yes	Yes	Yes	Yes
z – output current limiting	Yes	No	Yes	No	Yes	Yes	Yes
Frequency response $A_I=\dot{I}_z/\dot{I}_x$							
DC gain α_{xz}	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Dominant pole at f_{p1}	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Second pole at f_{p2}	Yes	No	No	No	No	No	No
Third pole at f_{p3}	Yes	No	No	No	No	No	No
Input voltage noise density	No	No	No	No	Yes	No	No
Input current noise density	No	No	No	No	Yes	No	No
Frequency response of the CMRR							
DC value of the *CMRR*	Yes	No	No	No	No	No	No
Upper cut-off frequency	Yes	No	No	No	No	No	No
Offsets according to power supply – offset current, SVRR, V_{ref} and *i_{cs}*							
Output offset current	Yes	No	No	No	Yes	No	No
SVRR	Yes	No	No	No	No	No	No
Power-supply common terminal	Yes	No	No	No	No	No	No
Quiescent current	Yes	No	No	No	No	No	No
$r_x(I_{bias})$ $r_z(I_{bias})$	Yes	No	No	No	No	No	No
Large-signal transient response							
Slew rate rising slope	Yes	No	No	No	No	No	Yes
Slew rate falling slope	Yes	No	No	No	No	No	Yes
Year	2018	1997	1998	2001	2005	2010	2017

TABLE V
COMPARISON TO OTHER CFOA MODELS WITH RESPECT TO OUTPUT PARAMETERS AND NUMBER OF COMPONENTS

Parameter	This model	Ref. [13]	Ref. [14]	Ref. [5]	Ref. [15]	Ref. [16]	Ref. [26]	Ref. [27]	Ref. [17]
Output characteristics and parameters in saturation mode of operation									
Output voltage range	Yes	Yes	Yes	No	No	No	No	Yes	Yes
DC voltage gain α_{zo}	Yes	No	Yes	No	No	Yes	No	Yes	Yes
Short-circuit output current	Yes	Yes	Yes	No	No	No	No	Yes	No
Frequency dependence of the output impedance									
Output resistance r_o	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
Output inductance L_o	Yes	No	Yes	No	No	Yes	No	No	No
Large-signal transient response									
Slew rate rising slope	Yes	Yes	Yes	No	No	No	No	No	Yes
Slew rate rising slope	Yes	Yes	Yes	No	No	No	No	No	Yes
Component list									
Passive components	9	9	30	4	8	13	3	5	9
Diode	-	8	10	-	-	-	-	-	-
Transistor	-	-	4	-	-	-	-	-	-
Independent source	8	4	10	-	2	-	-	7	-
Controlled source	6	8	13	3	3	4	2	3	3
Year	2018	1990	1990	1994	1996	1999	2009	2010	2015

V. MODELS VALIDATION

For purpose of validation the behavior of the practical electronic circuits employing standard PSpice macro-models and proposed models are compared. The intended computer simulations are performed under the same conditions and the same input signals.

The first circuit, an object of analysis and simulation testing, is a universal filter using two four-terminal CFOAs, reported in [34]. This filter (Fig. 17) can realize low-pass, band-pass, high-pass, band-reject (or notch) and all-pass filters from the same configuration.

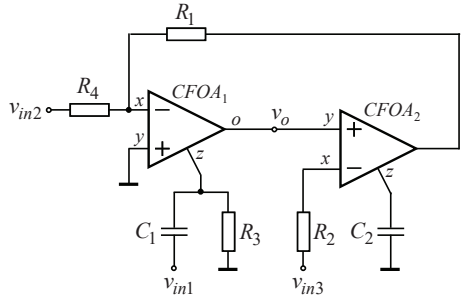

Fig. 17. Universal filter using two four-terminal CFOAs [34].

The operation of the two active filters has been analyzed using AD844A as a four-terminal CFOA, biased with ±15V. The universal filter example was designed for center (notch) frequency $f_p = 10kHz$ and quality factor $Q = 0.707$ based on the Butterworth approximation method. Capacitors $C_1 = C_2 = 2.2nF$ were chosen. Other parameters are: $R_1 = R_2 = R_4 = 7.15k\Omega \pm 1\%$ and $R_3 = 4.99k\Omega \pm 1\%$. For computer simulation AC sweep and transient analysis were performed using the proposed VHDL-AMS model and AD844A/AD PSpice macro-model.

Fig. 18 shows the simulation results for both filters. In the transmission band the frequency responses are not ringing and decreased monotonically with increasing the frequency of the input signal. The slope is approximately equal to $-30dB/dec$. For the notch filter the stop-band attenuation ratio at 10kHz is smaller than $-40dB$. The maximum relative error between the two simulation models for the whole working frequency range is not greater than 2%.

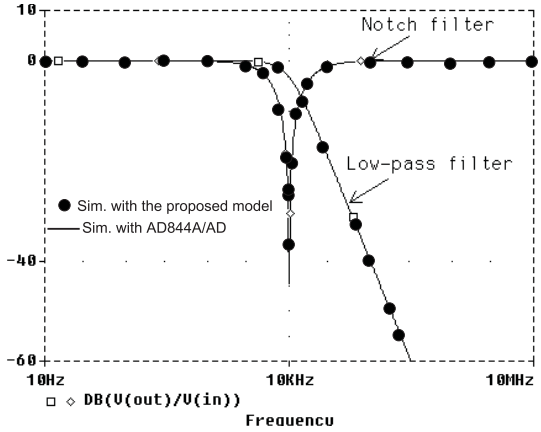

Fig. 18. Amplitude-frequency responses for a low-pass and notch filter (Fig. 17), obtained with AD844A/AD (—) and with the proposed model (●) as active building blocks.

The simulation results obtained from SV confirm the results of the simulation analysis for the electronic circuit, using AD844A/AD. At low frequencies for the both filters the voltage gain is equal to 1. For a frequency equal to 10 *kHz* the gain of the low-pass filter decreases by $-3dB$ compared to the DC value. The phase shift at 10 *kHz* of the output signal is around $-90°$ (Fig. 19).

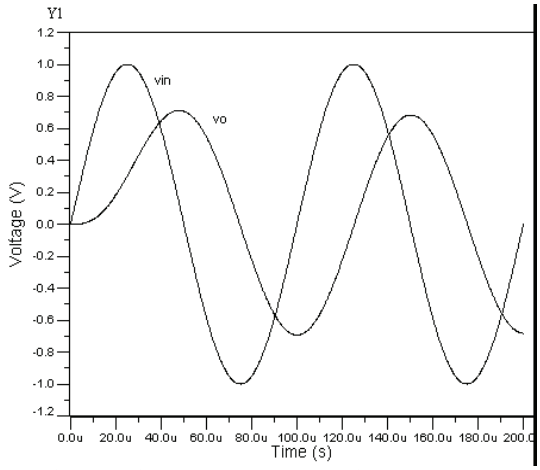

Fig. 19. Simulation of the input and output signal at frequency equal to 10*kHz* of the low-pass filter with the proposed CFOA model.

Upon simulation testing of the notch filter with proposed filter in time domain in a change of the frequency from 1 *kHz* to 10 *MHz* (at 1 *V* amplitude of the input signal) do not obtained visible distortion in the output signal (Fig. 20) from the normal form. The *THD* = 0.071 % at 1 *kHz* and 0.179 % at 10 *MHz* from the OrCAD PSpice simulation with AD844A/AD. The analysis of CPU time on transient analysis of the electronic circuit within frequency range of the input signal from 1 *kHz* to 10 *MHz* is about 3*s* by using the OrCAD PSpice program and about 1s by using the SV program.

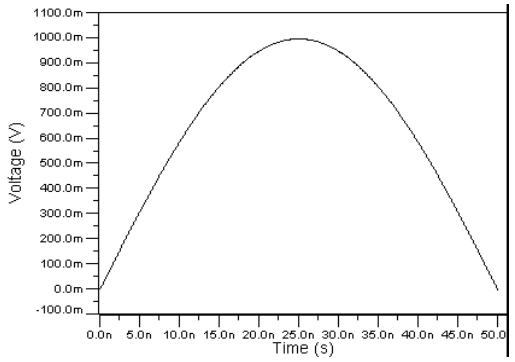

Fig. 20. Form of the simulated output signal at frequency equal to 10*MHz* of the notch filter with the proposed CFOA model.

The second electronic circuit, an object of simulation and experimental test is a current controlled band-pass filter using CCCII+s, operating in a current mode [28]. For this filter (Fig. 21) the central frequency f_0 can be adjusted by the bias currents I_{bias1} and I_{bias2} of the used current conveyors. It uses only two CCCII+s and two capacitors.

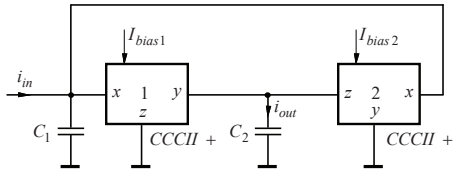

Fig. 21. Current-controlled band-pass filter implemented from CCCII+ [28].

The operation of the filter has been analyzed employing a single monolithic op amp OPA860 [35] used as a CCCII+, biased with ± 5 *V*. The model parameters for the OPA860ID are as follows: $i_{ib} = 16.5\mu A$, $i_{io} = 27\mu A$, $v_{io} = 3mV$, $\alpha_{yx} = \alpha_{xz} = \alpha_{zo} \approx 1$, $r_y = 455k\Omega$, $C_y = 2.1pF$, $C_x = 1pF$, $L_x = 10nH$, $v_{dpy2} = 4.2V$, $v_{sny2} = -4.2V$, $r_z = 54k\Omega$, $C_z = 1.3pF$, $f_{p2} = 230MHz$, $f_{p3} = 1GHz$, $v_{dpz} = 4.7V$, $v_{snz} = -4.7V$, $SR_p = 900V/\mu s$, $SR_n = -900V/\mu s$, $CMRR = 10^5$, $f_{pcm} = 1kHz$, $SVRR = 20\mu A/V$, $SUPPLY\_CURRENT = 0.14mA$ and $I_{bias} = 11.2mA$.

Considering CCCII+ to be characterized by the hybrid matrix, given in (2), the basic parameters current transfer function are: $\omega_0 = 1/r_x\sqrt{C_1C_2}$ – central frequency, $Q_0 = 0.5\sqrt{C_1/C_2}$ – quality factor and $H_{BP} = 0.5$ – gain.

Formula (31) shows that the value of the central frequency is adjustable by the bias current without affecting the Q_0.

Capacitor $C_1 = 33nF$ was chosen and the capacitor C_2 was found to be equal to $510pF$. Fig. 22 displays the band-pass functions for the different values of the bias current I_{bias}: 0.5*mA*, 0.7*mA* and 1.25*mA*. For the experimental study the circuit were implemented on a FR4 printed circuit boards laminate with surface-mount device passive components for the capacitor C_1 and C_2.

Thus, the simulated value for the frequency f_0 are $1.29MHz$, $2.44MHz$ and $3.89MHz$, respectively, and correspond to the measured values are $1.34MHz$, $2.56MHz$ and $4.07MHz$, respectively. The maximum error between the calculated values of the center frequency and the simulation results is not greater than 5%. Moreover, it can be seen that the f_0 can be tuned electronically without affecting the Q_0.

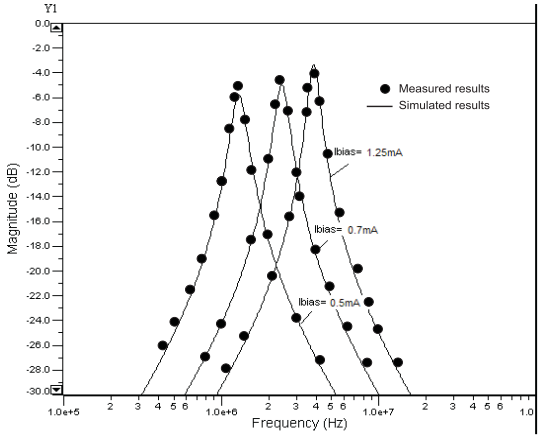

Fig. 22. Amplitude-frequency responses at bias current equal to 0.5mA, 0.7mA and 1.25mA for the band-pass filter (Fig. 21).

VI. CONCLUSION

In this paper, behavioral non-linear VHDL-AMS models for the monolithic CCII+s, CCII–s and CCCIIs were presented. Based on the proposed CCII+ model improved models for monolithic three-terminal CFOAs and four-terminal CFOAs were developed. For the proposed models, simplification and build-up techniques known from the macro-modeling of conventional monolithic op amps are adapted.

The created VHDL-AMS models of CCIIs show a good agreement of the simulated parameters with the datasheet typical values for the CCII+ part in AD844A. In comparison with the available CCII – based models also the proposed model takes into account the input offsets, non-dominant poles in the frequency response, *CMRR* versus frequency, *PSRR*, midpoint related to the supply voltages, terminal voltage/ current operating ranges (in comparison with [7] and [9]), slew rates, current controlling of the r_x and r_z and their temperature drift. This makes the created models useful for simulation of high-frequency (with cut-off frequency > 1*MHz*) amplifiers and active filters, for which it is necessary to precisely evaluate of the shape of the amplitude-frequency and phase-frequency responses at differential and the common-mode input signals. Also, the model is suitable for simulation of various type oscillators, because for them it is important to explore the large-signal transient responses. In this way, it is possible to determine the oscillation conditions of the circuits.

The comparative analysis between the proposed model of four-terminal CFOA and macro-model for CFOA in [14], showed that the maximum value for the relative error of the modeled DC and AC parameters does not exceed 5%, which guarantee sufficient degree of accuracy. Moreover, the

proposed model is further modeled the DC value of *SVRR* parameter and frequency dependence of the *CMRR*. An important advantage of the developed model is the use of the VHDL-AMS language, which allows describing the structure of the model with smaller number of passive elements and controlled sources. By using VHDL-AMS the complete set of equations that representing the behavior of the real device can be implemented by combining both behavioral elements and structural description as a net-list. As a result, the CPU efficiency improves and the proposed model runs about three times as fast on transient analysis.

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