Science, Technology and Innovation
ISSN 2544-9125 ▪ 2021; 12 (1): 37–44
doi: 10.5604/01.3001.0015.2999

STI • 2021;12 (1): X-X

Synchronization of transmission systems with ANS-DM codecs

Juliusz Godek[1, B,E-J], Ryszard Golański[1, A-C,H-J]

[1]University of Applied Sciences in Tarnow, Politechnic Faculty, Department of Electronics, Telecommunications and Mechatronics ul. Mickiewicza 8, 33-100 Tarnów, Poland

Original article

Abstract

Adaptive Delta Modulation with Non-uniform Sampling (ANS-DM) is one of the waveform coding techniques, where a sampling instant and a quantization step size are adapted to the signal. The ANS-DM modulator produces an output binary stream, that carries information about the signal and includes necessary data of coder parameters (sampling instant and quantization step). In the demodulator, these values are recovered for proper signal reconstruction.

The paper reports the problem of synchronizing clocks (transmitting and receiving) in the (ANS-DM) delta codecs systems. The original synchronization method, valuable in systems dedicated to the transmission of the bits with variable time duration was projected and experimentally verified. Performed measurements and observations have shown the elimination of the synchronization loss phenomenon.

Keywords

- delta modulation
- non-uniform sampling
- Adaptive Delta Modulation with Non-uniform Sampling (ANS-DM)
- digital PLL
- digital transmission
- one-bit codec delta

Authors contributions

A – Conceptualization
B – Methodology
C – Formal analysis
D – Software
E – Investigation
F – Data duration
G – Visualization
H – Writing – original draft preperation
I – Writing, reviewing & editing
J – Project administration
K – Funding acquisition

Corresponding author

Juliusz Godek
e-mail: j.godek@pwsztar.edu.pl
University of Applied Sciences in Tarnow
Department of Electronics,
Telecommunications and Mechatronics
ul. Mickiewicza 8
33-100 Tarnów, Poland

Article info

Article history

- Received: 2021-09-11
- Accepted: 2021-09-27
- Published: 2021-09-27

Publisher

University of Applied Sciences in Tarnow
ul. Mickiewicza 8, 33-100 Tarnow, Poland

Financing

This research did not received any grants from public, commercial or non-profit organizations.

Conflict of interest

None declared.

Introduction

Previous research works [1, 3, 4] allow to affirm, that reaching high accuracy in a wide dynamic range, with the use of the uniform sampling ADM converters, is not possible. Hence, using the 1-bit delta modulation is proposed, in which sampling intervals are adapted to the input analog signal. The results of simulating works showed that for non-stationary sources, the adaptive sampling delta converters uncover higher coding efficiency than the previous proposals, based on uniform sampling methods.

The simple synchronization method, useful in systems dedicated for transmission of variable duration of bits is presented in the article [2].

In the work, the synchronization mechanism with temporary increasing or decreasing the pulse's number of the main clock in the decoder is proposed [2, 6]. The method provides the correct synchronization of the transmission systems with a variable time base. The coder's clock should be slower or faster than in the decoder.

The analysis presented in the paper is focused on discovering the implementation of synchronizing mechanism, working irrespective of the sign of the difference between the clock frequency in the coder and decoder.

ANS-DM modulation

Several military and commercial systems use delta modulations with uniform and non-uniform sampling. Many semiconductor vendors produce specialized IC's based on delta system (pacemakers, CAT scans, MRI scan). The very spectacular application of the delta technique has been the voice encoding system used in the Shuttle system. It has been chosen by NASA because of its tolerance to channel errors [3, 4].

A characteristic feature of ANS-DM delta modulation is the stream with a variable duration of bits, that carries information of the next value of sampled amplitude and the next duration of bit.

ANS-DM (Adaptive Non-uniform Sampling Delta Modulation [3]) codecs are 1-bit delta converters with step size and sampling instant adaptation. NS-DM (Non-uniform Sampling Delta Modulation [4]) codecs are 1-bit delta converters with sampling instant adaptation only. Step size is fixed.

Adaptation of two parameters (ANS-DM) makes the hardware implementation of the delta codec more complicated in relation to the solutions with one parameter adaptation (NS-DM) but increases the quality of conversion (SNR). The total dynamic range (DR) of the delta converters with two parameters adaptation is a product of the companding gain of each parameter [3, 4]. For the input signal $x(t)$ the predicted signal $s(t_i)$ at time t_i (Figure 1) is given by expression (1):

$$s(t_i) = s(t_0) + \sum_{n=1}^{i-1} k_i d_i \tag{1}$$

where: $di = sgn[x(ti) - s(ti)]$, and: ki – i-th step size.

The output code stream is:

$$b_i = \begin{cases} 1 & for \quad d_i = 1 \\ 0 & for\, d_i = -1 \end{cases} \tag{2}$$

where: bi – the digital value of the output bit,

Let τ_s be the sampling instant. The sampling instant $\tau_s = ti_{+1} - t_i$ vary according to the characteristics of $x(t)$ thus the next sampling time t_{i+1} is expressed as:

$$t_{i+1} = t_i + \tau_s \tag{3}$$

Value of the sampling interval τsi is determined by the algorithm:

$$\tau_s = \begin{cases} K1 \cdot \tau_{s-1} & for \quad d_i = 1 \\ K2 \cdot \tau_{s-1} & for\, d_i = -1 \\ \tau_{s0} & other \quad cases \end{cases} \tag{4}$$

where: $K1$, $K2$ are constant factors of interval time modification and $K1 < 1 < K2$;

Formula (4) represents the 3-bit *Zhu adaptation algorithm* of the change of the sampling interval [4].

Generally, in the ANS-DM modulator algorithm, the limitation of the maximum and minimum sampling interval values are:

$$\begin{aligned} &\tau_s = \tau_{smax} \text{ if } K2\,\tau_s > \tau_{smax} \\ &\text{and} \\ &\tau_s = \tau_{smin} \text{ if } K1\,\tau_s < \tau_{smin} \end{aligned} \tag{5}$$

where: τ_{s0} – start sampling and this value decides about the average output bit rate and $\tau_{smin} < \tau_{s0} < \tau_{smax}$.

Quantization step size k_i adaptation is determined by the algorithm [3, 4]:

$$k_i = \begin{cases} k_{i-1} \cdot P \\ k_0 \quad other \quad cases \end{cases} \tag{6}$$

where: P is the constant factor of the step-size modification with $1 < P$. Generally in the ANS-DM coder algorithm the limitation of the maximum and minimum step-size values are:

$$\begin{aligned} &k_i = k_{imax} \text{ if} \\ &Pk_i > k_{imax} \text{ and } k_0 = k_{min} \end{aligned} \tag{7}$$

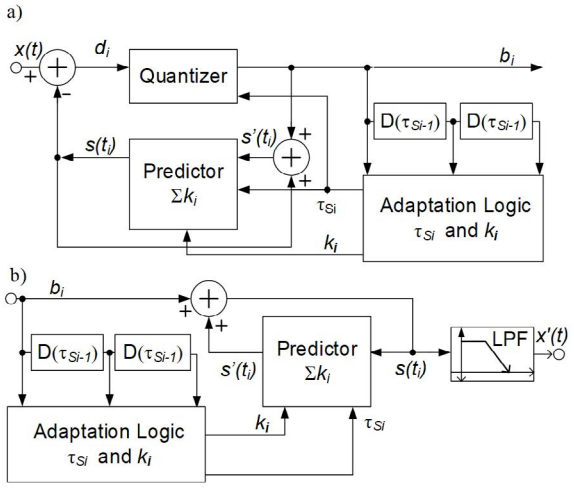

Figure 1. Block diagram of ANS-DM codec: a) coder, b) decoder

Formulas (4) and (5) represent the 3-bit adaptation algorithms of the change of the sampling interval. One can see that the ANS-DM output binary stream carries the information about the sampling interval and the step values allowing reconstruction of the input signal. So that in the decoding process the irregular staircase signal can be recovered.

Table 1. The logic of modification function of interval and step size in the ANSDM delta modulation

b_{i-2}	b_{i-1}	b_i	k_{i-1}	τ_{i-1}	k_i	τ_i	step	interval
0	0	0	0	0	0	1	$k0$	$K1\ \tau_{s-1}$
			0	1	1	0	$k_{i-1}P$	τ_{s0}
			1	0	1	1	$k_{i-1}P$	$K1\ \tau_{s-1}$
			1	1	1	1	$k_{i-1}P$	$K1\ \tau_{s-1}$
1	0	0	H	H	0	0	$k0$	τ_{s0}
0	1	0	H	H	0	1	$k0$	$K2\ \tau_{s-1}$
1	1	0	H	H	0	0	k_0	τ_{s0}
0	0	1	H	H	0	0	k_0	τ_{s0}
1	0	1	H	H	0	1	k_0	$K2\ \tau_{s-1}$
0	1	1	H	H	0	0	k_0	$\tau s0$
1	1	1	0	0	0	1	k_0	$K1\ \tau_{s-1}$
			0	1	1	0	$k_{i-1}P$	τ_{s0}
			1	0	1	1	$k_{i-1}P$	$K1\ \tau_{s-1}$
			1	1	1	1	$k_{i-1}P$	$K1\ \tau_{s-1}$

The first five bits are taken into account to designate the actual step and interval. 0 descripted return to the starting value, 1 descripted other change, *H* means irrelevant data (4), (6).

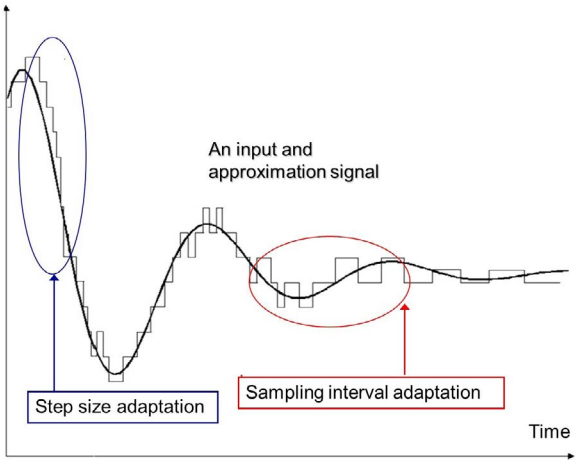

Figure 2. The waveform of the coded signal by ANS-DM modulator

ANS-DM modulation bases on the (4) and (6) functions which describe modifying the sampling interval and the step size according to the time-varying slope characteristics of the input signal. In this way, an ANS-DM approximation stair waveforms (Figure 2) are better fitted to the source signals than other delta modulations (LDM, NS-DM).

ANS-DM encoder output stream carries the information about sampling duration and quantization step size values [3, 5].

The mechanism of return to the starting sampling duration τ_{s0} (5) and to the starting step size q_0 (5) in the ANS-DM coder increases the tolerance to channel errors and provides to the synchronization when the decoder is turned on.

Design of the ANS-DM implemented in the transmission system

The ANS-DM encoder and decoder implemented using A/D and D/A converters and PLD devices were used for tests. At the encoder input, an amplifier with software adjustable gain is placed (Figure 3). Its output is connected to the A/D converter, which generates (with the base clock cycle $1/f_b$ = 720 ns) 14-bits length digital representation of the instantaneous value of the analog input signal. After reducing the representation to 12 bits (due to the resolution of the D/A decoder) it is

compared with the value at the output of the predictor (Figure 2). Depending on which signal is greater, the output of the encoder produces a logical zero or one. LDM, NS-DM, ANS–DM encoding methods, differ mainly only in the construction of the predictor. Basic clock signal controlling a decimation module, comparator, and predictor is derived from the main clock signal (f_m = 50 MHz) which controls the A/D work [6, 7, 8].

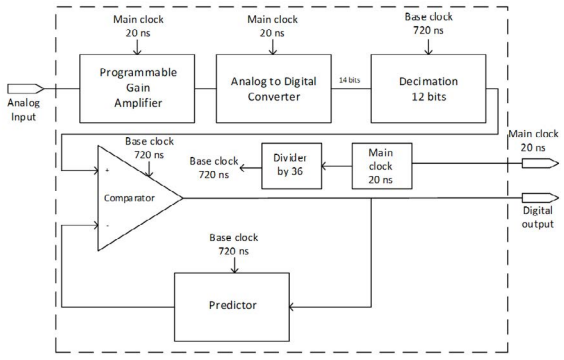

Figure 3. Block diagram of an encoder ANS-DM trainer

Decoder (Figure 4) contains a predictor and 12-bit D/A converter. On the basis of the subsequent one-bit digital values from the encoder output, the predictor generates consecutive 12-bit words, approximating the instantaneous values of the input signal. These words were given to the input of the D/A and consequently generate on its output staircase signal, approximating the signal at the encoder input. Similar to the operation in the encoder, D/A converter is controlled by the main clock.

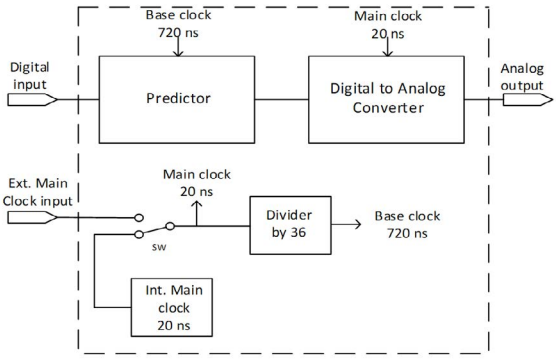

Figure 4. Block diagram of a decoder ANS-DM trainer

Just as in the encoder, the operation of the predictor in the decoder module is controlled by the base clock (720 ns) produced from the main clock. As the main clock of the decoder, an internal generator or externally supplied signal (eg. from the encoder) can be used (Figure 4).

All implemented algorithms work properly and allow reconstructing the analog input signal at an SNR ratio above 20 dB [7].

Synchronization problems

Synchronization is an act of coordination processes in time. In practice, it should lead to the compatibility of two or more periodic phenomena. In the case of data transmission [6, 8, 9] synchronization means the delivering and tracking (or only tracking) of the clock signal in the receiver in comparison to the information contained in the received signal.

In one of the best known method of the clock signal synchronization is embedded into the transmitted bit stream and next extracted by the receiver. An alternative method to encoding the clock in the transmitted bitstream is to apply a constant clock source at the receiver which is kept in time synchronism with the incoming data bits. In this technique, it is required to encode the data in such a way that there is all time enough bit transitions in the transmitted waveform to permit the receiver clock to be resynchronized at frequent intervals. Usually, the classical digital phase-locked loop (DPLL) is the method used to maintain bit synchronism in systems with constant clocks. DPLL needs only very small correcting at irregular intervals in order to work properly. Hence, to take advantage of DPLL, the main clock source (crystal-controlled oscillator) should hold its frequency sufficiently stable.

In the paper, the method of synchronization employing temporary adding or removing of a single main clock period has been applied in the decoder.

To synchronize the coder-decoder system many methods base on using information that comes from data signal on the decoder input and controlling its main clock (Figure 4). In the testing ANS-DM transmission system to prevent too high phase shifting that cause breaking the synchronization (Figure 4) a method based on temporary changing the number of clock pulses was applied in the decoder.

The previously described parameters of codecs allow keeping synchronization by changing the number of main clock pulses equal to the temporary difference between the period of the main clock in the coder and decoder. The additional clock pulses are inserted or removed in this part of the basic clock waveform, which does not affect the work of the predictor and D/A (Figure 5).

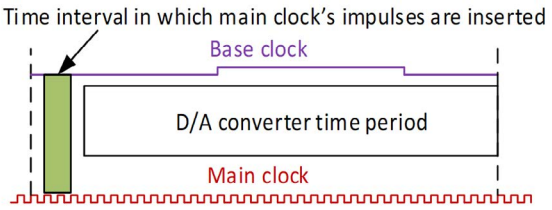

Figure 5. Timing diagram of the decoder synchronization method, based on clock pulses insertion

Experimental studies have shown the elimination of the synchronization loss phenomenon, which is typical in systems of encoder and decoder with independent clocks.

Analysis has been focused on the proposed implementation of synchronizing mechanism, working irrespective of the sign of the difference between the clock's frequency in the coder and decoder.

Proposition of the synchronization methods addressed to transmission system with variable duration of bits

A. Synchronization procedure with decreasing of the main clocks ratio division in decoder

There was decided to use for the synchronization a technique of temporarily decreasing the number pulses of the main clock decoder. Base clock pulses are used for the measurement of the main clock frequency deviation between transmitter and receiver. If the maximum clock frequency in the D/A converter is used, this method is applicable only when the main clock frequency in the receiver (decoder) is higher than the main clock frequency of the transmitter (coder). A block diagram of synchronization procedures in the decoder is shown in Figure 6.

In described transmission system too high phase shift causes breaking of the synchronization. To protect the transmission system against the synchronization breakdown the method employing a temporary decreasing number of the main clock pulses (adding of single main clock period for example) has been applied in the decoder. Measuring and control circuits (Figure 7b) have to be implemented for this purpose [8].

The previously described parameters of main generators and codecs allow keeping synchronization by adding one of the main clock periods to equal the temporary difference between the period of the main clock in the coder and decoder. The added period of the clock is inserted in this part of the base clock waveform, which does not affect the work of the predictor and D/A converter (Figure 5, 7).

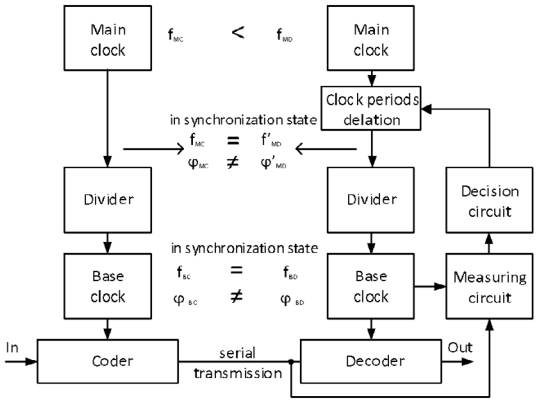

Figure 6. Synchronization procedure with decreasing of the number of the main clock periods in the decoder in transmission systems with variable duration of bits

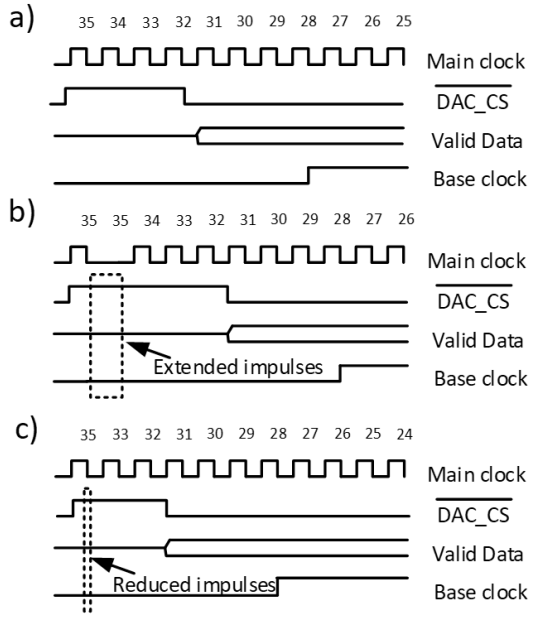

Figure 7. Synchronization for ANS-DM: a) synchronization state, b) main clock modification causes extending all produced signals, c) main clock modification causes reducing all produced signals

The proposition of this synchronization mechanism is based on the assumption, that the crystal oscillator (main clock) in the transmitter has a lower frequency

than the clock of the receiver. The idea of the proposed method (Figure 7b), is based on the temporal extension of the low state of the main clock (for one period). This method of synchronization procedure does not decrease the maximum rate of transmission.

B. Synchronization procedure with increasing of ratio division the main clock

In case of some reason that is impossible to use the main clock of a coder with a lower frequency than used in the decoder, the procedure of increasing the main clocks ratio division is proposed (Figure 8).

The method based on temporarily increasing the number of pulses of the main clock can be applied in the decoder. However, this solution takes a risk of disturbing predictor and D/A converter work. Moreover, this method can be applied only when the frequency of the main clock in the decoder is lower than the maximum operating frequency of A/D and D/A converters (Figure 7c).

This method reduces conversion time by one pulse of the main clock. To reach synchronization simplified digital phase detector base clock is used. In this way, the basic frequencies of the receiver and transmitter clock reach the same value. Moreover, the phase of the base clock in the receiver is synchronized with the phase of the base clock in the transmitter. However, the frequency and phases of the main clocks are different. The period of the base clock is increased by one period of the main clock. The block diagram of the circuit, which allows synchronizing receiver base clock and transmitter base clock, on condition that transmitter frequency of the main clock is grater then receiver frequency of the main clock is shown in Figure 8.

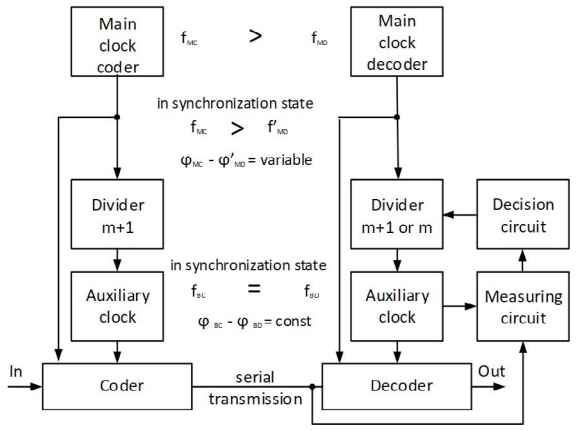

Figure 8. Functional diagram of synchronization procedure with increasing of the number main clock periods

For this method of synchronization maximum rate of transmission is decreasing $1/m$ (section VI) times. Where: m – the ratio of division between main and base clock.

C. The proposition of synchronization procedure with removing or increasing of the clock pulses number in the decoder

Analysis in this section is focused on discovering of synchronizing mechanism, working irrespective of the sign of the difference between the clock's frequency in the coder and decoder.

Combining described in section A and B methods allows, independently of difference sign main clocks frequency, achieve synchronization:

- on main and base clocks level - if the temporary value of clock frequency in the transmitter is lower than the temporary value of clock frequency in the decoder;
- only on base clocks level - in the opposite case.

The block functional diagram of the circuit joining together both mentioned methods is shown in Figure 9.

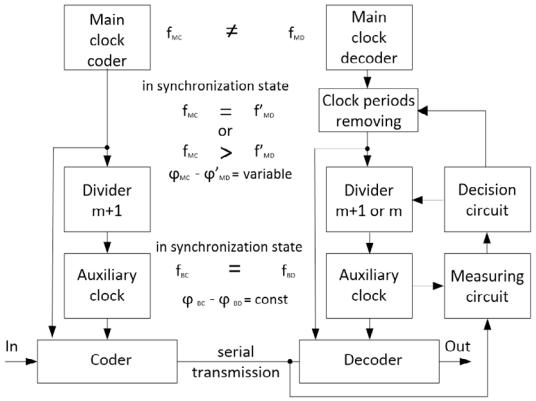

Figure 9. Functional diagram of synchronization procedure with removing of the main clock pulses in decoder and with increasing of the main clocks ratio division

In that method of synchronization, the maximum rate of transmission is $1/m$ (section VI) times reduced.

It should be noted here that with slight differences in the frequency of the main clocks of the transmitter and receiver, the decision mechanism will be activated relatively rarely. For generators with an accuracy of ± 50 ppm, the system should operate once every 10,000 pulses of the master clock [9].

Constraints of the proposal methods of synchronization

For the methods presented in section V (A, B, and C), the maximum frequency difference between the main clock of the coder and decoder is [8, 9]:

$$\Delta f_{max} = f_C \frac{k-1}{2^N - 1} \frac{K_S}{K_F} \tag{8}$$

where:
$f_C \approx f_{MC} \approx f_{MD}$ – the clock main frequency of the transmitter or receiver;
$k \approx m/2$ – the received slope counted with main clock periods;
N – the A/D converter bit resolution;
m – the ratio of division between main and base clock;
K_S – the ratio between maximal ANS-DM step size and A/D converter absolute voltage resolution;
K_F – the ratio between maximal A/D converter frequency and maximal ANS-DM frequency.

With m about 40 and a resolution of N equal to 12, and assume that the coefficients $K_S \approx K_F$, fraction in the formula is around 0.005 (500 ppm). For a resolution of N equal to 16, we get 0.0003 (30 ppm). It follows that synchronization can be difficult to achieve with a high bit resolution [9].

Some results of experimental research based on ANS-DM trainer modules

Performed measures and observations, with different combinations of applied crystal oscillators, have shown elimination of the synchronization loss phenomenon. The test has been doing continuously for several days with different values of temperatures of the crystal oscillator in transmitter and receiver.

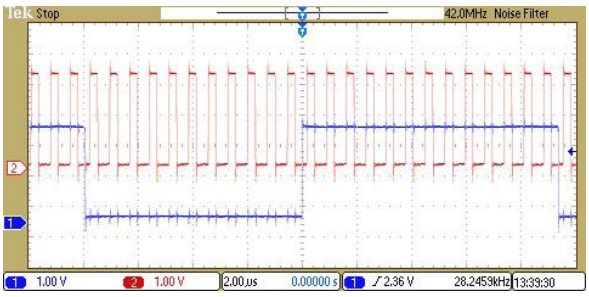

Figure 10. ANS-DM data (blue waveform) and the main clock (red waveform) are in the background

Figure 10 shows ANS-DM received data stream with variable duration (blue waveform) and base clock (red waveforms) in the background.

Conclusions

Functioning of the 1-bit delta A-D and D-A converters with adaptation step size and sampling interval has been presented (ANS-DM). The studies of the synchronization procedures in transmission systems with variable lengths of bits are shown.

The ANS-DM trainer module of transmission system with non-uniform delta codecs sampling was developed. The universal testing platform with the ability to implement different delta codec algorithms and making studies of synchronization methods for delta codecs with non-uniform sampling rates have been used.

Analysis in the work is focused on discovering of synchronizing mechanism, working irrespective of the sign of the difference between the frequency of the clock in the coder and decoder. It means that mechanism of both inserting and removing of the pulses the main clock should be used in the decoder.

These methods provide the accurate synchronization of the bitstream transmission with a variable sampling interval.

The implementation of the proposed synchronization mechanisms increases the complexity of the decoder circuit only by an average of less than one percent.

The mechanism that uses the pulses removal of the main clock in the decoder does not introduce any additional delays in the conversion process.

On the other hand, inserting virtual main clock periods requires increasing the period's length of the base clock in both the encoder and the decoder. This lengthens the basic signal processing period, resulting in a reduction of the upper cut-off frequency of the converted analog signal.

References

[1] Marvasti F. Nonuniform sampling. Theory and practice. New York: Kluwer Academic Publishers; 2001. doi: https://doi.org/10.1007/978-1-4615-1229-5.

[2] Godek J, Golański R, Kołodziej J, Stępień J. New synchronization method for transmission systems with variable length of bits. International Journal of Electronics and Telecommunications. 2015;61(1):31–36. doi: https://doi.org/10.1515/eletel-2015-0004.

[3] Golański R. A/D and D/A delta converters with adaptive sampling–methods analysis and performances

evaluation. Kraków: Akademia Górniczo-Hutnicza Uczelniane Wydawnictwa Naukowo-Dydaktyczne; 2005.

[4] Zhu YS, Leung W, Wong CM. Adaptive non-uniform sampling delta modulation for audio/image processing. IEEE Transactions on Consumer Electronics. 1996;42(4):1062–1072. doi: https://doi.org/10.1109/30.555910.

[5] Golański R. Study on the dynamic range of delta modulations with time-varying sampling periods. IEEE Signal Processing Letters. 2004;11(8):666–670. doi: https://doi.org/10.1109/LSP.2004.831727.

[6] Bregni S. Synchronization of digital telecommunications networks. New York, Chichester: John Wiley and Sons; 2002. doi: https://doi.org/10.1002/0470845880.

[7] Godek J, Golański R, Kołodziej J, Stępień J. Transmission system with variable duration of bit – proposal of synchronization. In: 2014 International Conference on Signals and Electronic Systems (ICSES). Piscataway, NJ: Institute of Electrical and Electronic Engineers (IEEE); 2014. doi: https://doi.org/10.1109/ICSES.2014.6948717.

[8] Godek J, Golański R, Machowski W, Kołodziej J, Stępień J. Proposition of the full synchronization method for transmission systems with variable duration of bits. In: 2016 International Conference on Signals and Electronic Systems (ICSES). Piscataway, NJ: Institute of Electrical and Electronic Engineers (IEEE); 2016. doi: https://doi.org/ 10.1109/ICSES.2016.7593864.

[9] Godek J. Adaptacyjny, niskostratny kodek delta z nierównomiernym próbkowaniem – problemy synchronizacji i rozwiązania układowego w technologii CMOS [Adaptive, low loss delta codec with nonuniform sampling – synchronization problems and systemic solution in CMOS technology]. Doctoral dissertation. Kraków: AGH University of Science and Technology. Faculty of Computer Science, Electronics and Telecommunications; 2016.