Small-Signal Parameters of the VeSFET and Its Application in Analog Circuits

Dominik Kasprowicz, and Bartosz Swacha

***Abstract*—The Vertical Slit-based Field-Effect Transistor (VeSFET) is a novel junctionless device with two identical, independently controlled gates. The VeSFET, so far prototyped only as single-device test structures, has been considered in the literature exclusively as a component of digital systems. This article shows that the device's properties make it attractive also for the analog designer. Some of the VeSFET's analog-design related parameters are compared with those of the MOSFET of the corresponding technology node. Subsequently, a two-stage Miller operational transconductance amplifier (OTA) is proposed that makes use of the VeSFET's two independently-controlled gates to drastically reduce the common-mode gain. An example application of the OTA in a current mirror is also presented.**

***Index Terms*—VeSFET, VeSTIC, OTA, analog circuit, dual-gate device, independent gates.**

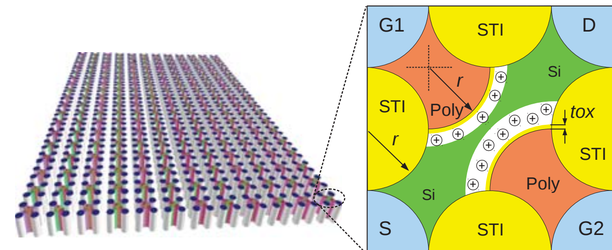

Fig. 1. Left: portion of a VeSTIC layout [2]. White cylinders, passing all through the SOI body layer, are contacts to vertical-channel devices spanned between them. Wiring and isolation between devices (STI) are left out for clarity. Right: top view of a single VeSFET device. The effective geometry of the n-type channel is defined by the depleted regions (white) controlled by two *independent* gates. Parts of the metallic contacts are seen in the corners.

I. Introduction

VeSTIC (Vertical-Slit Transistor-Based Integrated Circuit) is a recently demonstrated technology for low-power VLSI circuits [1]–[3]. The circuits are fabricated with a slightly modified SOI CMOS process sequence. Lithography requirements are greatly relaxed by the total departure from the usual rectangular features in favor of circular ones and by extreme regularity of the layout: all the devices, having the same geometry, are spaced on a square grid (see Fig. 1, left) [2]. Intended as an alternative to CMOS, the technology permits easy integration of various types of device (dual-gate MOSFETs, JFETs, and bipolar transistors) on the same SOI wafer. The staple component of VeSTICs, however, is the novel junctionless Vertical Slit-based Field-Effect Transistor (VeSFET), whose top view is presented in Fig. 1 (right). The key properties of this device include:

1) Operation based on the flow of majority carriers. Thus, the dominant regime is partial depletion of the active region rather than inversion.
2) Two identical, *independently controlled* gates on either side of the active region connecting the source and drain. The central, narrowest part of the active region is referred to as the *slit*.
3) Volume flow of carriers along the slit rather than surface-channel conduction like in the conventional MOSFET or FinFET. The effective cross-section of the slit (and, as a consequence, its conductance) is controlled by the buildup of depleted regions controlled by the voltages of the gates. If the gate voltages are low enough to deplete the *whole* slit to some extent, the device enters the subthreshold region where the drain current is dominated by carrier diffusion.

D. Kasprowicz and B. Swacha are with the Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, Warsaw, Poland, email: D.Kasprowicz@imio.pw.edu.pl

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Those properties have important implications. The use of two separate gates controlling a *common* volume channel is in contrast with other dual-gate transistors having two, only weakly coupled, surface channels like those described in [4]. This makes the VeSFET something more than just two single-gate transistors connected in parallel. Possible advantages include easy implementation of techniques like dynamic control of the threshold voltage or construction of two-input NAND/NOR gates with two, rather than the usual four, transistors (the latter idea, proposed in [5], was verified experimentally in [6]). Furthermore, volume carrier flow mitigates to some extent effects related to silicon-dielectric interface scattering of carriers as well as flicker noise and gate dielectric degradation due to hot-electron injection. Majority-carrier based operation means that the slit is of the same doping type as the source and drain regions. Lack of source- and drain junctions eliminates channel-length variability due to random dopant fluctuation. More about the VeSTIC technology can be found in [2], while an exhaustive description of VeSFET operation, including a compact model, is presented in [5].

The original motivation underlying the VeSTIC technology was to provide an alternative to classic CMOS for low-power VLSI digital applications. Indeed, careful device optimization based on finite-box simulation enabled a nearly ideal subthreshold slope of 65 mV/dec and $I_{on}/I_{off} > 10^8$ [5]. Those parameters, attractive from the digital-circuit standpoint, have been confirmed by prototype measurements [2], [6].

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Nevertheless, any technology aspiring to be a viable alternative for CMOS must also perform well in analog applications. Even predominantly digital systems incorporate analog parts like digital-to-analog or analog-to-digital converters, phase-locked loops for clock recovery, input and output buffers etc. As the cost of through-silicon vias is still high, it is preferable to integrate both analog and digital components of the system on the same die. So far, the VeSFET has been optimized and extensively analyzed numerically only as a component of low-power digital circuits [5], [7]–[9]. It is only recently that small-signal parameters of the VeSFET have been studied and first VeSFET-based analog circuits have been simulated [10].

This article, being an extended version of [10], is organized as follows. Section II reviews the principles of VeSFET operation and compares some of the VeSFET's analog-design related parameters with those of the corresponding MOSFET. Those parameters are presented as a function of the voltages on the two independent gates, which provides suggestions for optimal device biasing in analog circuits. Section III presents an example of a circuit whose operation is enabled by the existence of a device having two independent gates controlling a common channel. The circuit is a variant of two-stage operational transconductance amplifier (OTA) with two common-mode compensation mechanisms working efficiently across nearly the entire input voltage range. This circuit is subsequently compared with a VeSFET-based 'textbook' OTA where the devices' gates are shorted together. Section IV presents the performance of the former OTA (i.e. the one that makes use of independent gates) as a component of a current mirror. Section V summarizes the work.

II. VeSFET's Small-Signal Parameters

The VeSFET transistor is characterized by the following design parameters (see Fig. 1):

- characteristic radius r, shared by all the rounded parts like gates, contacts, and isolation (STI),
- thickness h of the active layer (i.e. silicon layer on top of an SOI wafer where transistors are located),
- thickness t_{ox} of the gate oxide (or another dielectric),
- active-layer doping level N_s,
- gate doping level N_g.

All those parameters, except radius r, are process dependent and, as such, cannot be used as design variables. The value of r must also be kept fixed throughout the wafer to ensure regularity of the VeSFET array, which greatly simplifies the optimization of lithography and etch processes [2]. As a consequence, transistor sizing in the VeSTIC technology can be achieved only by choosing the number of devices connected in parallel. This is in contrast with CMOS, where both the channel length and width can be treated as almost continuous design variables. However, transistor channels used in CMOS analog design are usually tens of times wider than the minimum feature size. This corresponds to a parallel connection of tens of VeSFETs, which seems to provide granularity fine enough for most purposes. If finer tuning is necessary (e.g. for cancellation of systematic offset in an operational amplifier), it can be done by appropriately biasing one of the VeSFET gates, while using the other as a signal input like in a MOSFET.

The VeSFETs considered in this work have a characteristic radius r of $50\,\mathrm{nm}$, gate-oxide thickness t_{ox} of $4\,\mathrm{nm}$, active-region thickness h of $200\,\mathrm{nm}$, and gate doping level N_g of $5\times10^{18}\mathrm{cm}^{-3}$ (opposite type than the active region). Substrate doping depends on the device function, which will be reviewed in the next paragraph. Such geometries and doping levels have been optimized for digital applications [5]. The use of the same device parameters for analog design is supposed to greatly simplify the manufacturing process of mixed-signal circuits.

Two device flavors emerged from studies on the optimization of VeSFET for digital applications. The goal was to create dual-gate devices that mimic the behavior of two single-gate transistors connected in parallel or in series. Those devices are referred to as OR- and AND-VeSFET, respectively. They enabled building dual-input NAND- and NOR gates with two transistors rather than the usual four. The desired type is obtained by differentiating the active-region doping level N_s, while leaving all the other physical parameters identical. The the active-region doping level is $4\times10^{17}\mathrm{cm}^{-3}$ (n-channel) or $5\times10^{17}\mathrm{cm}^{-3}$ (p-channel) in OR devices and $1\times10^{17}\mathrm{cm}^{-3}$ (n-channel) or $1.5\times10^{17}\mathrm{cm}^{-3}$ (p-channel) in AND devices [5]. This difference has profound impact on the device's response to gate voltages V_{G1} and V_{G2}, especially if the two differ substantially. This effect is demonstrated in Fig. 2. Due to lower doping level in the active region, AND devices exhibit greater sensitivity of the depletion depth to gate voltage. Thus, it is sufficient to ground a single gate to deeply deplete the slit, which leads to a cutoff of the drain current. The active region of the OR-type device, on the other hand, is doped so heavily that grounding a single gate depletes only a part of the slit. The drain current, although reduced to some extent, remains substantial. This also explains why AND devices have a greater threshold voltage of around $0.75\,\mathrm{V}$, as opposed to $0.55\,\mathrm{V}$ for the more heavily doped OR devices. The transfer characteristics of both devices, their application in two-transistor logic gates, as well as more in-depth explanation of the underlying physics, can be found in [5]. In loose terms,

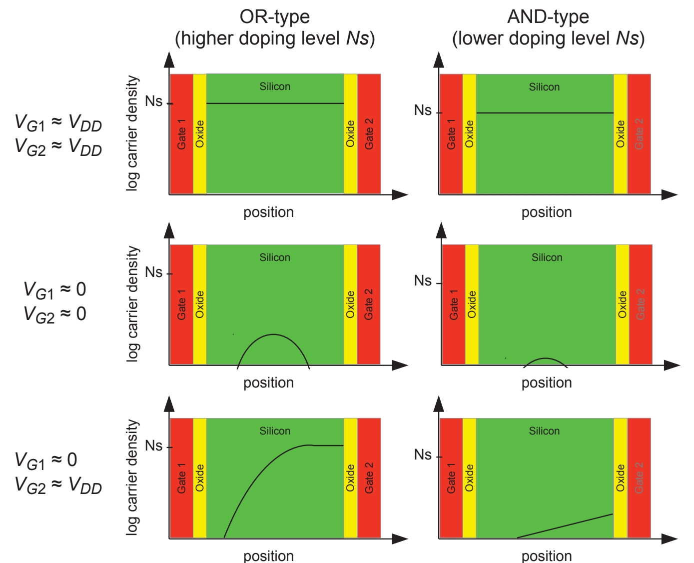

Fig. 2. Carrier distribution across the channel of an OR- and AND-type VeSFET for various biases of Gate1 and Gate2

the behavior of an AND device mimics a series connection of two single-gate devices, while an OR device behaves more like two single-gate transistors connected in parallel.

In the rest of this Section, the AND and OR VeSFETs are compared with an example 90-nm MOSFET. To provide fair comparison, the VeSFET's gates have been be shorted together throughout the experiments. The VeSFET data has been obtained by simulation with Synopsys' Sentaurus Device – a tool using the finite-boxes method for electrical simulation of arbitrary 2D or 3D structures composed of semiconductors, conductors and dielectrics [11]. The MOSFET was simulated with Hspice [12] using the PTM model [13]. The 90-nm process node has been chosen as a CMOS equivalent of the 50-nm-radius VeSFET, because both can be manufactured with litho-etch equipment capable of printing 90-nm-wide lines. The MOSFET width used in the simulation was $200\,\mathrm{nm}$, which corresponds to the thickness h of the active areas of the VeSFETs.

The first parameter of interest is transconductance g_m. The g_m-V_{GS} curves for both kinds of n-type VeSFET are presented in Fig. 3. The peak g_m values of the AND VeSFET are on par with the 90-nm MOSFET. The maximum g_m of the OR VeSFET is twice as great, which results from the higher active-area conductivity due to higher N_s. The main difference between the three devices is the threshold voltage, being the highest for the AND VeSFET and the lowest for the MOSFET.

The differences between the three kinds of transistor are more evident in terms of intrinsic voltage gain defined as the ratio of the device's transconductance to its output conductance: $A_{vi} = g_m/g_{ds}$. This figure is independent of the device width. The plots of A_{vi} versus V_{GS} are presented in Fig. 4. They reach maximum values for high drain voltages for gate voltages around threshold. Of course, A_{vi} grows with increasing V_{DS}, i.e. in deep saturation. As can be seen, the intrinsic gain of the AND device is up to three times as large as that of the equivalent MOS transistor.

Another crucial parameter of a transistor is its transconductance efficiency, defined as the ratio of the transconductance to the drain current [14]. Fig. 5 presents the comparison of g_m/I_D of the two VeSFET types and the same 90-nm MOSFET as before. This metric reflects a device's performance as a low-power amplifying component. The theoretical maximum for the planar MOSFET is $g_m/I_D = q/(kT)$ (where k is the Boltzmann constant and T is the absolute temperature), which is around $38.5\,\mathrm{V}^{-1}$ at room temperature, but in practice only values of $25 - 30\,\mathrm{V}^{-1}$ are obtained. In the VeSFET, the maximum value of transconductance efficiency is $31\,\mathrm{V}^{-1}$ for the OR type and as much as $51\,\mathrm{V}^{-1}$ for the AND type. As in the case of MOSFETs, the maximum values of g_m/I_D are attained in the subthreshold regime. The advantage of the AND type is due to its aforementioned greater sensitivity of the depletion depth (and, as a consequence, drain current) to gate voltage. The lower active-region doping level in AND devices means also greater slit resistance, which translates into lower I_D levels and further boosts the g_m/I_D ratio. Please note that in the case of MOSFETs g_m/I_D curves are usually plotted against the inversion coefficient, which is the drain current normalized w.r.t. some process-dependent constant multiplied by the W/L ratio. This is why such plots are independent of the transistor width. The operation of the VeSFET, on the contrary, is unrelated to inversion, which makes such normalization impossible. Thus, the g_m/I_D curves have been plotted as a function of the drain current of a "unit-size" transistor, which means a single VeSFET and a MOSFET of $W = 200\,\mathrm{nm}$. This is why the *horizontal* position of

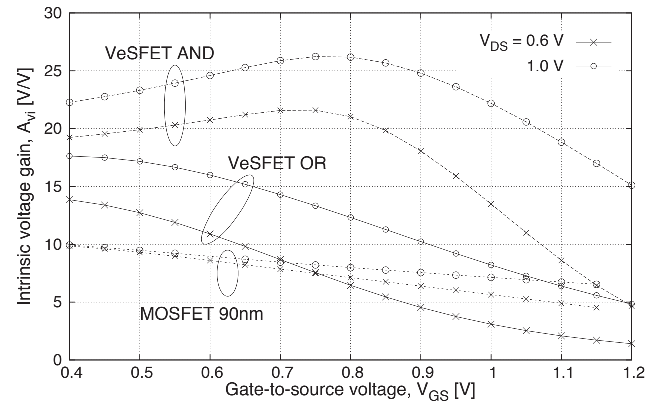

Fig. 4. Intrinsic voltage gain of the VeSFET (dashed – AND-type, solid – OR-type) and 90-nm PTM MOSFET (dotted) as a function of terminal voltages. The VeSFET gates are shorted

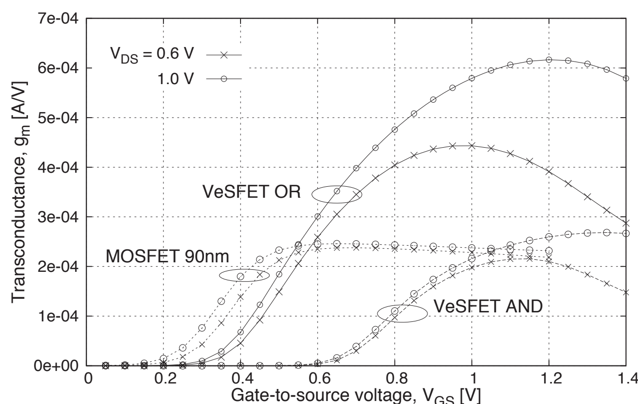

Fig. 3. Transconductance of the 90nm MOSFET (PTM model) and two types of VeSFET. The VeSFET gates are shorted. The MOSFET channel width $W = 200\,\mathrm{nm}$, which equals the active-area thickness of the VeSFETs

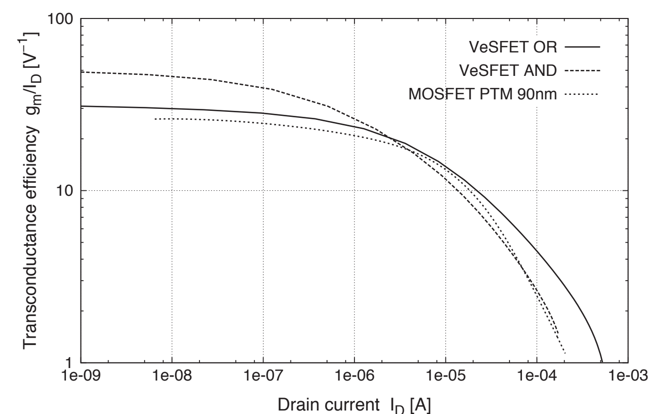

Fig. 5. Transconductance efficiency as a function of the drain current for the 90nm MOSFET (PTM model) and two types of VeSFET (gates shorted). The MOSFET channel width $W = 200\,\mathrm{nm}$, $V_{DS} = 1\,\mathrm{V}$ in all the cases

the MOSFET curve w.r.t. its VeSFET-related counterparts in Fig. 5 is somewhat arbitrary. Nevertheless, it is clear that the maximum g_m/I_D value for the MOSFET is only 26, i.e. half the value for the AND VeSFET. Interestingly, the curve for the OR VeSFET rolls off for larger currents than in the case of the AND device, which makes the two curves cross at approximately $I_D = 2\,\mu$A. This provides the designer with a suggestion to use AND devices if the current per transistor does not exceed single microamps and OR devices otherwise.

The last criterion of comparison between the devices is the intrinsic cut-off frequency f_T as a function of the drain current. The results are shown in Fig. 6. Once again, the superiority of the AND VeSFET manifests itself mostly in the subthreshold region, where its f_T exceeds that of the MOSFET by a decade. For drain currents greater than around $10\,\mu$A, the OR VeSFET is a better choice. Such good result are mostly due to the large thickness of VeSFET gate oxide. At $4\,$nm it is much greater than in the corresponding MOSFET, leading to a smaller gate capacitance. The roll-off of the f_T curves observed for high values I_D results from a g_m drop for strong V_{GS} and V_{DS}, caused mostly by carrier velocity saturation.

The values of the aforementioned parameters suggest that the VeSFET is superior to the MOSFET of the corresponding process node. The greatest advantage of the VeSFET, however, is the presence of two independent gates controlling a common channel. Fig. 7a presents lines corresponding to constant values of drain current in the space spanned by the voltages of the two gates.

If the threshold voltage is defined as the gate voltage corresponding to some predefined value of drain current, this plot can be interpreted as representing the threshold voltage of one gate as a function of the potential of the other gate. As can be seen, this dependence is very strong, especially for high gate voltages. Indeed, it is much stronger than that for dual-gate planar SOI devices presented in [4] (see Fig.7b). Additionally, the relationship is symmetrical. This creates interesting possibilities for design of analog circuits like the one presented in the following Section.

Small-signal parameters are of course also functions of the voltages on both gates. Transconductance and intrinsic voltage

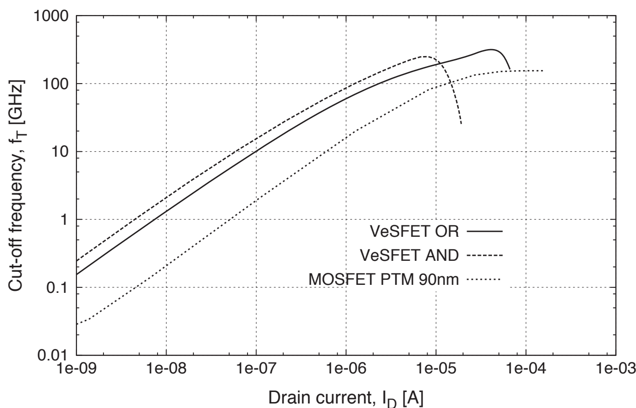

Fig. 6. Intrinsic cut-off frequency as a function of the drain current for the 90nm MOSFET (PTM model) and two types of VeSFET. $W = 200\,$nm in all the devices.

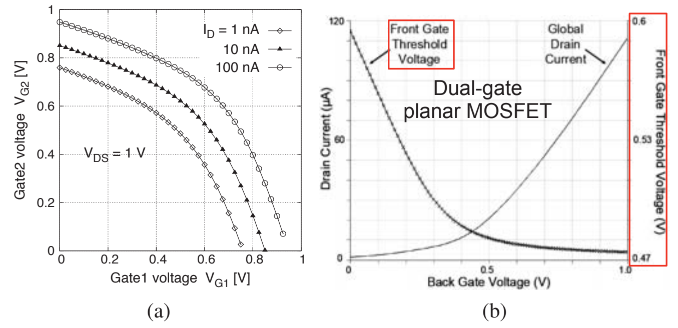

Fig. 7. Lines corresponding to constant values of the AND-VeSFET drain current as a function of gate voltages V_{G1} and V_{G2} (a). This plot can also be interpreted as the threshold voltage of G_2 as a function of V_{G1}. A similar plot for a dual-gate planar MOSFET (source: [4]) shows much weaker threshold-voltage control (b)

gain for a single gate (Gate1 in this case) can be defined as

$$g_{m1} = \partial I_D / \partial V_{G1} \tag{1}$$

and

$$A_{vi1} = g_{m1}/g_{ds}, \tag{2}$$

respectively. The values of g_{m1} and A_{vi1} are plotted in Fig. 8 and Fig. 9, respectively, in the space spanned by the voltages on the two gates. Fig. 9 clearly suggests that the maximum intrinsic gain is achieved by applying relatively high voltages (around 1 V) on the driven gate, while keeping the other one grounded or even biasing it with a negative voltage. This effect is easy to explain based on the carrier distribution across the slit. The key to achieving high values of g_{m1} and A_{vi1} is to maximize the influence of Gate1 on the overall number of carriers in the slit. This is why it is desirable to bias

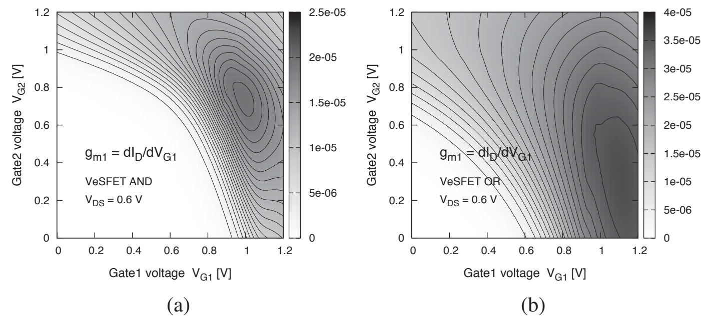

Fig. 8. Transconductance of Gate1 as a function of voltages on both gates for the AND VeSFET (a) and OR VeSFET (b)

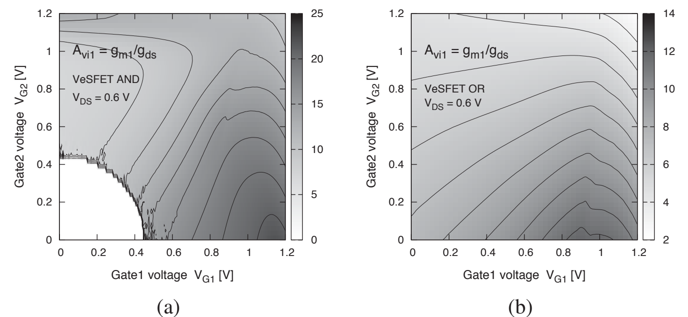

Fig. 9. Intrinsic voltage gain A_{vi} of signal applied to Gate1 as a function of voltages on both gates for the AND VeSFET (a) and OR VeSFET (b). The extremely noisy data corresponding to the lowest gate voltages for the AND VeSFET have been left out for clarity

Gate1 near the flatband voltage (which is about 0.9 V for the AND-VeSFET and 0.95 V for the OR-VeSFET) or even in weak accumulation. The control of Gate1 over carrier density may extend relatively deep into the slit, but only if Gate2 is biased in depletion. Otherwise the slit becomes "flooded" with carriers controlled by Gate2, leaving little control to Gate1. In the case of AND-VeSFET, however, the influence of either gate on the entire slit is so strong that biasing Gate2 too low may cause its respective depletion region to penetrate as far as under Gate1. This explains why g_{m1} assumes the maximum at $V_{G2} \approx 0.75$ V, which is a relatively high value.

III. VeSFET-Based OTA

Unless otherwise noted, the following assumptions apply throughout the rest of this work. The circuits are built exclusively from AND VeSFETs, as they provide the highest intrinsic voltage gain. If parallel connection of several VeSFETs is required in some portions of the circuit, this fact is denoted in diagrams by an appropriate multiplier, e.g. "x10". All the circuits are powered with asymmetric supply voltage $V_{dd} = 1.2\,\mathrm{V}$. All the voltages are defined w.r.t. the ground. Small-signal parameters like differential gain A_d, common-mode gain A_c, and common-mode rejection ratio CMRR are all determined for the "neutral" common-mode input voltage $V_c = V_{dd}/2$.

Even though compact models exist for VeSFET drain current [5] and capacitances [15], their accuracy is the highest either for gate voltages above the threshold voltage or in deep subthreshold operation. The transition between those regions is modelled using smoothing functions, which adversely affects the accuracy. As the devices used in the circuits described below are usually biased near the threshold, the accuracy of the models was found inadequate. Therefore, all the circuit simulations in this work have been performed with Synopsys' Sentaurus Device, which guarantees high accuracy. The price to pay, however, is the inability of obtaining the frequency response of the simulated circuits. Therefore, this work is limited to DC characterization.

The circuit diagram of the OTA investigated in this work is presented in Fig. 10 (a). The diagram of the block denoted there as CMCB (common-mode compensation block) can be found in Fig. 10 (b). The differential pair $M_1 - M_2$ of the input stage of the OTA is a *differential current mirror* proposed in [4]. (The latter circuit has been originally presented for planar double gate MOSFETs with independently driven gates. The function of the differential current mirror within the amplifier proposed in the cited work, however, was different than presented here.) The most striking difference between the resulting two-tier architecture and a "conventional", three-tier differential amplifier is the lack of the "tail" current source. That current source, being in the simplest case a single transistor M_{CS}, provides the necessary common-mode attenuation in the conventional architecture. However, it limits the input voltage range. Indeed, the minimum acceptable voltage on either input is

$$V_{in\,min} = V_{TH\,M1} + V_{sat\,M1} + V_{sat\,M_{CS}}, \tag{3}$$

where V_{sat} denotes the saturation voltage of a device while V_{TH} – its threshold voltage. $V_{in\,min}$ can be minimized by reducing either $V_{sat\,M1}$ or $V_{sat\,M_{CS}}$. This, however, can only be done by increasing the width of either of these transistors (or, in the case of VeSFETs, connecting several devices in parallel). As V_{sat} is inversely proportional to the square root of the transistor width, this dramatically increases the silicon area occupied by the circuit. Of course, M_5 cannot be simply removed from the conventional differential amplifier because this would lead to a dramatic increase in the unwanted common-mode gain A_c. The use of dual-gate transistors, however, provides additional feedback paths that can be used to largely reduce A_c. One such feedback is introduced by the short between the drain of M_1 and one of its gates. Any change in the drain potential is fed back to the gates of M_1 and M_2, thus counteracting the original shift in the drain potential and limiting the common-mode gain. Unfortunately, this mechanism also reduces the differential gain. However, this feedback loop is necessary to reduce the output swing due to common-mode input signal, which enables efficient operation of the common-mode compensation block CMCB (described below) across the entire range of input voltages.

The transfer characteristics of the input stage are shown in Fig. 11. The values of small-signal differential gain A_d and common-mode gain A_c in this structure are $5.1\,\mathrm{V/V}$ and $-0.32\,\mathrm{V/V}$, respectively, which translates into a CMRR of $24\,\mathrm{dB}$. This figure is subsequently improved by the CMCB, which is another example of circuit made possible by independent-gate transistors. It is a simple dual-input circuit with a negligible gain for the differential signal and a common-

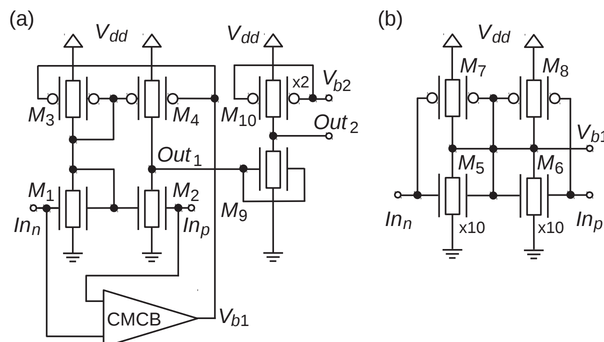

Fig. 10. Two-stage VeSFET-based OTA (a) and the circuit diagram of the common-mode compensation block CMCB (b)

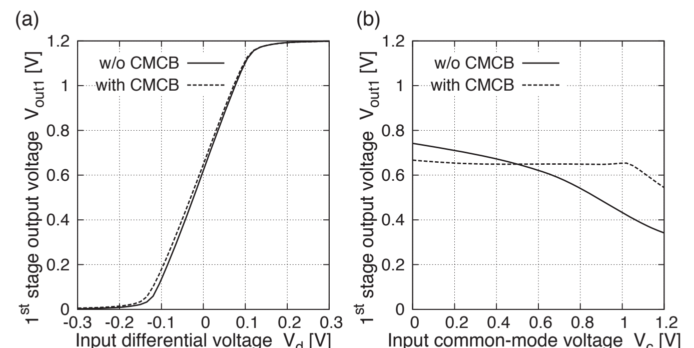

Fig. 11. Transfer curves of the input stage with and without the CMCB

mode gain of about -1 V/V across almost the entire range of input voltages (Fig. 12). The inputs of the CMCB are connected in parallel with those of the OTA's input stage, while the output signal V_{b1} is fed back to the gates of M_3 and M_4. The ratio between the n- and p-channel VeSFETs in the CMCB has been chosen so as to minimize the overall common-mode gain of the entire OTA. As shown in Fig. 11 (a), the impact of the CMCB on the OTA's differential gain is negligible. The transfer curves of the complete two-stage OTA with CMCB are presented in Fig. 13. The values of differential- and common-mode gain of this two-stage amplifier are -54 V/V and -29.6 mV/V, respectively, resulting in a CMRR of 65.2 dB. Thus, the CMCB boosted the CMRR by as much as 41 dB. As can be seen in Fig. 13 (b), this compensation is efficient for common input voltages ranging from around 0.35 V to 0.9 V. The systematic input offset of the entire two-stage OTA is $V_{offset} = 1.28$ mV. The value of $V_{b2} = 0.616$ V reduces the systematic input offset to single microvolts. However, the choice of $V_{b2} = V_{dd}/2$ is more convenient because this value can be obtained with a simple voltage divider. Please note that a voltage divider build with diode-connected VeSFET transistors delivers a more accurate voltage ratio than its bulk-MOSFET counterpart because of lack of body effect.

Even though the amplifier (including the CMCB) has been optimized for $V_{dd} = 1.2$ V, it performs well for supply voltages down to 0.6 V, as summarized in Table I. The acceptable range of common-mode input voltage actually expands as the supply voltage decreases. As indicated in Fig. 14, for $V_{dd} = 0.6$ V the amplifier remains nearly insensitive to common-mode input voltage ranging from zero to $90\,\%$ of V_{dd}. Unfortunately,

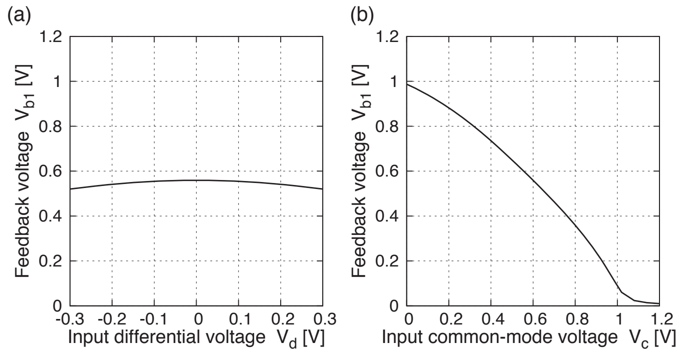

Fig. 12. Transfer curves of the CMCB

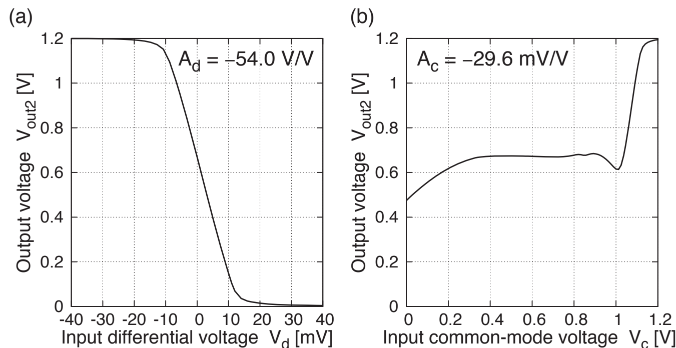

Fig. 13. Transfer curves of the complete OTA with the CMCB. A_d and A_c denote differential and common-mode gain, respectively

TABLE I
SUPPLY-VOLTAGE DEPENDENCE OF SELECTED PARAMETERS OF THE OTA

V_{dd} [V]	A_d [V/V]	A_c [mV/V]	CMRR [dB]	Voffset [mV]
0.6	32.8	20.8	64.0	3.10
0.8	37.5	10.3	71.2	2.70
1.0	44.0	38.6	61.1	2.17
1.2	54.0	29.6	65.2	1.28
1.4	69.2	46.0	63.5	–0.33

as in any other OTA, the offset voltage is optimized for one particular value of V_{dd} and cannot remain unaffected by its change. The fact that M_{10} in the output stage has two gates may provide an additional feedback input for offset cancellation.

To further confirm the benefits coming from independent-gate operation, the OTA examined above has been compared with a "traditional" OTA architecture presented in Fig. 15. To ensure an appropriate level of common-mode attenuation, as many as 30 VeSFETs had to be used to form the common current source M_{CS} for the differential pair. This drives the total number of transistors to 47, which is much larger than the 29 devices used in the previous design. What is more, the presence of M_{CS}, combined with the relatively high threshold voltage of AND VeSFET, drives the minimum acceptable input voltage to levels above $V_{dd}/2 = 0.6$ V. This effect had to be offset with input-voltage level shifters M_5–M_8. The transfer curves of the resulting circuit are presented in Fig. 16.

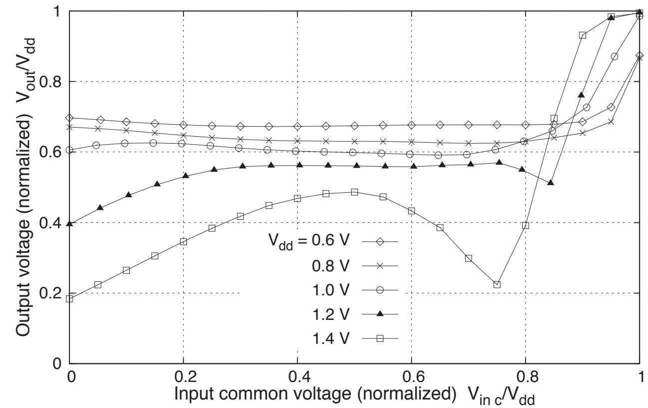

Fig. 14. Common-mode transfer curves of the OTA for various values of supply voltage V_{dd}

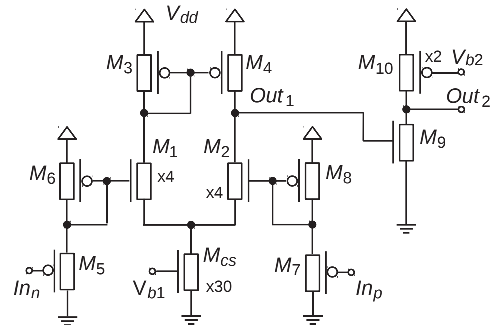

Fig. 15. "Conventional" OTA built with VeSFETs. As each device has its gates shorted, only a single gate per transistor is drawn for clarity. $V_{b1} = 0.6$ V, $V_{b2} = 0.7$ V

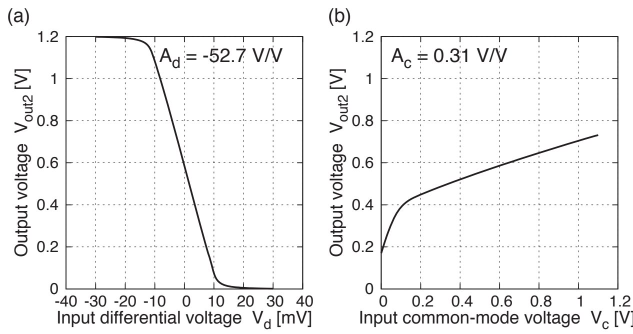

Fig. 16. Transfer curves of the "conventional" OTA shown in Fig. 15. A_d and A_c denote differential and common-mode gain, respectively

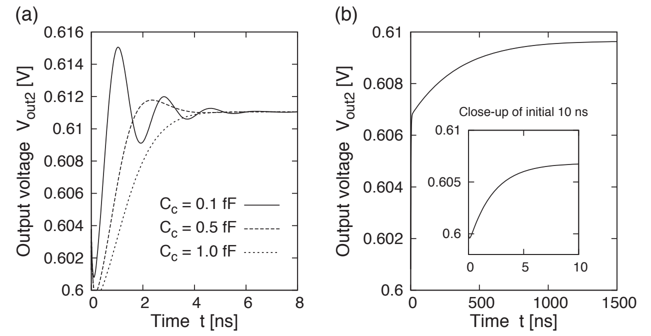

Fig. 17. Step responses of the proposed OTAs: using independent gates (a) and "conventional" (b), both in the voltage follower configuration i.e. with the inverting input connected to Out_2. The input stimulus is a 2-ps step from $0.6\,\mathrm{V}$ to $0.61\,\mathrm{V}$. C_c is the value of compensation capacitor (found unnecessary in the "conventional" OTA). Note the time-scale difference between the plots

Table II summarizes crucial parameters of this design compared with those for the independent-gate architecture. The differential voltage gain is $-52.7\,\mathrm{V/V}$, i.e. around the same as previously obtained. However, even with a very large M_{CS} in place, the common-mode input signal is not sufficiently attenuated. This leads to a CMRR of only 44.6 dB, i.e. over 20 dB worse than in the independent-gate architecture. The only way to improve CMRR in this architecture is to make M_{CS} even wider and bias it with a lower gate voltage V_{b1} to drive it deeper into saturation. This, however, would lead to further expansion of the circuit size. Additionally, the independent-gate architecture is less sensitive to supply-voltage changes, achieving a PSRR that is 9 dB greater than that of the conventional OTA.

Finally, the two architectures have been compared with respect to speed. As mentioned before, the frequency-domain analysis in Sentaurus Device cannot determine the transmittance of circuits composed of several devices. Thus, time-domain simulations have been performed. Each OTA has been configured as a voltage follower by shorting its inverting input with the output. The non-inverting input was stimulated with a voltage step from $0.6\,\mathrm{V}$ to $0.61\,\mathrm{V}$. The OTA using independent gates needed a compensation capacitor between Out_1 and Out_2 to dampen oscillations – see Fig. 17 (a). However, the required capacitance C_c turned out to be less than $1\,\mathrm{fF}$. This is only several times the average gate capacitance of a single VeSFET (see [15] for exact values), which means C_c can be realized with only a modest increase in the circuit size. With proper compensation, the output voltage settles within $5\,\mathrm{ns}$. By way of comparison, the "conventional" OTA did not require any compensation, as evidenced in Fig. 17 (b). The output voltage, however, after taking about $10\,\mathrm{ns}$ to reach $70\,\%$ of the step height, started creeping towards its final value at about $1\,\%$ of its initial speed. This behavior is observed for both positive and negative input steps of various magnitudes. This is another argument in favor of the independent-gate architecture.

TABLE II
COMPARISON OF THE TWO OTA ARCHITECTURES: "CONVENTIONAL" (FIG. 15) AND USING INDEPENDENT GATES (FIG. 10)

Parameter	Conventional	Indep. gates
A_d [V/V]	52.7	54.0
A_c [mV/V]	310	29.6
CMRR [dB]	44.6	65.2
PSRR (DC) [dB]	37	46
Voffset [mV]	-0.26	1.28
Num. devices	47	29

IV. EXAMPLE APPLICATION OF THE OTA

An example application of the independent-gate VeSFET OTA is a high-precision current mirror presented in Fig. 18. The OTA forces the drain voltage of M_{m1} to a value very close to that of M_{m2}. Unlike in a simple two-transistor current mirror, the drain voltages of M_{m1} and M_{m2} are kept equal by inserting the mirror in the feedback loop of the OTA. With identical gate-source and drain-source voltages, the drain currents of those two transistors are the same, even for output voltages well below the saturation voltage of M_{m2}. Assuming perfect matching of M_{m1} and M_{m2}, the only source of copying error is the amplifier offset. This is why the offset should be minimized for an arbitrary value of common-mode voltage. Fig. 19 (a) shows current-copying error as a function of the output voltage for various values of the reference current, while Fig. 19 (b) presents the corresponding output resistance.

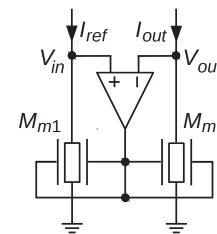

Fig. 18. Current mirror with an OTA in the feedback loop

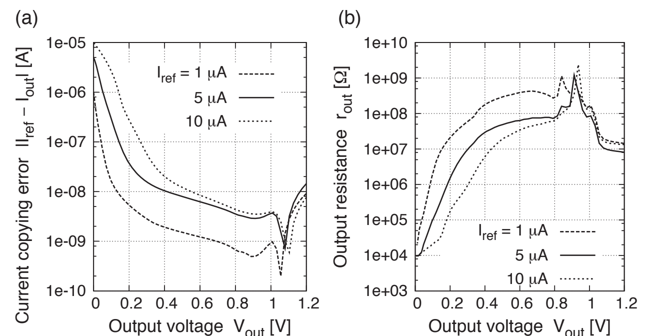

Fig. 19. Current mirror with the VeSFET-based OTA in the feedback loop: current copying error (a) and output resistance (b) for various values of the reference current

The copying error increases substantially only in situations where high output current is expected in spite of a low output voltage. This requires driving the transistors' gates to increasingly high voltages, which is limited by the saturation of the OTA's output at the V_{dd} level. For a typical situation of $V_{out} = 0.6\,V$ such saturation takes place if the reference current exceeds about $13\,\mu$A. For lower current levels (or larger output voltages) the source preserves good linearity, with relative errors of current copying less than $0.2\,\%$, as shown in Fig. 20. If higher currents or better parameters are expected, several parallel-connected VeSFETs must be used in place of M_{m1} and M_{m2}.

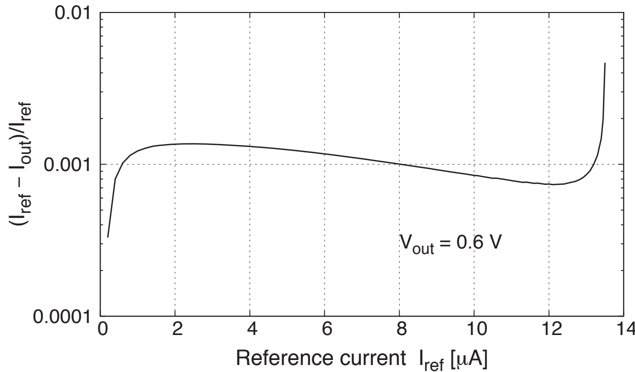

Fig. 20. Relative current-copying error of the OTA-based current mirror for a range of reference currents

V. Conclusions and Future Work

As shown in the previous sections, the VeSFET has promising properties as a component of analog circuits. The biasing conditions maximizing the transconductance and intrinsic voltage gain have been identified and explained based on the device's physics. The VeSFET has been shown to be superior to the equivalent-generation MOSFET in terms of transconductance, transconductance efficiency, intrinsic voltage gain, and cut-off frequency. The VeSFET's most important property, two independent gates controlling a common channel, enables introduction of strong feedback even in very simple circuits. As an example, two VeSFET-based OTA architectures have been compared. While their differential gain was identical, the one taking advantage of the VeSFET's two independent gates has been demonstrated to outperform the "conventional" Miller architecture in terms of CMRR and speed. Studies of the stability of VeSFET-based OTAs are under way.

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Dominik Kasprowicz received his M.Sc. and Ph.D. degrees in Electrical Engineering (both with honors) from the Warsaw University of Technology (WUT) in 2001 and 2006, respectively. He has been an Assistant Professor in the Institute of Microelectronics and Optoelectronics of WUT since 2007. His fields of scientific interest include automated optimization of analog circuits and dual-gate transistor modeling. He has published about 20 scientific papers.

Bartosz Swacha received his B.Sc. degree in Electrical Engineering from the Warsaw University of Technology (WUT) in 2012. He is pursuing his M.Sc. degree at WUT. He is currently working on sensors for medical applications.