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Three phase active power filter with selective harmonics elimination

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Abstract: This paper describes a three phase shunt active power filter with selective harmonics elimination. The control algorithm is based on a digital filter bank. The moving Discrete Fourier Transformation is used as an analysis filter bank. The correctness of the algorithm has been verified by simulation and experimental research. The paper includes exemplary results of current waveforms and their spectra from a three phase active power filter.

Key words: active power filter, discrete fourier transform, harmonic distortion, power system harmonics

1. Introduction

Nowadays devices based on power electronics are major components commonly found connected to power lines. Such devices as saturated transformers, arc furnaces and semiconductor switches, and so on, draw non-sinusoidal current from the power line. As a result the increasing number of power electronics devices with more and more nonlinear loads connected to power lines makes the problem of harmonic compensation of power line current increasingly important. Therefore a typical power distribution system has to deal with harmonics and reactive power support. To suppress power line harmonics, an active power harmonic compensator can be used, which is also called an active power filter (APF).

The APF can be connected in series or in parallel with the power line. The parallel compensator (also called: a shunt APF and a current-fed APF) permits compensation of the harmonics, reactive power and asymmetries of the line currents caused by nonlinear loads.

In the proposed solution the user can select which harmonics are the most crucial in the active power filtration process. This is very important, especially when several APFs are working in parallel or cascaded connection. Another application for such a filter is as a power line harmonics resonance dumper.

The most commonly used filters in APF control circuits are such as: Discrete Fourier Transformation (DFT), recursive DFT, synchronous individual harmonic *d-q* frame, ordinary

band-pass IIR filters, repetitive control etc., in [1-3, 5-17, 18-20]. Proposed in the paper is an alternative control circuit with filter bank in [11-14].

2. Active power filter

A simplified diagram of a three phase compensation circuit with shunt APF without feedback is shown in Figure 1. The APF has unity gain and was chosen because of its assured stability in use. The shunt APF injects AC power current $i_C(t)$ to cancel out power line AC harmonics content. The resulting line current $i_M(t)$ is the difference between the load current $i_L(t)$ and the compensating current $i_C(t)$

$$i_M(t) = i_L(t) - i_C(t). \tag{1}$$

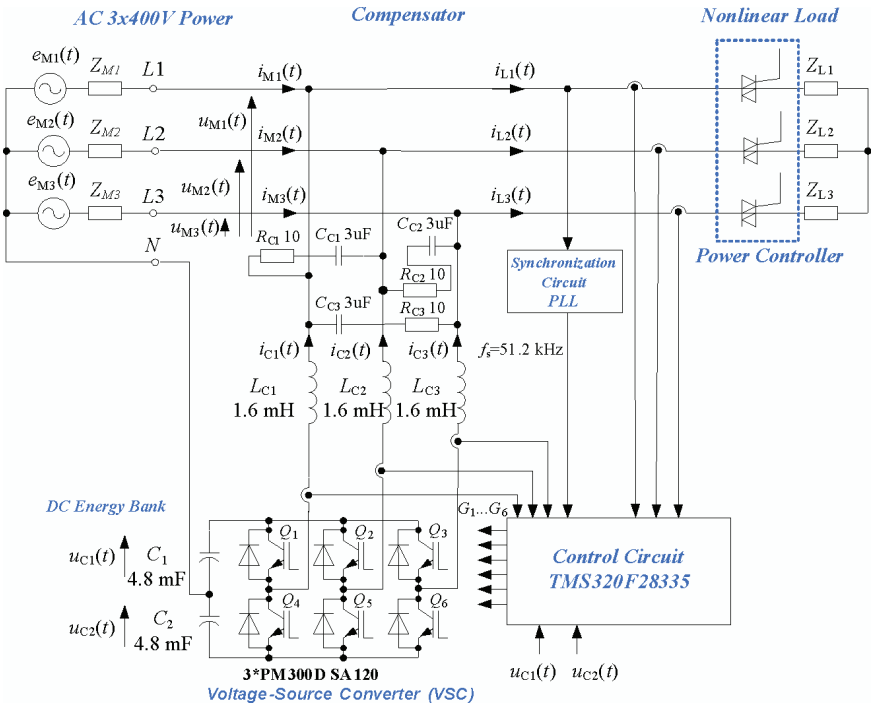

Fig. 1. Three phase active power filter compensation circuit

In the case of full compensation of reactive power and harmonics, the compensation current can be determined by

$$i_C(t) = i_L(t) - I_{H1}\sin(2\pi f_M t + \varphi_{H1}), \tag{2}$$

where: I_{H1} – amplitude of first harmonic, f_M – frequency of first harmonic, φ_{H1} – phase angle of first harmonic.

However, in the case of elimination of selective harmonics in the line current, the value of the compensation current is the sum of selected harmonics, which can be determined by the equation

$$i_C(t) = \sum_{k=2}^{N} I_k \sin(2\pi k f_M t + \varphi_k), \tag{3}$$

where: I_k – amplitude of k^{th} harmonic, kf_M – frequency of k^{th} harmonic, φ_k – phase angle of k^{th} harmonic.

3. The filter banks

The general form of the N-channel filter banks is shown in Figure 2, where N is the number of subbands. Problems related to the design of the filter banks are widely described, for example in [4, 18, 14]. Analysis filter banks decompose signal spectra into a N of directly adjacent frequency bands and recombine the signal spectra by means of synthesis filter banks. The output signal of filter banks $Y(z)$ can be calculated by the equation

$$Y(z) = X(z)\sum_{k=0}^{N-1} H_k(z)G_k(z). \tag{4}$$

It is possible to simplify this equation to

$$Y(z) = F(z)X(z), \tag{5}$$

where $F(z)$ denotes the quality of signal reconstruction. The typical frequency responses of N-channel uniform band analysis and synthesis filter banks are shown in Figure 3.

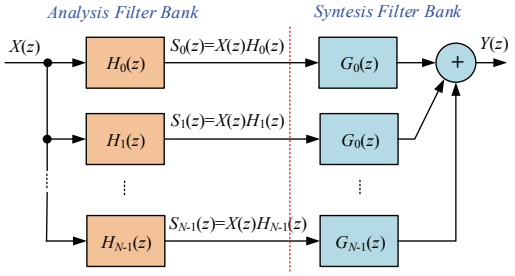

Fig. 2. An N-channel uniform band analysis and synthesis filter bank

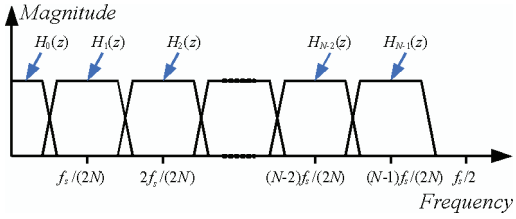

Fig. 3. A typical frequency response of N-channel uniform band analysis and synthesis filter banks

4. The control algorithm

A block diagram of a digital control circuit for a three phase APF is depicted in Figure 4. The control circuit is shown for one phase. In the block diagram, the voltage controller for the capacitors C_1 and C_2 (Fig. 1) is omitted for simplicity. Analog signals are converted to digital form by 16-bit A/D converters with simultaneous sampling. The circuit uses a coherent sampling frequency of f_s = 51.2 kHz, generated by a phase-lock loop circuit (PLL) synchronized with the power network voltage $u_{M1}(t)$.

As the current controller, a digital version of a hysteresis controller is used. The advantage of the controller is its simplicity and excellent dynamic properties. The output inverter consists of an LCR filter for suppressing modulation components. The author is aware that the use of the LCL filter would be much better, but at the time of the research the author had at his disposal only an APF with an LCR filter. In the future it is planned to modify the APF output circuit in order to apply an LCL filter.

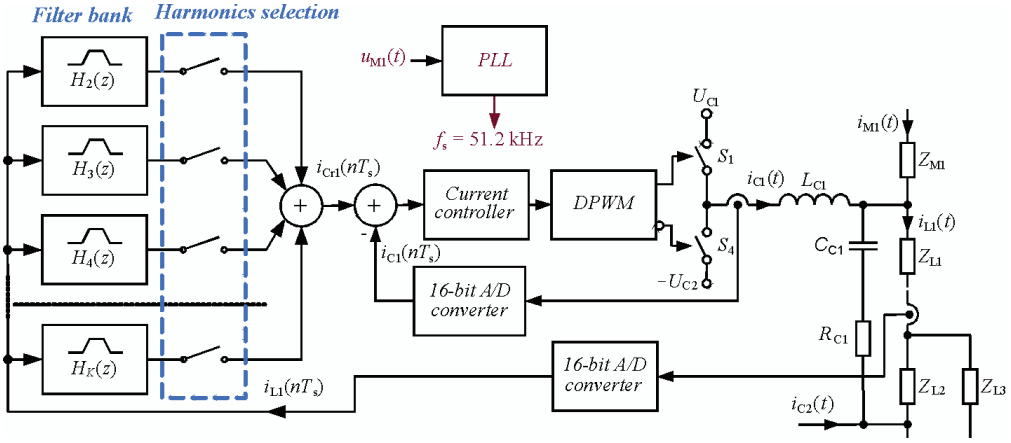

Fig. 4. Simplified block diagram of control circuit for harmonics compensator

The digital analysis filter bank is used for harmonics detection [11-13]. A simple summing block is used in the control circuit as a synthesis filter bank. The analysis filter bank is based on a Fourier series, also called moving DFT (MDFT) [8].

The distorted load current can be approximated by

$$\begin{aligned} i(n) &= I_0 + \sum_{k=1}^{N} I_k(n)\sin(2\pi kn/N + \varphi_k(n)) = \\ &= I_0 + \sum_{k=1}^{N} \left(A_k \cos(2\pi kn/N) + B_k \sin(2\pi kn/N)\right), \end{aligned} \tag{6}$$

where: I_k – amplitude of k-th harmonic.

The value of time varying coefficient $A_k(n)$ and $B_k(n)$ can be calculated by

$$\begin{cases} A_k(n) = \dfrac{2}{N} \displaystyle\sum_{m=n-N+1}^{n} (i(m)\sin(2\pi k m/N)) \\ B_k(n) = \dfrac{2}{N} \displaystyle\sum_{m=n-N+1}^{n} (i(m)\cos(2\pi k m/N)) \end{cases} \tag{7}$$

and in the recursive form

$$\begin{cases} A_k(n) = A_k(n-1) + \dfrac{2}{N}(i(n) - i(n-N))\sin(2\pi k n/N) \\ B_k(n) = B_k(n-1) + \dfrac{2}{N}(i(n) - i(n-N))\cos(2\pi k n/N). \end{cases} \tag{8}$$

Finally the *k*-th component is determined by

$$i_k(n) = A_k(n)\sin(2\pi k n/N) + B_k(n)\cos(2\pi k n/N). \tag{9}$$

A block diagram of a MDFT analysis filter bank for one component is depicted in Figure 5.

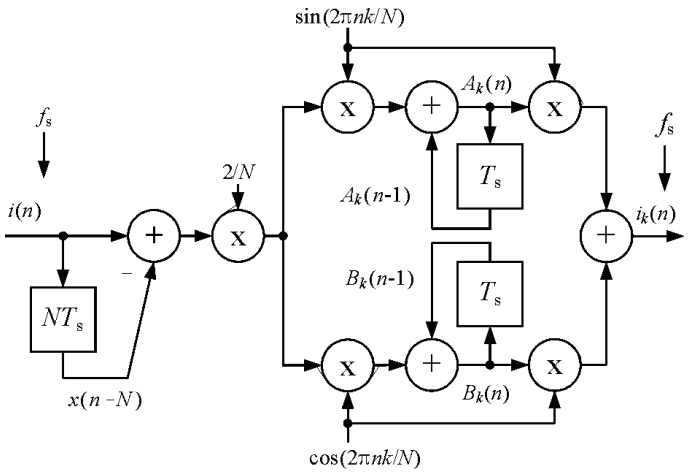

Fig. 5. Block diagram of MDFT filter

A frequency response of such a filter for $k = 1$, $N = 256$ and $f_s = 50 \cdot N = 12.8$ kHz is shown in Figure 6. In this case for a frequency of 50 Hz, the gain is equal to 1, and the phase shift is equal to 0 (Fig. 6).

As with all filter banks based on the DFT algorithm, the circuit does not have very good filtration properties and it is better suited for harmonic filtering in systems with coherent sampling. Therefore phase-locked loop circuit (PLL) should be used.

A block diagram of a simplified circuit for 5th harmonic compensation is depicted in Figure 7. In the circuit the MDFT filter from Figure 5 is used as a 5th harmonic detector. The simulation parameters are: $k = 5$, $N = 256$, $f_s = 50 \cdot N = 12800$ Hz.

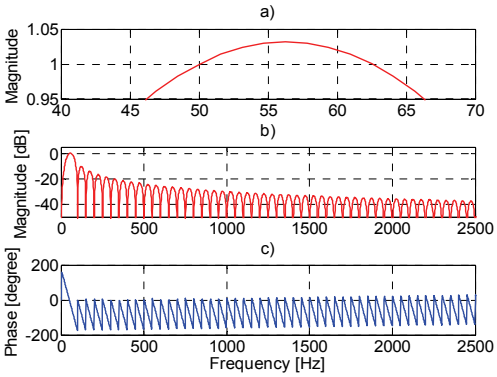

Fig. 6. Frequency response of MDFT filter for $k = 1$ (50 Hz): a) magnitude – pass-band, b) magnitude, c) phase

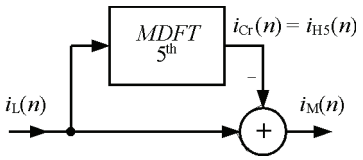

Fig. 7. Block diagram of simplified circuit for 5th harmonic compensation

Simulation studies have been performed on the presented circuit. The circuit input signal $i_L(n)$ is a sinusoidal signal with a unitary amplitude and frequency of 50 Hz. To this signal the 5th harmonic (a sinusoidal signal with 0.35 amplitude and frequency 250 Hz) is added for a time equal to three periods of the first harmonic. The results of such a simulation are shown in Figure 8, where there are presented waveforms of currents: $i_L(t)$, $i_C(t)$, $i_M(t)$. The analysis of line current waveform $i_M(t)$ shows that the response time for such a circuit is equal to 20 ms (one period of line voltage).

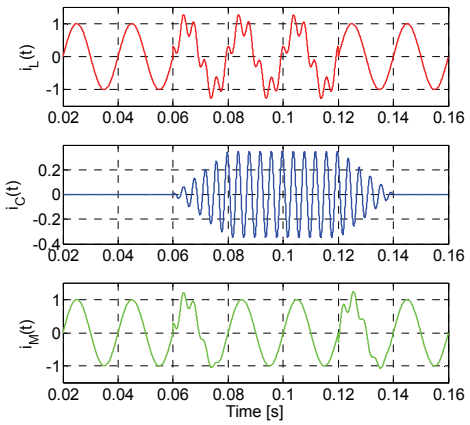

Fig. 8. Waveforms of simplified compensation circuit in transition state

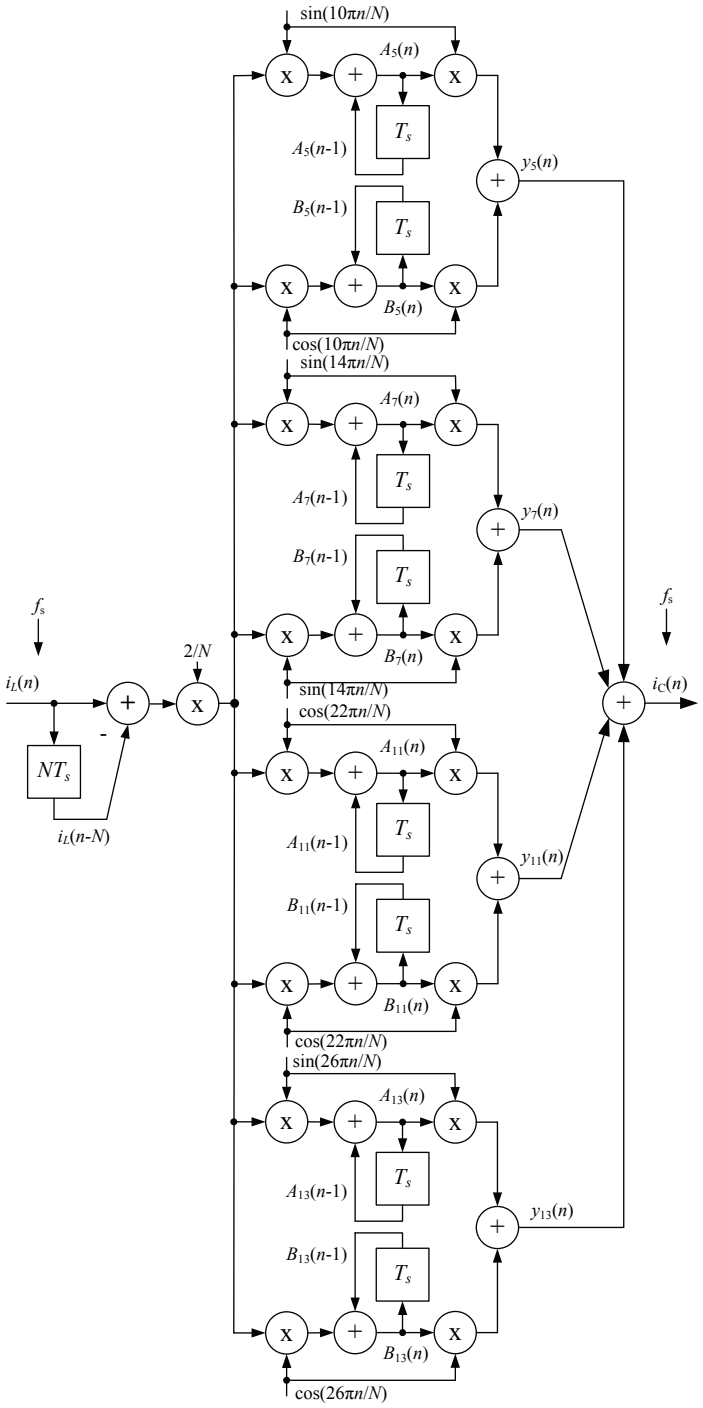

Fig. 9. Block diagram of four channel MDFT filter bank for $k = \{5; 7; 11; 13\}$ harmonics

5. Simulation of compensation circuit

Using the MDFT filter shown in Figure 5 it is possible to build an analysis filter bank for selected components. A block diagram of a four channel MDFT analysis filter bank for $k = \{5; 7; 11; 13\}$ harmonics is depicted in Figure 9. An analysis filter bank consists of a common comb filter on the input and the four branches. The frequency response of such a circuit is depicted in Figure 10. Simulation studies on the control system shown in Figure 4 have been carried out for a three phase APF compensation circuit. The simulation circuit block diagram is shown in Figure 11, in which the circuit output inverter was simulated by voltage controlled current sources. The simulation results of such a compensation circuit (Fig. 11) for orthogonal load currents are shown in Figure 12, which presents waveform currents and their amplitude spectra. Compensation of the selected harmonics has occurred, as predicted.

In order to further validate the operation of the compensation circuit, additional simulation studies on a thyristor power controller with resistive loads were also carried out. The results of such simulation are depicted in Figure 13. Measured values of currents $i_L(t)$, $i_C(t)$, $i_M(t)$ for selected harmonics are shown in Table 1. Based on the simulation results it can be concluded that the compensation of selected harmonics is successful.

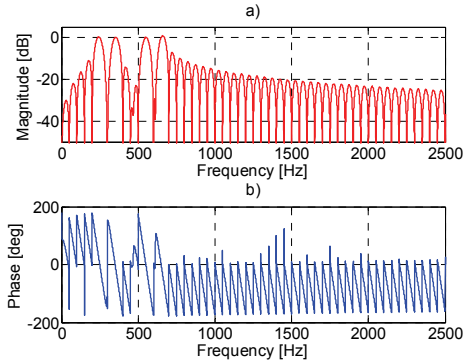

Fig. 10. Frequency response of four channel MDFT filter bank for $k = \{5; 7; 11; 13\}$ harmonics

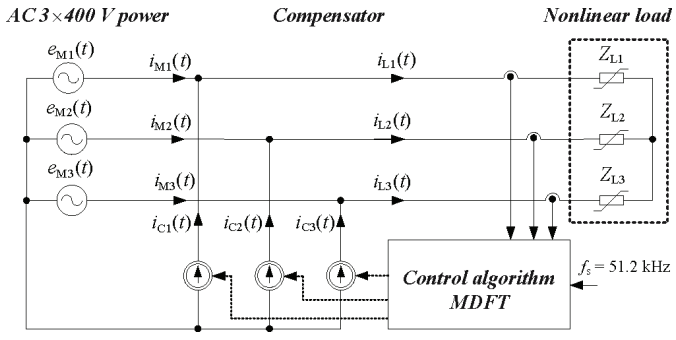

Fig. 11. Block diagram of simulation circuit of APF compensation circuit with MDFT selective harmonics compensation for $k = \{5; 7; 11; 13\}$

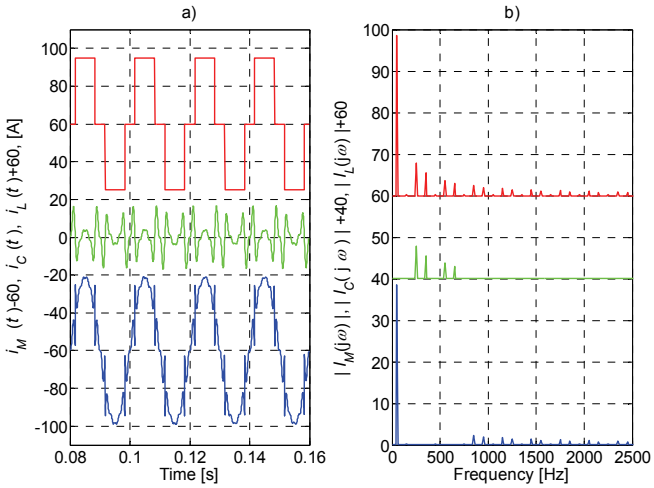

Fig. 12. Simulation results of APF with MDFT selective harmonics compensation for k = {5; 7; 11; 13}, for orthogonal load currents: a) waveforms, b) spectra

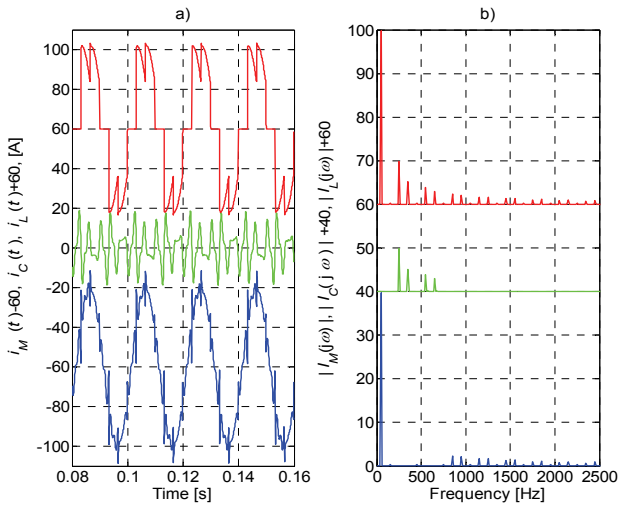

Fig. 13. Simulation results of APF with MDFT selective harmonics compensation for k = {5; 7; 11; 13}, for power controller with resistive loads: a) waveforms, b) spectra

Table 1. Value of currents $i_L(t)$, $i_C(t)$ and $i_M(t)$ for selected harmonics

f [Hz]	50	**250**	**350**	**550**	**650**	850	950
$\|I_L(j\omega)\|$ [A]	39.72	9.81	5.16	3.85	3.01	3.35	2.14
$\|I_C(j\omega)\|$ [A]	0	9.81	5.16	3.85	3.01	0	0
$\|I_M(j\omega)\|$ [A]	39.72	0	0	0	0	2.35	2.14

6. Experimental test results

In order to fully verify the proposed selective harmonic elimination algorithm, experimental studies were carried out too. For this purpose, the compensation circuit shown in Figure 1 and 4 is used. The system parameters are shown in Table 2.

Table 2. Value of experimental circuit parameters

Parameter	L_C	R_L	C_C	R_C	C_1, C_2	f_s
Value	1.6 mH	7 Ω	3 µF	10 Ω	2.8 mF	51.2 kHz

The experimental results of such a compensation circuit (Fig. 1) are shown in Figure 14, which presents waveform and their amplitude spectra of currents $i_L(t)$, $i_C(t)$ and $i_M(t)$. Measured values of currents $i_L(t)$, $i_C(t)$, $i_M(t)$ for selected harmonics are shown in Table 3. To deal with the insufficient resolution of today's digital oscilloscopes (typically 8-bit) the author deployed a 16-bit A/D converter with coherent sampling frequency for current measurement.

Table 3. Value of currents $i_L(t)$, $i_C(t)$ and $i_M(t)$ for selected harmonics

f [Hz]	50	**250**	**350**	**550**	**650**	850	950
$\|I_L(j\omega)\|$ [A]	38.57	9.44	4.9	3.66	2.8	2.2	1.94
$\|I_C(j\omega)\|$ [A]	0.04	9.44	4.96	3.67	2.76	0	0
$\|I_M(j\omega)\|$ [A]	38.94	0.42	0.39	0.43	0	2.2	1.96

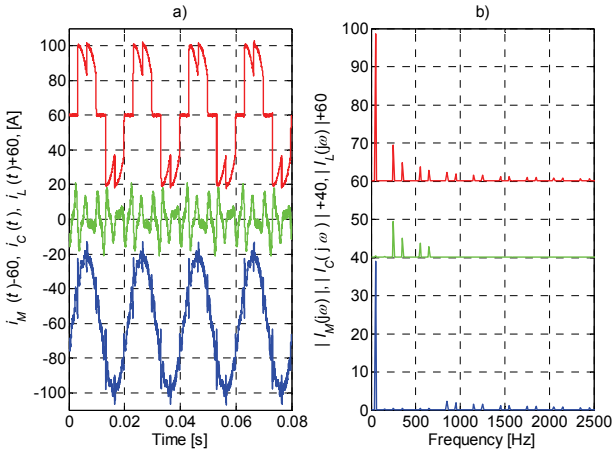

Fig. 14. Experimental results of APF compensation circuit with MDFT selective harmonics compensation for $k = \{5; 7; 11; 13\}$, for power controller with resistive load: a) waveforms, b) spectra

Compensation of selected harmonics has occurred, as predicted, though with incomplete suppression. This phenomenon is caused by dynamic distortions introduced by the APF output

circuit. These distortions are caused by a too low slew rate of the APF output (compensating) currents. The methods for elimination of such distortions are described in publications [9, 10-14].

7. Conclusion

As confirmed by the results of simulation and experimental research, the presented algorithm is highly suitable for selective harmonics compensation. Two big advantages of this algorithm are the low workload for the processor and the fast impulse response equal to 20 ms for a 50 Hz line frequency. As with all algorithms based on DFT, coherent sampling is required, thus the sampling process and control circuit should be synchronized with the power line using the PLL circuit.

The presented algorithm should also be useful for power grid resonance frequency active damping.

Further research on the considered APF will be focussed on a modification by adding a LCL output filter. In the next step it is planned to modify the considered APF by replacing the filter output LCR with a LCL filter. This will reduce the modulation components.

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