Upgraded Low Voltage Analog Current-to-Voltage Converter with Negative Feedback

Ryszard Wojtyna

***Abstract*—In this paper, an improved version of a current to voltage (C-V) converter is proposed. As compared to the previous version, the number of used transistors has been reduced by 1 and equals 7. The main results of this change are: an improvement of the circuit transfer function linearity, reduction the converter input resistance and decrease of the required supply voltage. Improvements in the considered converter results not only from the reduction of the number of the used transistors but also from the proposed realization of the feedback loop. In this way, it was possibly to get a strong loop gain. As a results, the achieved minimum supply voltage has been reduces from 2*V*, in case of the previous published converter version, to as low level as 1.2*V*, in the case of the newly proposed solution. As for the linearity of the C-V transfer function, apart from its strong loop gain, an important role play also output transistors operating in a small drain to source region (linear region). Working in this region, one obtains a quasi linear voltage to current relationship. The theoretical and simulation results are in a good agreement and are promising.**

***Index Terms*—Analog signal processing, current-to-voltage converters, feedback theory, analog CMOS electronics**

I. Introduction

ANALOG signal processing requires good quality converters of current to voltage (C-V) and voltage to current (V-C) types. This is because of the observed development of analog processing within a CMOS chip. This trend is because voltage mode and current mode operations complement each other. Current mode processing can be successfully carried out only when implemented on chip. So far, current mode signal processing is not used in digital electronics. Fortunately, the analog voltage mode and current mode combination may sometimes lead to better solution of a problem than using digital techniques. Thus, the developing advanced analog technique offers a valuable complement to traditional digital techniques. The interest in applying both voltage-mode and current-mode circuits is because the former are useful for long-distance signal transmission and the latter is useful when processing the signal locally.

Publications concerning applications of current mode circuits with negative feedback implemented in an integrated circuit form are a relatively new area of research interest. In the literature, publications about linear feedback theories one can find in [1]-[5]. Problems of untypical signal processing with the use of current mode technique are presented in [6]-[8].

Some ideas connected with current to voltage converters and their improvements have been published by the author in [9], [10], and [11].

In this paper, it is proposed a low power simple C-V converter which offers possibly good linearity of it transfer function and rather low value of it input resistance. There are two key elements which create basis of the C-V converter. The first one is two output resistors operating in linear region, where the very small drain to source voltage ensures the quasi linear current to voltage relation. This is connected with the applied small supply voltage, lower than the sum of absolute values of threshold voltages of the used transistors. The second key element is adding to the converter a negative feedback loop. Application of this loop leads to further improvement of the parameters mention, i.e. the linearity, input resistance and energy consumption of the C-V converter.

The newly presented version of the C-V converter is an improved version of that proposed in [11]. Differences between them include several factors. The first factor is reduction 8 MOS transistor to 7 one. The second is a change of the feedback loop structure. The third is the way in which transistor sizes were designed. All this factors cooperate with each others. More details about the C-V converter properties and it superiority over the converter previously published are presented in next sections.

The rest of the paper is organized as follows:

Section 2 explains advantages of applying negative feedbacks to improve electronic circuit's properties in the context of realizing the considered C-V converters.

Section 3 presents the previous version of the C-V converter with the use of 8 CMOS transistors. Weak points of this solution are discussed.

Section 4 explains why the proposed converter with the new 7 transistors is superior over the previous version of the C-V converter given in [11].

Section 5 presents the carried out SPICE simulations and the achieved results in the context of comparison between the present 7-transistors and the previous 8-transistors version. By means of SPICE, it has been confirmed that the new version is significantly better than the previous one given. Moreover, it has been shown a possibility of utilizing yet another output terminal of the C-V converter.

Section 6 includes concluding remarks.

R. Wojtyna is with the Faculty of Telecommunication, Computer Science & Electrical Engineering, University of Technology and Life Sciences, Bydgoszcz, Poland (e-mail: woj@utp.edu.pl).

II. Applying Negative Feedback to Improve Linearity, Input Resistance and Power Consumption of the Converter

To explain how a negative feedback can reduce unwanted nonlinearities of transfer functions of the considerate converters, look at the model presented in Fig. 1. In the diagram of Fig. 1, we can distinguish two amplifiers, denoted by A_{in} and A_{out}. The A_{in} block represents a linear current preamplifier while the A_{out} is a nonlinear current-to-voltage stage. The letter β represents a voltage-to-current feedback loop that is responsible for the feeding back. Output voltage, V_{out}, is send back and transforms it into the current input I_F. At this node, I_F is subtracted from the I_{in}. The obtained I_{in}-I_F current difference is provided to the preamplifier A_{in} and next to the A_{out} output amplifier.

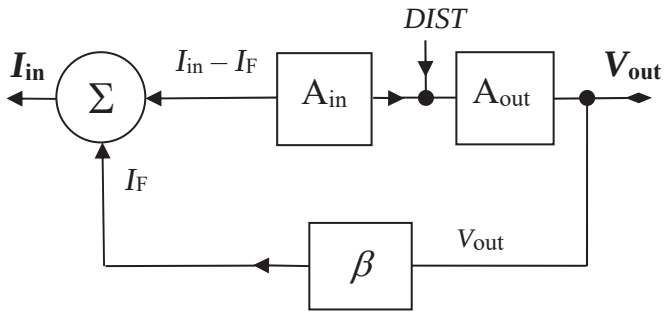

Fig. 1. Idea of applying negative feedback to decrease harmonic distortions of a circuit transfer function and to decrease input resistance of the circuit.

Apart from the external input current I_{in}, in the model of Fig. 1 there is additional internal source, denoted by *DIST* (distortion), representing nonlinear distortions. We want to get at the output a reduced nonlinearity of the circuit transfer function, represented by the *DIST* source. Making use of the existing feedback theory, one can show that the relations between I_{in}, *DIST* and V_{out} can be expressed as:

$$V_{out} = I_{in}\frac{A_{in}A_{out}}{1+A_{in}A_{out}\beta} + DIST\frac{A_{out}}{1+A_{in}A_{out}\beta} \quad (1)$$

On the right hand side of (1), the second component represents the part of output voltage, V_{out}, resulting from the distortion *DIST*. This means that distortion achieved at the output can by lower than the value of the distortion source *DIST*. This takes place if:

$$A_{in}A_{out}\beta > A_{out}, \quad (2)$$

Equivalently, the condition (2) can be expressed in the form:

$$\frac{A_{out}}{1+A_{in}A_{out}\beta} < 1 \quad (3)$$

This means that a suitable designing of the feedback loop can lead to reducing the unwanted nonlinearities, represented by *DIST*, of the considered C-V converter. To this and, a sufficiently strong feedback gain must be reached.

III. Based on 8 Transistors Quasi Linear C-V Converter

As mentioned in the introduction, in this section we will remind properties of the C-V converter circuit based on 8 transistors and published in [11]. Moreover, we want to compare effectiveness of the previous C-V converter with the new C-V converter built of only 7 transistors. Diagram of the previous 8-transistor converter is shown in Fig. 2.

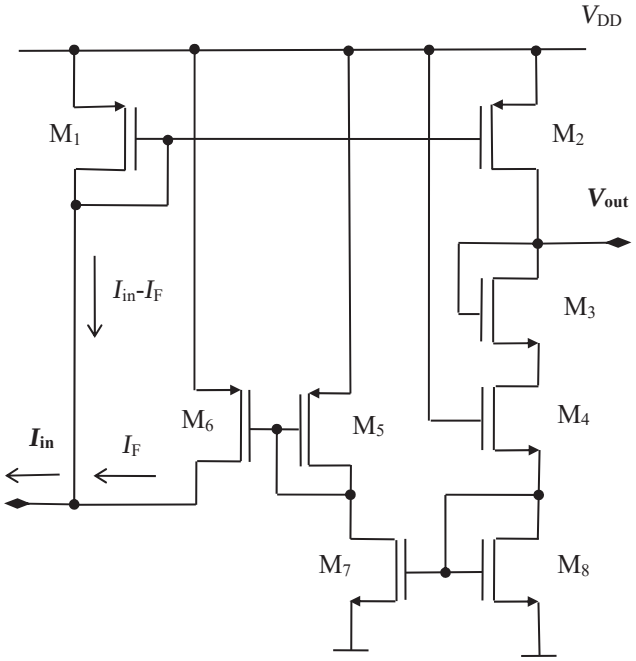

Fig. 2. The presented in [11] 8 transistor based C-V converter with 2*V* supply voltage.

The transistor pair M_1 and M_2 operate as current mirror, takes the input current, I_{in}, and transmits it to the M_2. The M_2 transistor delivers current flowing through the path between the supply rail and ground. The path includes four transistors, denoted by M_2, M_3, M_4 and M_8. The transistors M_3 and M_8 work as diodes (short circuit drain with gate). The transistors M_3 and M_8 operate with gate to source voltages being much smaller than its gate to source values. Suitably combining the M_3, M_4 transistor with the M_2, M_8 we can realize a quasi linear transfer function of our C-V converter.

The above presented discussion includes 5 transistors. Another 3 transistors give the total number equal to 8. These three transistors are denoted by M_5, M_6 and M_8 and serve to build negative feedback loop according to the principles presented in Section 2. To be precise, the transistor M_8 also participates in sending the C-V converter output voltage to create the feedback loop.

The fact that the number of transistors connected in series between the supply voltage and ground was equal to 4 made is impossible to decrease the supply voltage for a given transistor

sizes. This was the essential disadvantage of the previously presented 8-transistors C-V converter. Other features like linearity improvement and input resistance decrease were also not quite satisfactory. Our goal was to find solution of this problem without going into reducing the transistor sizes.

IV. Improved C-V Converter with the Use of Only 7 Transistors

Diagram of the proposed new version of the C-V converter is shown in Fig. 3. As already mentioned, the number of the transistors has been reduced by one in comparison with the converter presented in Section III.

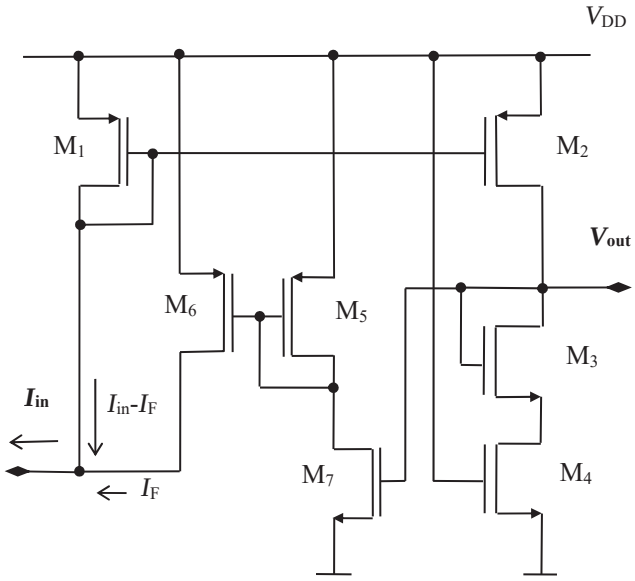

Fig. 3. Proposed in this paper C-V converter built of 7 transistors, supplied by 2*V*

From Fig. 3 it is seen that the total number of transistors connected in series between the V_{DD} and the ground is reduced from 4 to 3. This means that for the same transistor sizes, the supply V_{DD} voltage can be reduced considerably. Moreover, unlike in the previous version, gate to source voltage of the M_7 transistor can be high, far higher than gate to source voltage achievable in the converter of [11]. As a consequence, it becomes possible to enlarge gain of the feedback loop. This loop is built of 5 transistors. i.e. includes transistors numbered by M_7, M_5, M_6, M_1 and M_2. In case of the C-V converter of Fig. 2, the number of loop transistors was 6. The implemented stronger feedback loop results in achieving a better transfer function linearity of the new C-V converter. Another benefit of applying strong feedback is the obtained decrease of input resistance at the C-V converter. As a result, the input resistance can be reduced several times compared to what was offered in the converter version of Fig. 2.

V. Simulation Results of Both the 8-transistots and 7-transistors Based C-V Converters

Making use of SPICE simulator, several tests has been made concerning the version of [11] and the new version proposed in this paper. Both versions were tested applying the same CMOS technology. Threshold voltages of the used transistors are as follows: *N*-channel transistor threshold equal to V_{THN}=0.4655*V* and the *P*-channel one equal to V_{THP} = -0.617*V*. Sum of the absolute value of $V_{THN} + |V_{THP}|$ is 1.0825*V* and is only a little lower than the supply voltage equal to 1.2*V*. This means that the difference (headroom) is as small as 0.1175*V*. In case of the previous version of the C-V converter, the supply voltage was equal to 2*V*, i.e. much higher than in case of the new version.

Results of simulations concerning the previous 8 transistors version were taken from [11] and are presented for comparison reasons with the newly proposed C-V converter.

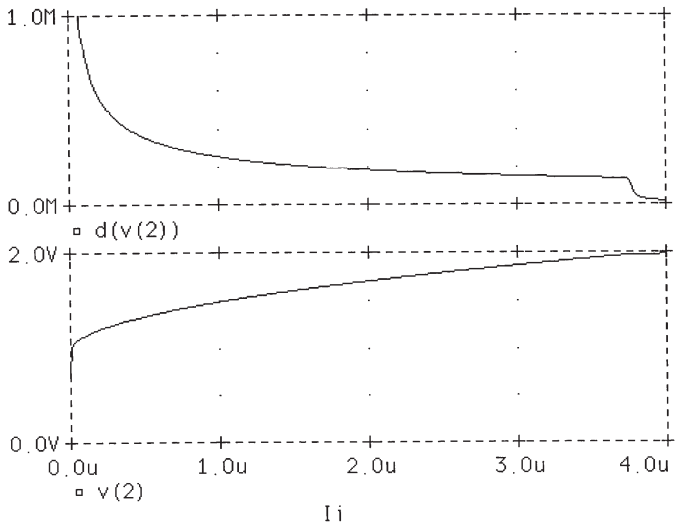

Fig. 4. Transfer function characteristics of the C-V converter with 8 transistors, supplied by 2*V*:
a) output voltage, V_o, as a function of I_{in} input current (bottom),
b) derivative $d(V_o)/dI_{in}$ as a function of I_{in} (upper).

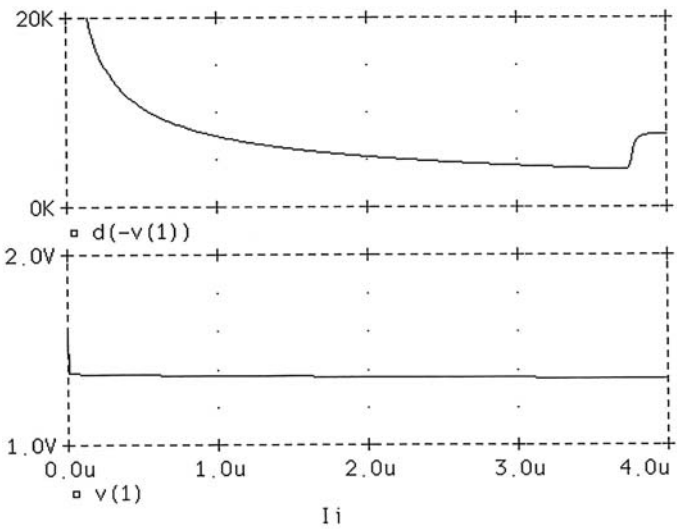

Fig. 5. Input resistance characteristics of the C-V converter with 8 transistors, supplied by 2*V*:
a) input voltage as a function of the I_{in} input current I_{in} (bottom),
b) derivative of input resistance with respect to input current as a function of the I_{in} input current (upper).

The other three figures, Fig. 6, Fig. 7 and Fig. 8, presents the simulation results concerning the 7-transitors C-V converters. Simulation results referring to the linearity of the converter transfer function are shown in Fig. 6. The bottom trace presents output voltage, V_{out}, as a function of input current, I_{in}, of the C-V converter. The upper trace shows derivative of the V_{out} with respect to I_{in} as a function of I_{in}. This trace serves as a measure of the transfer function nonlinearity. In ideal case, if the current to voltage relation is linear, the derivative given in the upper trace becomes constant and presents horizontal line. In case of Fig. 6, this takes place when the input current, I_{in}, equals about 8u*A*. Going left or right from the 8uA current, the derivative slowly goes up. This means a slow increase of the derivative value and, as a result, the increase of the function nonlinearity.

Comparing this results with the same relationships but concerning curves presented in Fig. 4, it is seen that the derivative value of the upper trace of Fig. 4 goes down. This means that ideal linearity of the C-V converter of Fig. 2 can never be achieved. In this respect, superiority of our converter is clear.

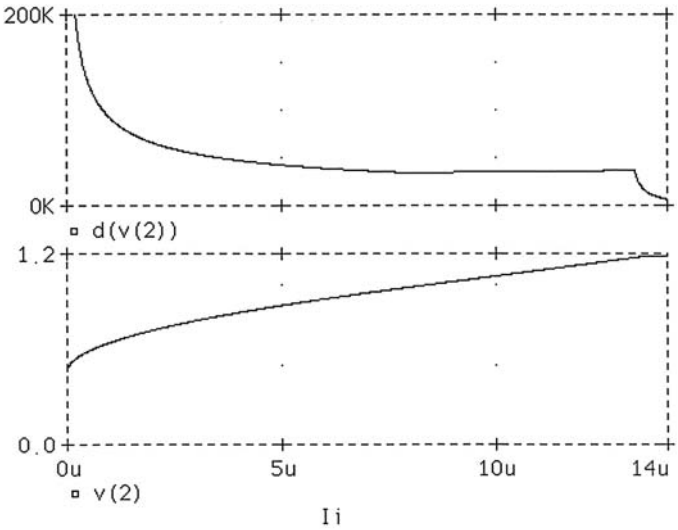

Fig. 6. Transfer function characteristics of the current to voltage converter in case of using 7 transistors and supply voltage equal to only 1.2*V*:
a) output voltage, V_{out}, as a function of I_{in} input current (bottom),
b) derivative $d(V_o)/dI_{in}$ as a function of I_{in} (upper).

Another important improvements of our C-V converter connected with the use of a stronger feedback loop relies on reducing the converter input resistance. The smaller is the converter input resistance the easier is to realize current mode operation at the input. This means that the required output resistance of the I_{in} source not necessaryly must be very large. It is the case if input resitance of the C_V converter is sufficiently low.

Input resistance of the C-V converter, which consists of 7 transistors, is presented in Fig. 7. The bottom trace illustrate static resistance while the upper trace dynamic resistance of the considered resistance. When comparing the results of Fig. 7 with that of Fig. 5 it is seen that the new C-V converter offers about three times lower input resistance in the case illustrated in Fig. 7.

What is worth emphasising is that all the improved parameters of the C-V converter result from the considerable reduction of the supply voltages from 2*V* to 1.2*V*. This, in turn, was possible after proposing a way of realizing a simple and effective feedback with a strong loop gain. The increase of the feedback loop gain enabled to realize the C-V converter with a very small headroom of the circuit. Removing the M_8 transistor play here also an important role.

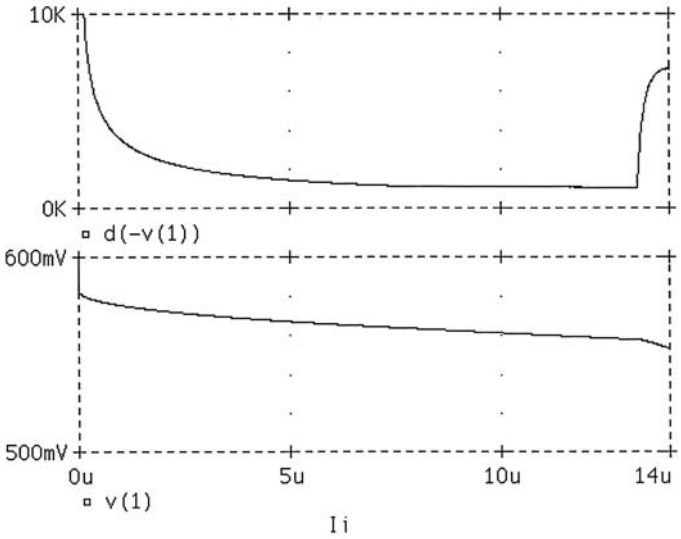

Fig. 7. Input resistance characteristics of the C-V converter with 7 transistors, supplied by of 1.2*V*:
a) input voltage as a function of the I_{in} input current I_{in} (bottom),
b) derivative of input resistance with respect to input current as a function of the I_{in} input current (upper).

Fig. 8 illustrates mechanism which functions at the output of our C-V converter. According to the theoretical predictions, the consumed supply voltage, V_{DD}, is equal to the sum of three voltages, namely M_2, M_3 and M_4, and equals 1.2*V*. This results from the diagram given in Fig. 3 and agrees with the Fig. 8. The transistor M_3 operates in saturation and is needed to introduce to the feedback loop output voltage V_{out}. Notice that the V_{out} voltage, presented in the middle curve of Fig. 8, is a sum of drain to source voltage of M_3 and drain to source voltage of M_4. In other words, the output voltage is grounded. The curve situated at the top and that in the middle resemble a mirror picture of each other. That is why the C-V converter offers the quasi linear transfer function.

From the Fig. 8 it is also seen that drain of the transistor M_4 can be used as addition output terminal of the C-V converter. However, range of the output voltage variation of this terminal is narrow. To be precise, in the bottom trace output voltages vary from zero to about 125m*V*. As regards linearity of such C-V converter, the output voltage can even be more linear than that with the output voltage taken from the transistor M_3. This results from the trace situated at the bottom of Fig. 8. If linearity is of primary importance, the transistor M_4 can be used as output terminal of the C-V converter.

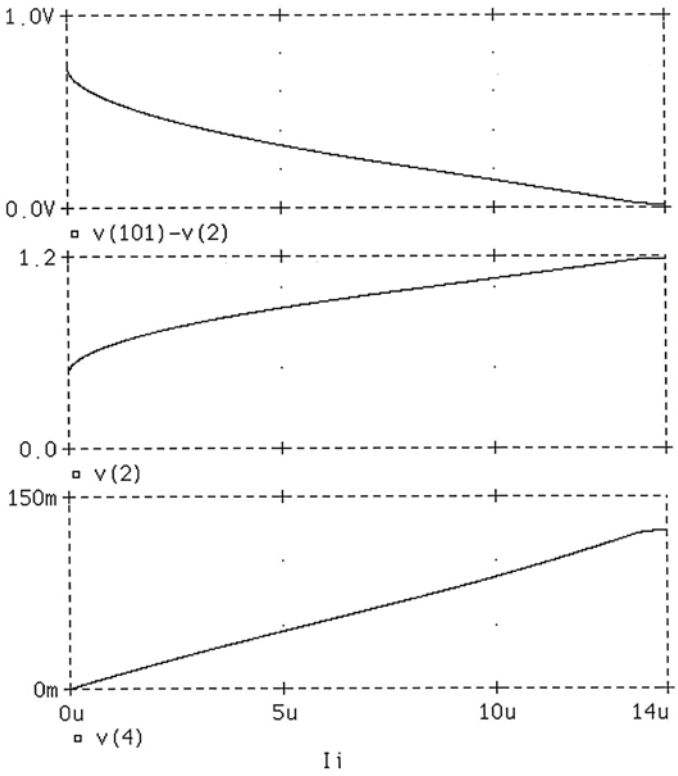

Fig. 8. Output pin voltages of the M4 and M3 transistors plus drain to source voltage of the transistor M2 in the 1.2*V* supply voltage case versus the input I_{in} current:
a) drain to ground voltage of the M4 transistor (bottom),
b) drain to ground voltage of the M3 transistor (middle),
c) drain to source voltage of the transistor M2 (upper).

VI. Conclusions

New idea and untypical approach to the problem of low power CMOS current to voltage C-V converter has been presented. The proposed new converter appeared as an improved version of the converter published in [11]. The improvement relies on a large decrease of the supply voltage, i.e. from 2*V* to 1.2*V*, on achieving more linear transfer function of the C-V converter and on significant reduction of the converter input resistance. All this improvements have been reached by reducing from 8 to 7 the number of the used transistors, by changing the applied feedback loop structure and by big enlargement of the loop gain. This was possibly due to a very small supply voltage resulting from properly designed feedback loop. For the supply voltage equal to only 1.2*V*, as small as 0.1175*V* headroom has been reached. This is a spectacularly result and I asses it as very promising. The proposed C-V converter is well suited to operate within integrated circuits. Even though the presented converter has only one output, another output terminal can also be used to this task, if the voltage will be changed in a narrow range. This is seen from the bottom trace of Fig. 8. Further research in this field will be continued.

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Ryszard Wojtyna received the M.Sc. in electronics from the Technical University of Gdańsk, Ph.D. degree in electronics from the Technical University of Poznań and Dr. of Science degree (D.Sci.) in electronics from the Technical University of Łódź, all in Poland, in 1974, 1982 and 1997, respectively. In 1974, he joined the Institute of Telecommunication, University of Technology and Live Sciences, in Bydgoszcz, Poland. Currently, he is Associate Professor at this university and head of Institute of Electronics and Computer Science. His main research interests are in the field of low-power analog signal processing based on both voltage-mode and current-mode CMOS circuits. R. Wojtyna published 146 works, including 87after receiving the D.Sci. degree. He was a supervisor of 4 doctorates, realized partly in cooperation with the University of Alberta in Edmonton, Canada. R. Wojtyna is an expert in Committee of Electronics and Telecommunication of the Polish Academy of Sciences (PAN). He is also a member of Polish Electrical Engineers Association (SEP).