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Accurate Phase Calibration for Digital Beam-Forming in Multi-Transceiver HF Radar System

Hung Q. Nguyen, Jim S. Whittington, John C. Devlin, Ha L. Vu, Ngoc-Vinh Vu, and Eddie Custovic

***Abstract*—The TIGER-3 radar is being developed as an "all digital" radar with 20 integrated digital transceivers, each connected to a separate antenna. Using phased array antenna techniques, radiated power is steered towards a desired direction based on the relative phases within the array elements. This paper proposes an accurate phase measurement method to calibrate the phases of the radio output signals using Field Programmable Gate Array (FPGA) technology. The method sequentially measures the phase offset between the RF signal generated by each transceiver and a reference signal operated at the same frequency. Accordingly, the transceiver adjusts its phase in order to align to the reference phase. This results in accurately aligned phases of the RF output signals and with the further addition of appropriate phase offsets, digital beam-forming (DBF) can be performed steering the beam in a desired direction. The proposed method is implemented on a Virtex-5 VFX70T device. Experimental results show that the calibration accuracy is of 0.153 degrees with 14 MHz operating frequency.**

***Keywords*—digital beam-forming, phased array antenna, phase calibration, radar, transceivers**

I. Introduction

THE Tasman International Geospace Environment Radar (TIGER) is a part of the Super Dual Auroral Radar Network (SuperDARN) which is an international network of HF radars dedicated to observing the auroral and polar cap ionosphere [1]. Existing TIGER operations consists of dual HF radars operating over the 8-20 MHz frequency band. Each radar has a main antenna array which consists of 16 log-periodic antennas and an auxiliary array consisting of 4 log-periodic antennas. The beam formed by this main array scans over 52° of azimuth in 16 steps separated $\approx$ 3.25^o by using a phasing network. The nominal beam widths are 4° at 10 MHz, 3° at 14 MHz and 2° at 18 MHz [2]. The phasing network consists of switchable, fixed delay lines, which produce relative time delays between the transceivers as appropriate for the selected beam direction. In the existing TIGER radars, these time delays vary with gain settings, component ageing and environment changes, hence significant calibration and maintenance is required. These limitations have been reduced in the TIGER-3 radar, currently being installed, where FPGA technology is being used to implement multi-channel transceivers and radar beam-forming.

H. Q. Nguyen, J. S. Whittington, J. C. Devlin, N.-V. Vu, and E. Custovic are with the Department of Electronic Engineering, La Trobe University, Bundoora Campus, Victoria, 3086, Australia (e-mails: qh4nguyen@yahoo.com; J.Whittington@latrobe.edu.au; J.Devlin@latrobe.edu.au; vinhvn@gmail.com; E.Custovic@latrobe.edu.au).

H. L. Vu is with Institute of Electronics and Telecommunication, Hoang Sam, Ha Noi, Vietnam (e-mail: vulehuongha@yahoo.com).

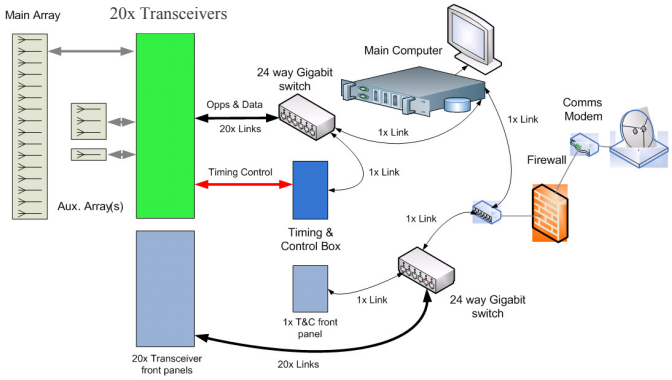

Fig. 1. Block diagram of the TIGER-3 radar system [3].

The TIGER-3 radar system, block diagram shown in Fig. 1, consists of several key components, including 20 *Transceivers*, a *Main Computer* and a *Timing-Control* box. In order to operate the radar in a certain mode, the *Main Computer* sends control data to transceivers via a Gigabit Ethernet connection. This data is processed to extract operational parameters, such as, phase offset, transmit frequency and beam number for the set-up of each transceiver. Received data streams from the transceivers are sent back to the *Main Computer* through the same Ethernet interface, where they are processed and merged to form the standard SuperDARN data set as produced by the existing TIGER radar systems.

The *Timing-Control* box provides the timing control required to coordinate 20 individual transceivers [4]. Further, for the proposed phase calibration method, the *Timing-Control* box performs reference signal generation and measures the phase difference between this signal and the RF signals fed back from transceivers. This function of the *Timing-Control* box is central to the scope of this paper, and hereafter, is referred to as Timing Hardware Server (THS) function.

The remainder of this paper is organized as follows: Section II briefly presents background information on digital beam-forming and specifies the DBF accuracy in the TIGER-3 radar. A mathematical foundation for phase measurement is introduced in Section III. Following this, Section IV provides phase measurement implementation on the Virtex-5 device utilising a CORDIC IP core. Next, Section V analyses the implementation of the method in a complete design, plus,

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empirical results are discussed. Finally, the conclusion is provided in Section VI.

II. Digital Beam-Forming and Accuracy

Beam-forming is a signal processing technique that enhances signal strength directed to or received from a particular direction. In addition, receivers using beam-forming techniques are able to reject interfering signals arriving from different directions. The principal operation is that the receivers automatically steer nulls into the direction of interferes, hence, reducing undesired noise [5]. With current DSP technology, a system with a phased array antenna and an ADC/DAC connected to each element, where signals from all elements can be processed in real-time, would produce the most flexible DBF platform. Due to its flexibility, this technique has been applied to a variety of applications, such as telecommunications, radar, sonar and speech recognition [6], [7]. This section briefly presents how DBF is performed in the TIGER-3 radar system, with the required DBF accuracy specified.

A. Phased Array Antenna and Digital Beam-Forming

Phased array antennas are used to steer radiated power towards a desired direction. One of the biggest advantages of an electronically steered array is the capability of rapid and accurate beam scanning, which permits the radar to perform multiple functions either interlaced in time, or simultaneously. Applying electronically controlled array phasing can give radars the flexibility needed to perform all the various functions in a way suited to the specific task at hand. The antenna beams in phased arrays exhibit the flexibility to be designed as needed, for instance, showing deep nulls in the direction of jammers while the main beam is nearly unaffected.

The number of geometrical arrangements, relative amplitudes and relative phases of the array elements determine the beam pattern and beam steering capability. To simplify calculations, an uniform one-dimensional array of N identical isotropic elements with identical amplitudes is considered. Figure 2 shows a linear antenna array of N elements with an inter-antenna spacing of d. The array factor is given by [8]:

$$\begin{aligned} AF &= 1 + e^{j(kd\cos\Phi)} + e^{j2(kd\cos\Phi)} + ... + e^{jN(kd\cos\Phi)} \\ &= \sum_{i=1}^{n} e^{j(n-1)(kd\cos\Phi)}, \end{aligned} \tag{1}$$

where $k = 2\pi/\lambda$, λ is the wavelength of the transmit signal.

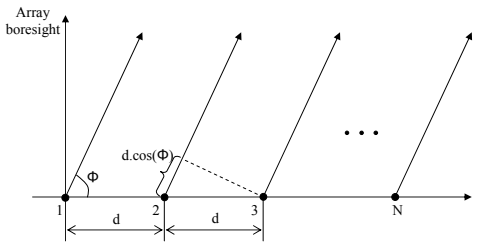

Fig. 2. Linear phased antenna array with N elements.

Equation (1) indicates that the array factor is maximum at $\Phi = 90^o$. In other words, the array has maximum directive magnitude at the array bore-sight.

Let Ψ represent the progressive phase of one element relative to the previous one, or the phase difference between two adjacent elements, we have:

$$\Psi = kd\cos\Phi. \tag{2}$$

This means that as the relative phases among the elements change, the pattern rotates so that its main lobe is in a different direction. When all the elements are in phase, that is, $\Psi = 0^o$, the pattern's maximum directive is to bore-sight, i.e. $\Phi = 90^o$.

Matlab simulations have been performed to investigate steering angle dependence on the progressive phase between adjacent elements. Figure 3 illustrates the progressive phase translation process and the corresponding rotation of the angular pattern. The simulation is performed for a 16-element uniform array with half wavelength spacing between elements, steered from bore-sight, at 90 degrees, to 85 degrees. This corresponds to the progressive phase translation from 0 to 15.7 degrees. Therefore, by changing the phase difference between elements, the array pattern can be electronically directed to a desired direction.

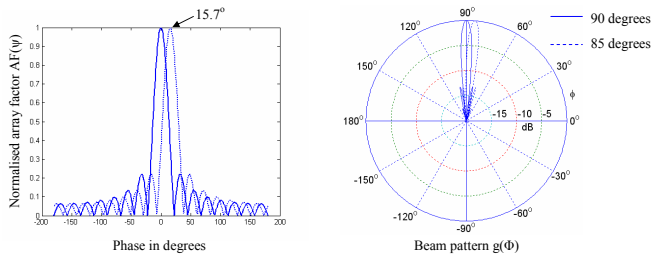

Fig. 3. Beam pattern steering 5 degrees from bore-sight.

In order to take advantages of FPGA technology, TIGER-3 employs Direct Digital Synthesizers (DDS) to generate phase offsets among transceivers. The remarkable features provided by Virtex-5 DDSs, such as, programmable frequency and phase offset setting, fine frequency and phase resolution, allow highly accurate and fine beam-forming.

B. DBF Accuracy Requirement

Since the beam-forming operation is based on the relative phases between transceivers, the beam steering accuracy must be taken into account. The relationship between progressive phase offsets and the antenna beam direction was provided in Equation (2). This is plotted in Fig. 4 with the inter-element space of a half wave length. The top graph shows the main beam scanning from 60° to 120° (with the bore-sight at 90°) as the progressive phase difference changes from 90° to -90°. The bottom graph is a zoom-in version in the beam scanning range 89.9^o – 90.1^o. The latter plot indicates that a phase offset of $\approx 0.314^o$ in adjacent elements causes the main beam to be directed to 0.1 degree from the bore-sight. This also means that, in the worst case, an approximate 0.314^o phase error in all elements causes the main beam to be 0.1 degree off the desired direction.

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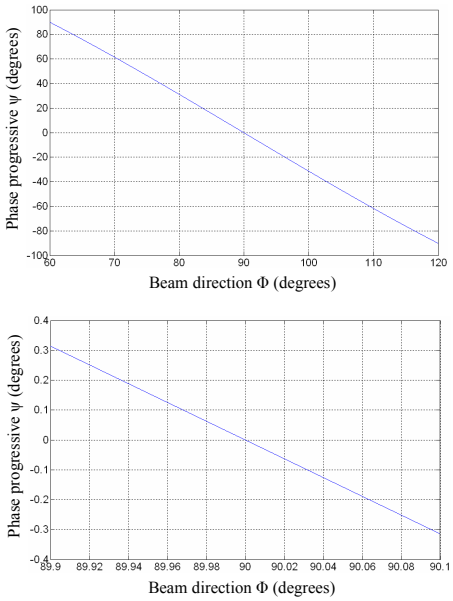

Fig. 4. Adjacent element phase progressive versus beam steering direction.

The TIGER-3 radar is capable of illuminating up to 110 range gates of length 45 km each. If the main beam is directed 0.1^o off the desired direction then the observed area is off the expected area by a certain distance. The further the observed area, the larger the deviation. Table I indicates the deviation corresponding to the observation range.

TABLE I
OFF-TARGET DEVIATION CAUSED BY 0.1^o OFF-DIRECTION BEAM

Range gate	Range (km)	Deviation (m)
1	45	78.5
2	90	157.1
3	135	235.6
...	...	...
110	4950	8639.4

This level of deviation has been set as an acceptable upper limitation for the TIGER-3 radar. In other words, the 0.314^o phase offset upper bound must be attained for RF output waveforms between transceivers over all operating frequencies. The RF phase calibration technique presented in this paper guarantees a minimum 0.314^o phase alignment between the transceivers' RF outputs.

III. PHASE MEASUREMENT BASIC CONCEPT

Transceiver RF output waveform calibration is an integral part of the synchronisation process in order to achieve the required DBF accuracy. Driven by the synchronous clock, attained by the clock synchronisation technique presented in [4], each transceiver generates RF pulse sequences utilising DDSs within the FPGA technology. The RF phase calibration technique guarantees phases of output signals from all transceivers are in phase at the bore-sight beam direction. This phase alignment is bounded by the specified DBF accuracy. In order to calibrate phase offsets among RF outputs, relative phases between them must be determined. Instead of directly measuring these phase differences, the phase of an RF signal from each transceiver is compared to the phase of a reference sine wave signal generated by a DDS on the THS. Based on this phase offset, the transceiver adjusts its phase accordingly. The basic concept of this phase offset measurement is presented in the following subsection.

A. Basic Concept

This section introduces the mathematical foundation for the proposed THS phase calibration technique based on the COordinate Rotational DIgital Computer (CORDIC) algorithm. For this purpose, calculation of a sinusoid signal phase with respect to a reference signal based on inverse tangent conversion is presented. An advantage of the proposed method is that the relative phase can be measured independently of signal magnitudes.

Assuming that two reference sinusoid signals with the same angular frequency $w = 2\pi f$ and 90-degree out of phase are generated:

$$\begin{aligned} S_1(t) &= A_{ref}\sin(wt), \\ S_2(t) &= A_{ref}\cos(wt). \end{aligned} \tag{3}$$

Further, a sinusoid signal that has the identical frequency, but an unknown phase can be represented as:

$$S_{FB}(t) = A_{FB}\sin(wt + \Delta\phi), \tag{4}$$

where $\Delta\phi$ is the phase difference that needs to be measured. After mixing the two reference signals generated in Equation (3) with this signal, we have:

$$\begin{aligned} S_{FB}(t) * S_1(t) &= A_{FB}\sin(wt + \Delta\phi) * A_{ref}\sin(wt) \\ &= \frac{A_{FB}A_{ref}}{2}(\cos(\Delta\phi) - \cos(2wt + \Delta\phi)), \\ S_{FB}(t) * S_2(t) &= A_{FB}\sin(wt + \Delta\phi) * A_{ref}\cos(wt) \\ &= \frac{A_{FB}A_{ref}}{2}(\sin(\Delta\phi) + \sin(2wt + \Delta\phi)). \end{aligned} \tag{5}$$

Using lowpass filters to eliminate the second harmonic components from the mixed signals, (5) becomes:

$$(S_{FB}(t) * S_1(t))_{fil} = \frac{A_{FB}A_{ref}}{2}\cos(\Delta\phi), \tag{6}$$

$$(S_{FB}(t) * S_2(t))_{fil} = \frac{A_{FB}A_{ref}}{2}\sin(\Delta\phi). \tag{7}$$

Based on (6) and (7), the phase difference $\Delta\phi$ can be computed as:

$$\Delta\phi = \arctan\frac{(S_{FB}(t) * S_2(t))_{fil}}{(S_{FB}(t) * S_1(t))_{fil}}. \tag{8}$$

This equation indicates that the unknown phase difference can be measured using the inverse tangent feature of the CORDIC algorithm disregarding amplitudes.

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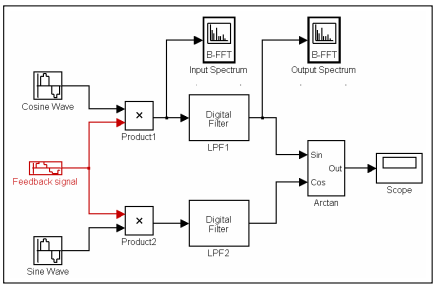


Fig. 5. Phase measurement with MATLAB modelling.

B. Concept Verification

In order to verify the correct operation of this concept, the MATLAB Simulink and DSP System Toolboxes are utilised for computation modelling in the digital domain. This verification model is provided in Fig. 5. Sinusoid input signals with the same frequency of 10 MHz are generated by sine wave generation blocks. The *Sine wave* and *Cosine wave* signals have 0 radian phase offset, while that of the *Feedback* signal is $\pi/6$ radians or 30°. Mixing operations of the *Feedback* signal with the *Sine wave* and *Cosine wave* signals are performed using simple multiplication functions. Next, the product of each multiplication is fed to the input of a lowpass filter designed using the MATLAB Filter Design Toolbox. Following the lowpass filter, these filtered signals are transferred to inputs of an *Arctan* block. The *Arctan* function then performs the inverse tangent of the quotient of the *LPF2* output divided by the *LPF1* output. Finally, the resultant phase difference between the *Feedback* signal and the other two sinusoid input signals is verified by an oscilloscope *Scope*.

Prior to discussing the verification result, a brief discussion of the lowpass filter design used for this purpose is presented. Since the generated sinusoid signals are 10 MHz, the lowpass filters are designed to eliminate the high frequency harmonic components in the mixed signals, which are at 20 MHz, while allowing the DC components to pass. To perform this requirement, the lowpass filters are designed with the following specifications: passband frequency $Fp = 4$ MHz; stopband frequency $Fst = 6$ MHz; passband ripple $Ap = 0.06$ dB; stopband attenuation $Ast = 60$ dB. As *equiripple* filter designs result in the low pass filter with the smallest possible order to meet the required specifications, *equiripple* filters are preferable for the verification. The resultant filter frequency response is shown in Fig. 6. Further details on digital filter design can be found in [9]–[11].

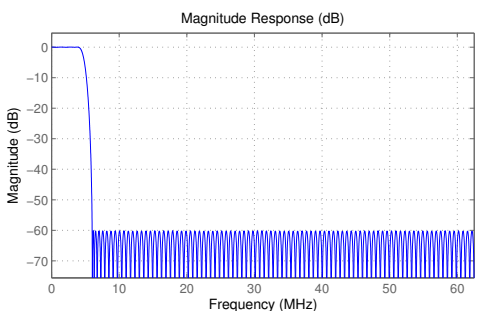
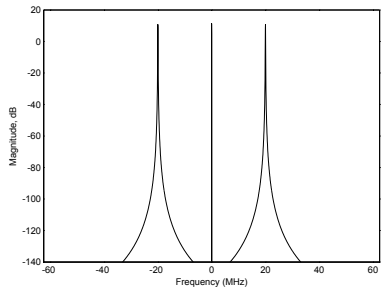
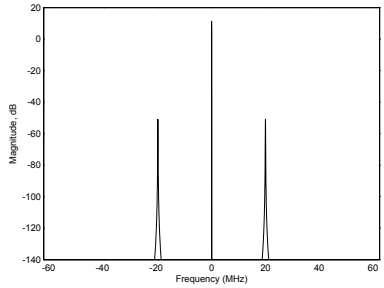


Fig. 6. LPF frequency response.

To examine the lowpass filter performance, the mixed signal generated by the *Product1* block in Fig. 5 is fed through the *LPF1* filter. Two FFT transformers are employed to explore the input and output signal spectrum of the filter. As indicated by Fig. 7, spectrum power of 20 MHz signals is attenuated by 60 dB as expected.



(a) Input signal spectrum



(b) Output signal spectrum

Fig. 7. LPF filter performance.

Once the filters were designed and their performance confirmed against the specifications, the whole model was verified for the concept discussed previously. The simulation results observed with an oscilloscope are illustrated in Fig. 8. At first, the measured phase fluctuates and then it is steady at 30 degrees after $0.5\ 10^{-6}$ seconds. The fluctuation phase is understandable and caused by signal propagation delays. This time period is mainly due to latency in the LPF filters. The higher the order of filter, the longer the delay. Consequently, the steadily output value reflects the phase offset between the feedback signal and the other two sinusoid input signals, which are pi/6 radians as mentioned previously.

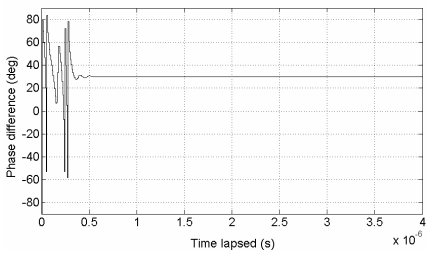


Fig. 8. Measured phase offset.

Thus far, the conceptual foundation of phase offset measurement has been confirmed for its correctness. In order to realise this concept on Xilinx hardware, the corresponding

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functional entities must be built to perform multiplication, lowpass filtering and inverse tangent functions. Virtex-5 FPGAs provide configurable resources which can be designed to perform a wide range of arithmetic and logic functions. These resources include DSP48 blocks, CORDIC algorithm, multipliers, lookup tables (LUTs) and memories. For the proposed phase measurement implementation, dedicated DSP48 slices can be used to design Finite Impulse Response (FIR) lowpass filters, while CORDIC IP cores can play the role of the inverse tangent computation.

Nevertheless, in contrast with most processors where floating-point arithmetic is performed, FPGAs utilise fixed-point arithmetic to minimise consumed resources. These resources are reduced, however, at the expense of precision. In others words, fixed-point arithmetic trades off numerical precision for hardware efficiency. With fixed-point notation, the number of bits used to represent operands is limited. The fewer the number of bits employed, the less the resource usage, yet the greater the level of quantisation error, resulting in a loss in precision. For example, if a fixed-point operand is represented with a number of fractional bits f, then the quantisation error is limited to 2^{-f}. Thus, fixed-point arithmetic-based hardware must be tested to ensure that it meets the required performance. Accordingly, the logic can grow bit-by-bit to accommodate the required fixed-point precision.

IV. Phase Measurement Implementation

Figure 9 illustrates the THS block diagram, which generates the reference sine and cosine signals and then performs the phase measurement based on the presented method. For functionality, DDS signal generation on the THS and transceivers must be configured identically using a digital implementation in FPGA hardware. A further constraint is the use of an accurate global clock to coordinate the operation of all DDS units [4]. With these constraints met, it is possible to generate reference sinusoid signals that have exactly the same frequency as the RF signals transmitted by transceivers. The return RF signal from each transceiver is mixed with sine and cosine waves generated at the same RF frequency by a DDS in the THS. The output signals of two mixers are then filtered utilising FIR lowpass filters. Following this, two filtered signals are transferred to the two inputs of a CORDIC IP core. Finally, the phase difference between the returned RF signal and the local reference signal is calculated by the CORDIC algorithm as shown in Equation (8).

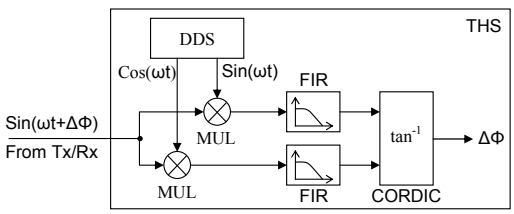

Fig. 9. Phase measurement block diagram.

This design has been implemented in a Virtex-5 VFX70T device using Xilinx System Generator, a system-level tool providing high-level abstractions that can be compiled into FPGA hardware. The tool also provides access to underlying FPGA resources through low-level abstractions, allowing the construction of highly efficient FPGA designs. System Generator also works in conjunction with Simulink to provide a modelling environment to assist design verification. During the design phase, Simulink simulations were employed for testing purposes. This verification compares the phase measurement precision between the designed fixed-point performance with the equivalent floating-point design that follows exactly the same arithmetic concept.

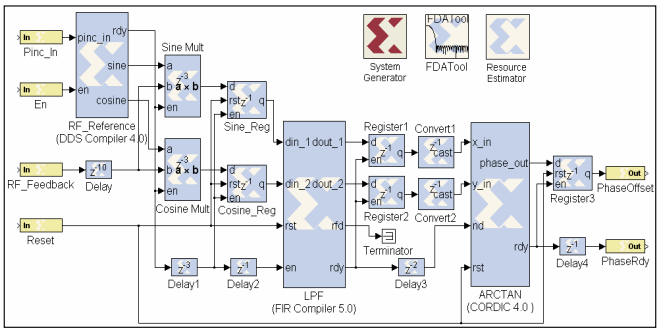

Fig. 10. Phase measurement using CORDIC algorithm.

Figure 10 illustrates the phase measurement hardware circuit designed in the System Generator. The DDS core generates sine and cosine waves with the exact frequency of the *RF_Feedback* signal from transceivers based on the *Pinc_in* input controlled by a higher-level design of THS. For the best frequency resolution of the transmit RF signals, transceiver DDSs are implemented with the highest available resolution of 48 bits. Therefore, the DDS on THS must have the same resolution in order to provide the same frequency reference signals, yielding a *Pinc_in* of 48-bit width. The lowpass filter *LPF* is designed with an FIR Compiler that targets the dedicated DSP48 hardware resources in the Virtex-5 device. The *ARCTAN* block, which is designed with the CORDIC Compiler, calculates the phase offset according to the filtered signals output from the lowpass filter. An important point is that data processing for the LPF filters and CORDIC algorithm are constructed with parallel architectures to maximise processing speed. Following this design flow, details of the two most important blocks, *LPF* and *ARCTAN*, are presented.

A. Lowpass Filter Design

The FIR Compiler IP core provided by Xilinx supports implementation of a variety of filter types from single-rate to multi-rate filters. The FIR Compiler can support input data and filter coefficients of bit-width up to 49 bits, thus providing significant precision. More details about the Compiler can be found in [12]. The filter coefficients can be designed using standard MATLAB functions such as $fir2$ or the MathWorks FDAtool. For this design, the FDAtool was utilised.

Since TIGER-3 operates in the 8-18 MHz frequency range, the reference sinusoid signals generated on THS must support frequencies within this range. Therefore, the goal of the lowpass filters is to attenuate all components in the $[16, \infty]$ MHz frequency range in order to filter out the two-fold RF frequency

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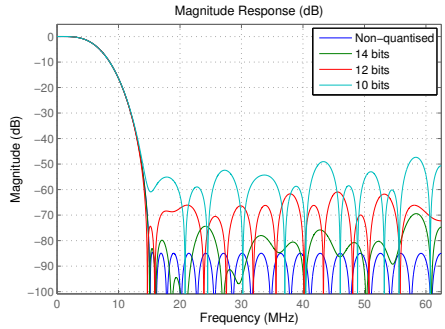
components in the mixed signal as provided in Equation (5). The passband and stopband frequency are specified accordingly at 1 and 15 MHz, respectively. In order to conserve the spurious-free dynamic range of the RF signals which are digitalised by 14-bit ADCs, DACs, the filter attenuation at passband is 84.6 dB whilst the stopband is 0.6 dB.

B. FIR Quantisation Error

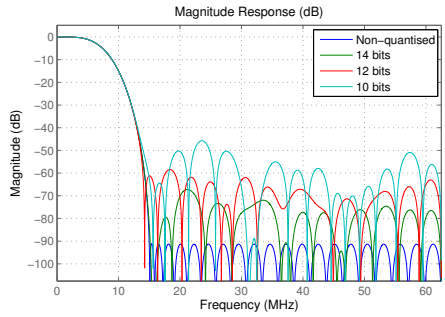
One of the factors that limits phase measurement accuracy is the quantisation error in fixed-point arithmetic. Therefore, investigating the impact of quantisation error on filter performance is necessary. Based on this investigation, the fixed-point data format for FIR inputs and coefficients is specified. In order to examine the quantisation error effect, the filter magnitude response is analysed for various quantisation levels. This analysis is performed with the MATLAB code provided in Fig. 11. The filter floating-point coefficients with given specifications are generated utilising the FDATool. These coefficients are then quantised with different fractional bit lengths. Accordingly, discrete-time, direct-form FIR lowpass filters are constructed with corresponding sets of coefficients.

```
% Loads filter coefficients created by FDATool
load xlfda_numerator.mat;
% Constructs a direct-form FIR filter with non-quantised coeffs
Hd_nq = dfilt.dffir(xlfda_numerator);
for F_Len = 1:49
   % Creates a quantizer object with:
   %   Signed fixed-point mode.
   %   Round towards nearest.
   %   Saturate at max value on overflow.
   q = quantizer('fixed', 'round', 'saturate', [F_Len+2 F_Len]);
   % Quantises coefficients
   qCoeff = quantize(q,xlfda_numerator);
   % Constructs a direct-form FIR filter with quantised coeffs
   Hd(F_Len) = dfilt.dffir(qCoeff);
end
close all;
% Analyses filter with different quantised levels
fvtool(Hd_nq,Hd(14),Hd(12),Hd(10));
legend('Non-quantised', '14 bits', '12 bits', '10 bits');
```

Fig. 11. FIR quantisation error MATLAB code.



(a) 36-tap FIR lowpass filter



(b) 45-tap FIR lowpass filter

Fig. 12. Impact of quantisation error on FIR filter magnitude response.

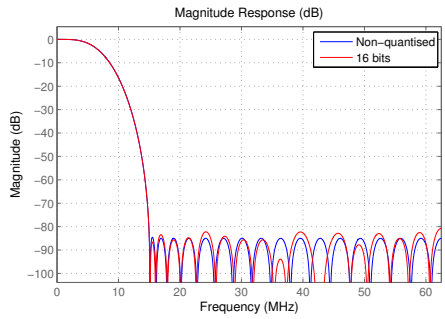


Fig. 13. Designed 36-tap FIR filter with 16-fractional-bit quantisation.

Though the FIR core is able to manage input data and filter coefficients up to 49-bit precision, Fig. 12 shows the magnitude response of the FIR filter with given specifications and quantized at a number of moderate levels. For comparison purposes, the non-quantized magnitude response is also provided. The figure indicates that once quantised up to 14 fractional bits, the stopband attenuation is less than 80 dB at various frequency bands. This is due to the poor utilisation of the available range for the quantised coefficients. The situation is unimproved when the filter order is increased from 36 to 45. On the other hand, there is significant improvement in the non-quantised magnitude response. Consequently, the trade-off solution is to quantise the 36-tap FIR filter with 16 fractional bits. This configuration ensures the stopband attenuation is marginally less than 84 dB as illustrated by the filter magnitude response shown in Fig. 13.

Furthermore, the number of DSP slices utilized by the FIR Compiler is primarily determined by the input data and coefficient bit width. As suggested by Xilinx [12], when the data and coefficient widths are specified to be greater than the input width of the DSP slice for the given device family, the core uses multiple DSP slice columns to implement the filter. Once configured with 16-bit width unsigned coefficients and data, each filter consumes only 2 DSP48 slice columns, thus minimizing the total DSP slice usage.

The designed filter performance quantised with 16 bits is examined using a combined signal which is mixed from two sinusoid signals with the same 12.5 MHz frequency but different phases. The spectrum of the input and output signals shown in Fig. 14 indicates that the frequency components at 25 and 50 MHz are attenuated about 80 dB by the filter, while the DC component is conserved. Consequently, the power spectrum of the spurious signals are approximately 84 dB less than the DC signal power spectrum as required.

C. CORDIC-Based ARCTAN Design

The Xilinx CORDIC IP core is designed to perform either vector rotation or vector translation. For vector rotation, a vector (X, Y) is rotated through a certain angle yielding a new vector (X', Y'), whilst vector translation rotates the vector

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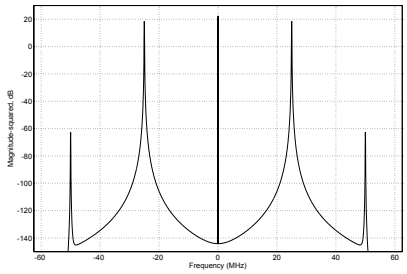
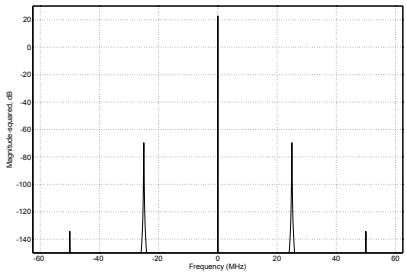


(a) FIR input signal spectrum



(b) FIR output signal spectrum

Fig. 14. FIR filter performance.

(X, Y) around the unit circle until the Y component equals zero.

In order to calculate the phase of the input vector (X, Y), a vector translational function is configured for the core. The input vector is rotated in a sequence of smaller steps, which are referred to as *micro-rotations*. Assuming that it takes n *micro-rotations* to calculate the inverse tangent of an input vector (X, Y) for a full translation, the vector rotation for n iterations can then be expressed as in Equation (9) below [13]:

$$\begin{aligned} X' &= \prod_{i=1}^{n} cos(atan(2^{-i}))(X_i - \alpha_i Y_i 2^{-i}), \\ Y' &= \prod_{i=1}^{n} cos(atan(2^{-i}))(X_i + \alpha_i Y_i 2^{-i}), \\ \theta' &= \sum_{i=1}^{n} \theta - (\alpha_i . atan(2^{-i})), \end{aligned} \tag{9}$$

where, $\alpha_i = \pm 1$ is the rotation direction.

Therefore, each $micro - rotation$ stage can be considered as a simple shift and add/subtract operation. Since speed is important for the synchronisation design, the CORDIC is configured in fully parallel architecture to increase throughput of the rotation algorithm.

D. CORDIC Quantisation Error

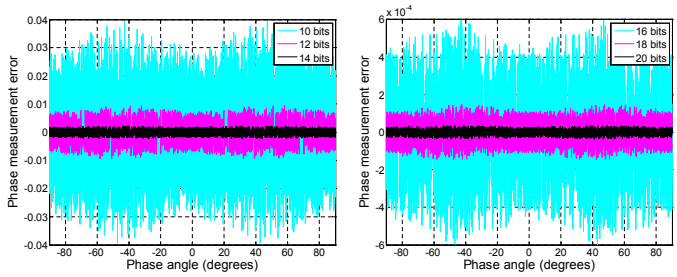
Since the CORDIC core is capable of performing with a wide range of input and output data widths that can be configured in the range of 8 to 48 bits, the input quantisation error effect is investigated for the entire range. MATLAB code presented in Fig. 15 is used for this purpose.

As illustrated in the code block, the phase offset angle *theta_rad* is tested in the $[-\frac{\pi}{2}, \frac{\pi}{2}]$ range. The $sin(theta_rad)$, $cos(theta_rad)$ inputs are quantised and

```
for F_Len = 8:48
   % Creates a quantizer object with:
   %   Signed fixed-point mode.
   %   Round towards nearest.
   %   Saturate at max value on overflow.
   q = quantizer('fixed', 'round', 'saturate', [F_Len+2 F_Len]);
   % Sum of Squares
   SS = 0;
   for i=1:1001
      theta_rad = -pi/2 + pi*(i-1)/1000;% Phase offset (radians)
      theta_deg = -90 + 180*(i-1)/1000; % Phase offset (degrees)
      qSin = quantize(q,sin(theta_rad));% Quantised Sine
      qCos = quantize(q,cos(theta_rad));% Quantised Cosine
      % Phase offset measurement error
      qErr(F_Len,i) = theta_deg - (atan(qSin/qCos))*180/pi;
      SS = SS + qErr(F_Len,i)^2;        % Sum of Squares
   end
   % RMS of phase offset measurement error
   qRMS(F_Len) = sqrt(SS/1001);
end
```

Fig. 15. CORDIC quantisation error MATLAB code.

then calculated for inverse tangent. As with the FIR design, quantisation errors need to be taken into account when implementing the CORDIC algorithm. The phase measurement error is the difference between the ideal phase and the calculated phase. This error is calculated for a number of moderate quantisation levels as shown in Fig. 16. The figure indicates that at all quantisation levels the phase measurement error varies over the whole range of the input phase offset angles. The phase error is at a maximum when the phase offset input is of -45° or 45°, and vice versa; and it is minimised at –90, 0, or 90 degrees. This means that the phase output error is dependant on the magnitudes of the CORDIC inputs, or precisely, on the $\frac{sin(theta_rad)}{cos(theta_rad)}$ ratio as stated by Xilinx in [13].



a) Quantisation with 10, 12 and 14 bits b) Quantisation with 16, 18 and 20 bits

Fig. 16. Impact of quantisation on phase measurement.

TABLE II
QUANTISATION AND CORRESPONDING PHASE MEASUREMENT ERRORS

Frac. bits	8	9	...	47	48
QE (deg)	1.95e-3	9.77e-4	...	3.55e-15	1.78e-15
RMS PE (deg)	6.56e-2	3.30e-2	...	1.20e-13	6.10e-14

Table II illustrates the relationship between the number of fractional bits versus quantisation errors (QE) and the corresponding RMS phase measurement errors (PE). It can be seen that the phase measurement error decreases roughly by half for each increase of one fractional bit in quantisation. The maximum accuracy that can be achieved with 48-bit quantisation is 6.10 10^{-14} degrees. The table also shows that at each quantisation level, the phase error is not simply dependent on the quantisation error in fixed-point arithmetic.

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To some extent, the RMS of phase errors are significantly higher than the quantisation errors. For example, if the inputs are quantised with 8 fractional bits, the quantisation error is $1.95\ 10^{-3}$, whilst the RMS phase measurement error is $6.56\ 10^{-2}$ degrees. However, the RMS phase error at 8 fractional bits is still superior to the required DBF accuracy specified previously, which is 0.314 degrees. Therefore, in this mechanism, the goal is to achieve a compromise on the best phase measurement accuracy with hardware efficiency. For this purpose, 16-bit quantisation is a trade-off solution, providing $\pm 6\ 10^{-4}$ degree precision. This results in an overall phase measurement accuracy of sufficient quality as presented later in this section.

E. Phase Measurement Design Verification

Once the phase measurement hardware circuit was completely implemented, its performance was verified with an equivalent function modelled in floating-point arithmetic. The testing sinusoid signals are simulated with the same frequency and phase offset as in the two models. In order to compare the performance of the two circuits, the measured phase is probed in each model, along with the phase error, which is the phase difference between the resultant phases is also illustrated in Fig. 17.

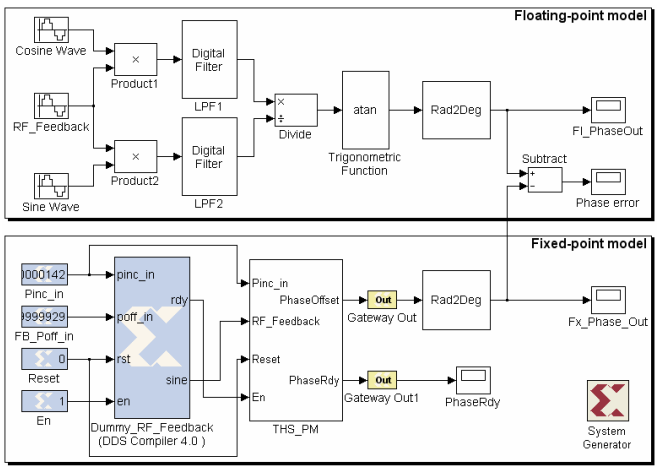
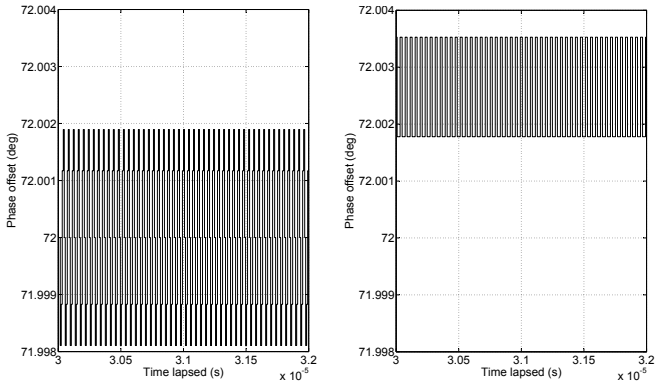


Fig. 17. Phase measurement verification.

For the fixed-point test bench, additional functions are built around the phase measurement circuit, indicated by the THS_PM block in Fig. 17. Another DDS Compiler is deployed to generate a sine wave signal, playing the role of the RF signal fed back from a transceiver. This DDS, together with the DDS inside THS_PM, generates sinusoid signals at the same 12.5 MHz frequency. For the first investigation, the phase offset configured for the two models is 72°. The phase measured in each model is converted to degrees and then subtracted from each other to calculate the phase error.

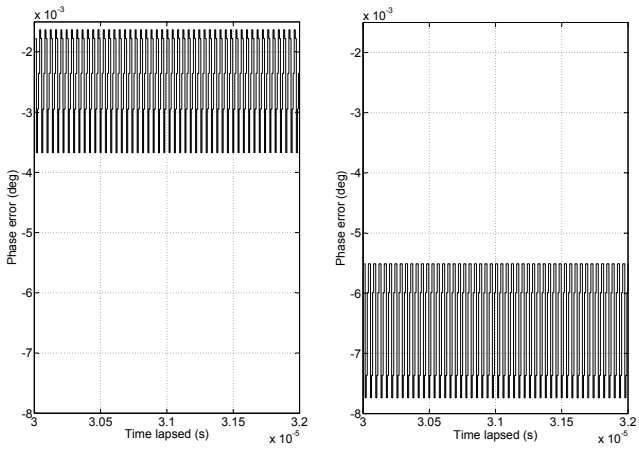
The measured phase offsets are plotted in Fig. 18. It is reasonable that the phase error of the fixed-point model is marginly worse than that of the floating-point model. These account for $3.53\ 10^{-3}$ compared to $1.89\ 10^{-3}$ degrees, respectively.



(a) Floating-point model (b) Fixed-point model

Fig. 18. Phase offset comparison.

As mentioned previously, the accuracy achieved in the fixed-point model varies with the magnitudes of the CORDIC inputs. In other words, it depends on the phase offset needed to be measured. The worst case scenarios specified are with $\pm 45^o$ phase offset. Figure 19 illustrates the phase error between the two models for 72° and 45° phase offsets. It can be clearly seen that the absolute phase error at 45° is $7.74\ 10^{-3}$ degrees, significantly higher than the $3.67\ 10^{-3}$ degrees at 72°.



(a) At 72° phase offset (b) At 45° phase offset

Fig. 19. Phase error comparison.

Consequently, the proposed phase measurement scheme is able to measure phase difference between sinusoid signals with a phase error of $7.74\ 10^{-3}$ degrees in the worst case scenario. Though, this achievement can be improved, the proposed phase measurement configuration is a trade-off solution between accuracy and efficient use of hardware resources.

V. CORDIC-Based THS Implementation and Experimental Results

A. Concept Design

Before implementing the RF phase calibration mechanism as a real application in the TIGER-3 radar system, the concept design was verified with a reduced system of two dummy transceivers. This concept was designed and analysed with the System Generator as shown in Fig. 20. Two DDSs perform the

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task of generating signals which mimic the role of dummy RF signals fed back from two transceivers. These DDSs are configured to generate sine wave signals at the same 12.5 MHz frequency with an *RF_Freq* input and are initialised with different phase offsets 54° and 234° for *DDS1*, *DDS2* by *Init_PO1* and *Init_PO2*, respectively.

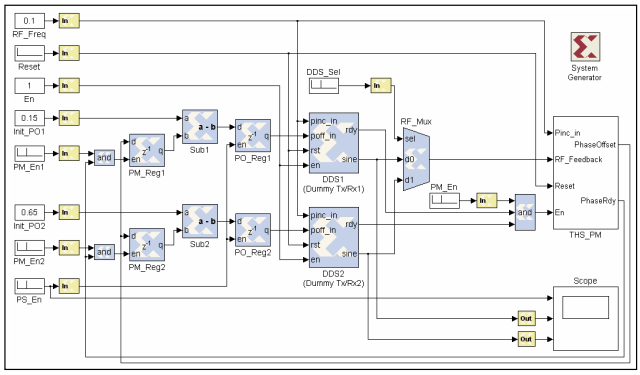

Fig. 20. THS concept design with two dummy transceivers.

The output signal of each DDS is multiplexed by the *RF_Mux* multiplexer and sent to the *THS_PM* for phase measuring. When active, the *PhaseRdy* signal indicates valid data on the *PhaseOffset* output. This measured phase is then stored in a corresponding register. Once the phase measurement is complete, using the two DDSs, in order to synchronise phases of the DDSs' output signals, the phase offset values for two DDSs are adjusted by subtracting the original phase offsets to the respective measured phase values, under the control of the *PS_En* phase shift enable signal. This ensures that the DDSs output signal phases are aligned to the DDS output phase on the *THS_PM*, and hence, aligned to each other.

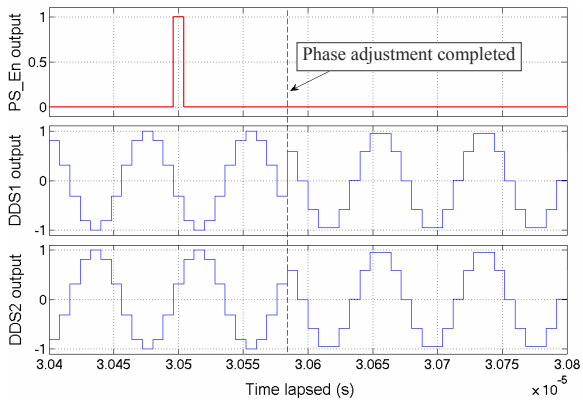

Fig. 21. DDSs outputs synchronisation.

An example of the phase relationship between two DDSs is illustrated in Fig. 21, resulting from a Simulink simulation. According to the figure, before phase synchronisation is activated, the DDSs outputs are 180 degrees out of phase due to the original phase initialised for each DDS. Once enabled by the *PS_En* signal, the phase adjustment stage is activated on the DDSs and completed after 10 clock cycles (80 ns). This results in the required phase alignment at the output signals of the two DDSs.

B. Implementation and Empirical Results

Motivated by the result of the concept simulation, a CORDIC-based phase synchronisation for 20 transceivers is implemented. In order to feedback the RF signals from 20 transceivers to THS, an analogue summer is utilised instead of the multiplexer in the concept design. Since the summer output is a summed signal of all 20 feedback signals from the transceivers, only the second DAC on one transceiver is activated at a time. This guarantees that phase measurement is performed for only one transceiver at a time.

Utilising a dual DAC on each transceiver allows phases of transmit RF signals to be calibrated on-the-fly. The first DAC channel is driven by a DDS which is configured with calibrated DBF phase information. This RF signal is then amplified and fed to the antenna array for the radar transmission purpose. The second DAC channel is driven by a separate DDS, clocked identically with the same frequency and a 0-degree phase offset. The output signal of this DAC is fed back to the 20-way RF summer, when required, as illustrated in Fig. 22. These two functions are performed independently, yet synchronously, due to the parallel architecture of FPGA technology. This implementation provides an achievable real-time phase calibration for any operating frequency without interfering with the radar operation. The phase calibration algorithm for the TIGER-3 system with 20 transceivers follows.

```
while {1} do
    for i ← 1 to 20 do
        Disable all second DACs;
        Activate second DAC on Tx/Rx(i);
        Enable THS_PM;
        while not(PhaseRdy) do
            Wait here;
        end
        Store PhaseOffset(i);
        Disable THS_PM;
        Calculate new phase offset;
    end
    Update DDSs with new phase offsets;
end
```

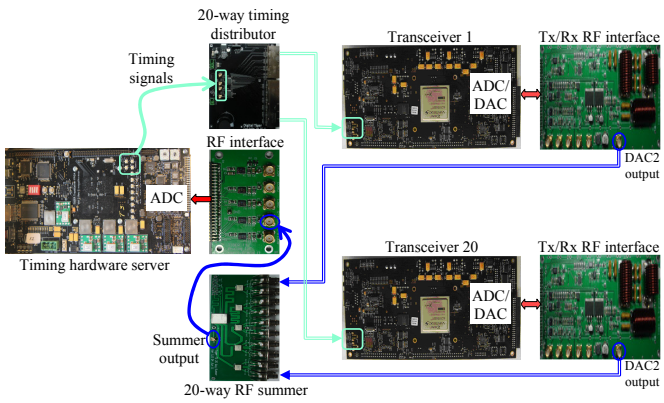

Fig. 22. CORDIC based synchronisation TIGER-3 radar system.

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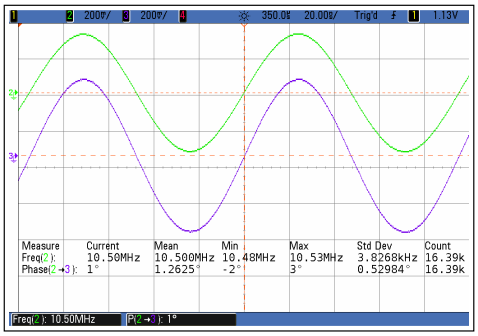
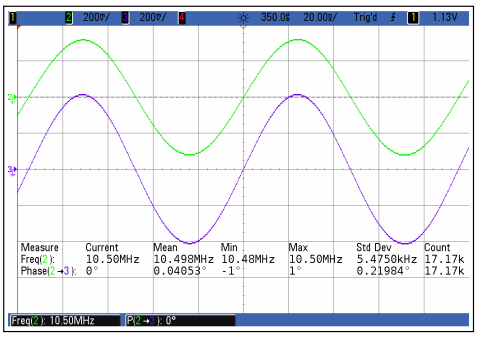


(a) Before calibration



(b) After calibration

Fig. 23. RF phase relationship between two transceivers.

Figure 23 shows empirical results of the presented phase calibration circuit. For this experiment, three transceivers were operated at a mid-range frequency of 14 MHz. As indicated by the figure, the average of phase offsets between channel 3 and channel 4 against channel 2 are originally 1.089^o and 1.132^o for 2.1 million cycles. After calibration, these offsets are significantly reduced to 0.129^o and 0.153^o, respectively. The achieved accuracy is lower than the estimated 7.7410^{-3} degree phase error from the Simulink simulation. There are several possible reasons for this, including limited precision of the oscilloscope, unmatched propagation lengths among the feedback cables from the transceivers to the summer, and mismatches among the cable lengths from the DAC outputs to the oscilloscope. However, the resultant accuracy is superior to the required DBF accuracy of 0.314^o, specified previously.

VI. Conclusion

Accurate digital beam-forming is essential to the operation of any systems utilising a phased antenna array. For the digital TIGER-3 radar, each antenna is connected to an individual transceiver. The combination of phase differences between transceiver output waveforms steers the main beam of the antenna array. Therefore, correct phase relation between transceivers must be maintained at all times for precise radar operation. A real-time accurate phase calibration method has been proposed, analysed and implemented using FPGA technology. In order to address phase mismatch problems within RF signals at the outputs of transceivers, this method sequentially measures phase of each signal with regard to a reference signal. Once the measurement cycle is complete, these phase offsets are taken into account to calculate overall phases required for accurate digital beam-forming across the entire system. Experimental results indicate the worst phase calibration accuracy is in the order of 0.153^o at an RF frequency of 14 MHz. It should be noted that this accuracy could be further improved at the expense of FPGA hardware resources. Although, the achieved result is at a superior quality and meets the requirements of the TIGER-3 radar system, allowing digital beam-forming to be operated at a very fine resolution.

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