Łukasz NIEWIARA*
Michał SKIWSKI*
Tomasz TARCZEWSKI*
Lech M. GRZESIAK**

COMPUTER AIDED DESIGN OF SNUBBER CIRCUIT FOR DC/DC CONVERTER WITH SiC POWER MOSFET DEVICES

In this paper a computer aided design of snubber circuit for DC\DC converter is presented. Due to the presence of parasitic LC circuit in the power stage (inductance and capacitance), it is necessary to use an additional snubber circuit for voltage overshoot and oscillations reduction. A simulation model of the converter with parasitic circuit was designed. Three types of snubber circuits (C, RC, RCD) were investigated in simulation tests. Simulation model of the proposed system has been investigated in Matlab/Simulink/PLECS environment. Input signal parameters like voltage overshoot, rise time, fall time were compared for considered snubber circuits. Experimental tests were carried out for the best simulation result. It confirm the proper choice of snubber circuit.

KEYWORDS: DC\DC converter, snubber circuit, SiC MOSFET

1. INTRODUCTION

SiC based power devices like MOSFET transistors and schottky diodes can reduce power losses and allow for switching frequency increase [1-2]. The use of fast SiC power devices for pulse-width modulation (PWM) converters carries out certain problems. Due to the presence of parasitic LC circuit the input signal deteriorates. Voltage overshoots and oscillations appear. It is necessary to use an additional snubber circuit to reduce the effects of parasitic circuit reactance. High switching frequency operation and high efficiency requires a proper PWM signal generation. It is necessary to generate a rectangular shaped signal.

The main task of the snuuber is to absorb energy from the reactive elements. The benefits of this can be voltage overshoots clamping and oscillations reduction. A properly designed snubber may increase the switch reliability by reducing the amount of stress [3-5]. The design process require a choice of snubber configuration and selection of proper components values. The article describes the design process and considered snubber configuration comparison.

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* Nicolaus Copernicus University, Toruń.
**Warsaw University of Technology.

2. CONVERTER TOPOLOGY

Proposed DC\DC converter topology consists a output RLC circuit fed from 2 SiC MOSFET transistors in a half bridge configuration. It's a buck configuration. The converter model contains a parasitic circuit. An additional circuit is formed by parasitic MOSFET output capacitance and path inductance. The circuit is shown in Fig. 1.
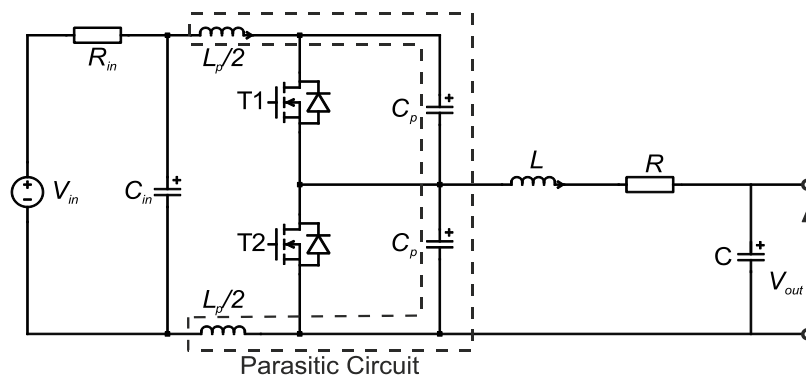

Fig. 1. Converter topology with Parasitic Circuit

The parasitic capacitance and inductance cause large turn-on oscillations in the PWM input signal (Fig. 2). There can be seen a big voltage overshoot.
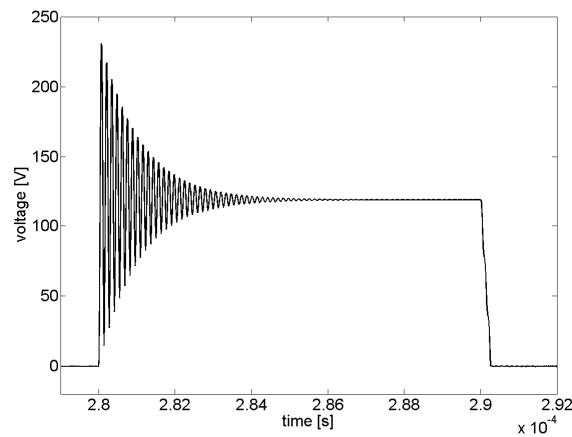

Fig. 2. PWM input signal without snubber circuit

In order to reduce voltage overshoot and oscillations, a snubber circuit should be used. The snubber circuit improves the input signal shape.

3. SIMULATION MODEL

This paper considers three types of snubber circuits shown in Fig. 3. Simulation tests of the converter with additional snubber circuits has been investigated in a Matlab/Simulink/PLECS environment.
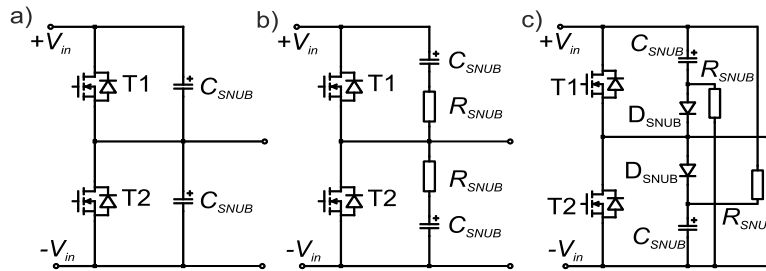

Fig. 3. Snubber configuration: a) additional capacitor, b) RC snubber, c) RCD snubber

Designed simulation model contain the parasitic inductance and capacitance (Fig. 1). It was necessary to determine the parameters of the parasitic circuit in order to create a proper simulation converter circuit model. The semiconductors output capacitance was measured using APPA 703 LCR METER. Determination of circuit inductance required frequency measurement of the input signal oscillations. The frequency was measured using TEKTRONIX TPS2024B oscilloscope with Tektronix P5122 voltage probe. It was not necessary to take into account frequency changes caused by damping in the circuit. The used approximation does not affect the behavior of proposed circuit model. The inductance can be calculated from resonant frequency of LC circuit as follows:

$$L = \frac{1}{4\pi^2 f^2 C} \tag{1}$$

where: L - parasitic inductance, f – input signal oscillations frequency, C – parasitic capacitance. Experimentally determined parameters are given in Table 1.

Table 1. Parasitic circuit parameters

C [nF]	5.0	F [MHz]	7.35	L [nH]	93.8

4. SIMULATION TEST RESULTS

The behavior of PWM input signal, obtained in a simulation study environment for converter with additional capacitor (Fig. 3a) is shown in Fig. 4. It can be seen that the use of a capacitor for the snubber circuit reduces the voltage overshoot and oscillations (with comparison to waveform presented in

Fig. 2). The overshoot value is still significant and is about 60V. Relative long fall time observed in Fig. 4 is caused by capacitor discharging. Large overshoot and long fall time cause, that considered snubber configuration is not suitable for high frequency DC/DC converter.
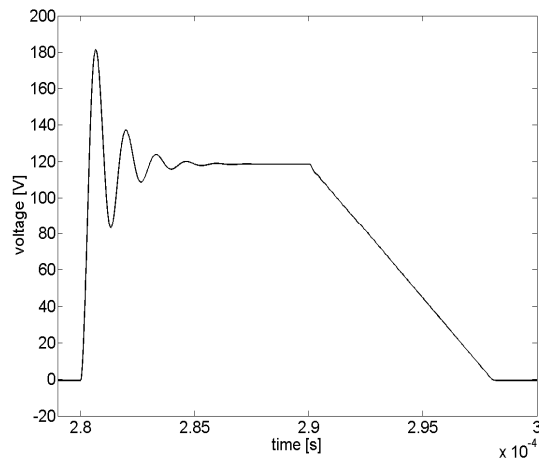

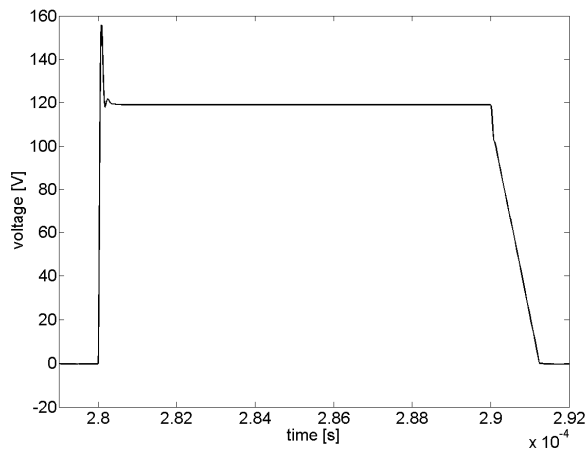Fig. 4. Input signal with additional capacitor

Fig. 5. Input signal with RC snubber

The behavior of input signal obtained in a simulation study environment for circuit with RC snubber circuit (Fig. 3b) is shown in Fig. 5. It can be seen that the use of an additional RC circuit reduces the voltage overshoot and oscillations. The overshoot value is about 40 V. There also can be seen the increase of fall time but it is smaller with comparison to snubber with single

capacitor. The energy stored in the capacitor were dissipated on the resistor. The presence of an additional resistor improves energy losses in a converter. Considered snubber topology cannot be used in a high efficiency converter.

The behavior of input signal obtained in a simulation study environment for circuit with RCD snubber circuit (Fig. 3c) is shown in Fig. 6. It can be seen that the use of an additional RCD circuit reduces the voltage overshoot. The overshoot value is about 20 V. There also can be seen that the fall time is very short. This configuration reduces the energy losses on the resistance thanks the diode. Due to small overshoot and fall time, considered snubber topology is suitable for use in a SiC Mosfet based DC/DC converter.
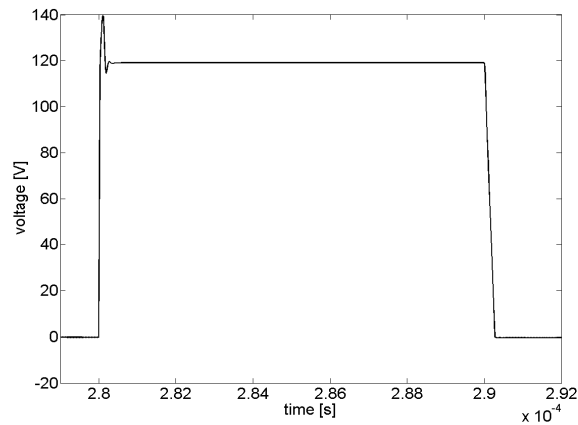

Fig. 6. Input signal with RCD snubber

Table 2. Input signal quality indicators for different snubber configurations

Configuration	Overshoot [%]	Rise time [μs]	Fall time [μs]	$T_{s2\%}$ [μs]
-	92.40	0.042	0.207	4.522
C	49.53	0.266	6.831	4.430
RC	28.13	0.033	1.167	0.149
RCD	16.35	0.025	0.218	0.229

Table 2 contains input signal quality indicators for different snubber configurations. It can be seen that the RCD configuration has the best parameters for almost all indicators. $T_{s2\%}$ refers to the time after which the signal reaches the ±2% path of the nominal value. The rise time refers to the time taken by input signal to change from 10% of nominal value to 90% of nominal value. Fall time refers to the time taken by input signal to change from 90% of nominal value to 10% of nominal value respectively.

5. EXPERIMENTAL TEST RESULTS

Experimental tests were obtained for DC\DC converter (Fig. 7). As a power devices SiC MOSFET transistors (C2M0080120D) [6] and SiC shottky diodes (C4D10120A) [7] were used. PWM input signal was measured using TEKTRONIX TPS2024B oscilloscope with Tektronix P5122 voltage probe. The switching frequency was set to 50kHz. To generate PWM signal dSpace DS1104 R&D controller board was used.
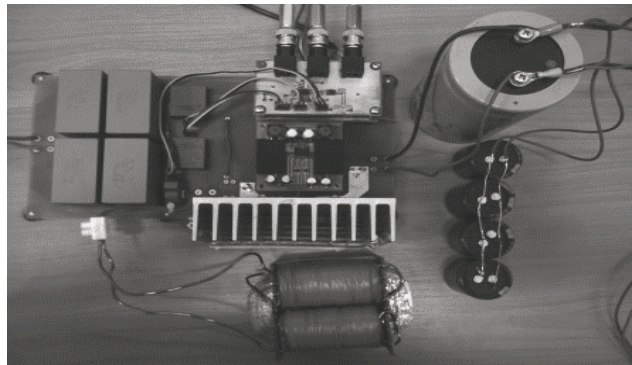

Fig. 7. DC/DC converter

Based on simulation results snubber topology with the best properties was chosen for experimental tests. Voltage overshoot is about 20V. The use of snubber improves the quality of the input signal. Waveform coincides with the simulation results.
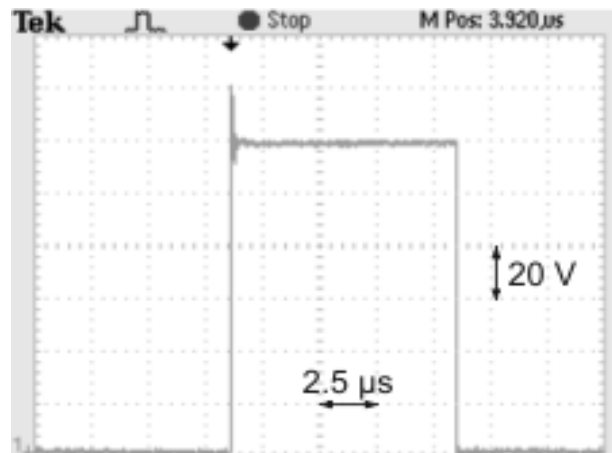

Fig. 8. DC\DC converter input signal with RCD snubber

6. CONCLUSION

It was found that using of snubber circuit improves the input signal shape, reduces voltage overshoots and oscillations. Simulation tests show that RC and RCD snubber circuit reduces input signal oscillations. However RC configuration has a longer fall time and dissipates more energy in every cycle than the RCD configuration. The use of capacitor based snubber does not produce the correct rectangular shape of the input signal. Because of this it is not suitable for this application. RCD configuration is the best option for use in this application.

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