Improvements of High-voltage Trapezoidal Waveform Edge-rounding Circuit

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***Abstract*—This paper introduces a solution to a design problem caused by necessity of electromagnetic noise reduction in simple close-range wireless command and control systems, including Radio-frequency identification (RFID) systems. Trade-off between simplicity of data transmission, detection and decoding on one side vs. presence of high frequency harmonics in transmitted signals on the other makes some designers choose approach in which trapezoidal waveforms are used instead of rectangular ones. Moreover, edges of trapezoidal waveforms are additionally rounded to further limit presence of higher harmonics and thus to comply to EMI regulations and requirements. The paper proposes a solution based on a reimplementation of a high-voltage structure already proposed by the author, but implemented with use of different semiconductor technology process. Utilization of this new process and devices available in this technology makes possible significant increase of the circuit operation quality.**

***Index Terms*—CMOS integrated circuits, high-voltage techniques, wireless communications, current-mode circuits, RFID tags, harmonic distortion, electromagnetic compatibility.**

I. Introduction

RADIO-frequency identification (RFID) based and similar systems have become very popular means of very close range signaling and controlling systems. One of problems with wireless data transmission is trade-off between simplicity of signal generation in transmitters, its reception and interpretation in receivers vs. generation of electromagnetic noise due to presence of high frequency harmonics in the signal waveforms fed to antenna and transmitted into surrounding environment.

Trapezoidal waveforms are sometimes used in such applications [1]. Such binary-looking waveforms are simply decoded back to their original form and meaning. However, one problem related to utilization of trapezoidal waveforms still remains. Wireless transmission of these waveforms causes electromagnetic noise, as bandwidth of such waveforms is significantly higher than in case of sine or similar waveforms [2, 3]. Higher bandwidth of trapezoidal waveforms is related mainly to parts (moments) of signal, in which the waveforms reach and leave their minimum and maximum levels.

Such properties may lead to problems with meeting electromagnetic compatibility (EMC) requirements for wireless equipment. Thus, the applied trapezoidal waveforms should be reshaped [4, 5] for lowering their bandwidth, before they are used for wireless transmission. Precisely, the extremes of these waveforms, that is parts close to the minimum and maximum waveform voltages, should be rounded.

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Such a process is sometime called waveform or signal edge-rounding or bandwidth limitation. Edge-rounded trapezoidal waveforms can still be simply decoded, while their bandwidth is significantly limited [3].

The paper presents reimplementation of the high-voltage edge-rounding circuit that offers superior operation quality as compared to its predecessors.

Section II of the paper presents the first, low-voltage edge-rounding circuit that uses the rule of operation finally adopted in the reimplemented circuit.

Section III presents the original high-voltage version of the edge-rounding circuitry based on a modified implementation of the same rule of operation. This circuitry has been implemented with use of a 0.8 μm SOI process.

Section IV presents the new reimplemented version of the high-voltage edge-rounding circuitry and improvements of its edge-rounding capabilities. This new operation quality is related to capabilities of a high-voltage AMS 0.35 μm process, used for the presented circuit remake.

II. Low-voltage Edge-rounding Circuits

Personal expertise of the author, gained mainly during projects focused on design of commercially available integrated circuits and through a following research [6, 7] points at specific requirements for such circuits. Some approaches to a rounding process require both keeping constant waveform slew-rate in middle section of the waveforms (e.g. 10-90 % or 20-80 % of voltage range) and rounding the waveform extremes so as to obtain required bandwidth limitation.

Fulfilling this kind of requirements for signal shape may be not wholly straightforward. First attempts of solving this problem, undertaken by the author, were low-voltage circuits based mostly on low-voltage operational amplifiers and, sometimes, current mirrors [6, 7]. Fig. 1 and Fig. 2 show structures intended to cope with reshaping of trapezoidal

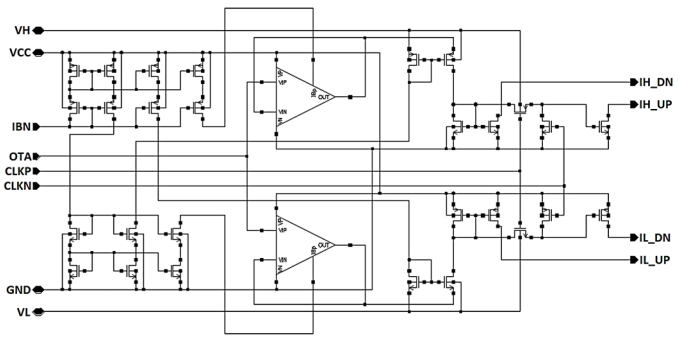

Fig. 1. Low-voltage edge-rounding circuitry that combines trapezoidal waveform generator with rounding circuitry.

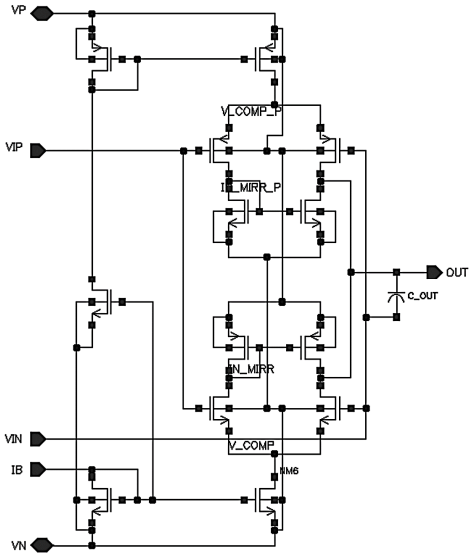

Fig. 2. Low-voltage edge-rounding circuit that uses already formed trapezoidal waveforms as its input signal and only rounds its edges.

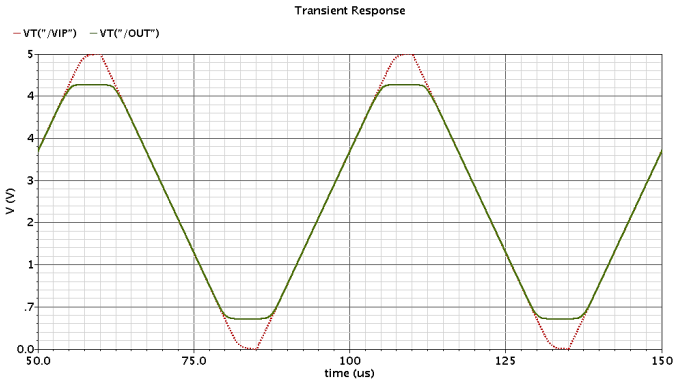

Fig. 3. Input and output waveforms of the circuit presented in Fig. 2.

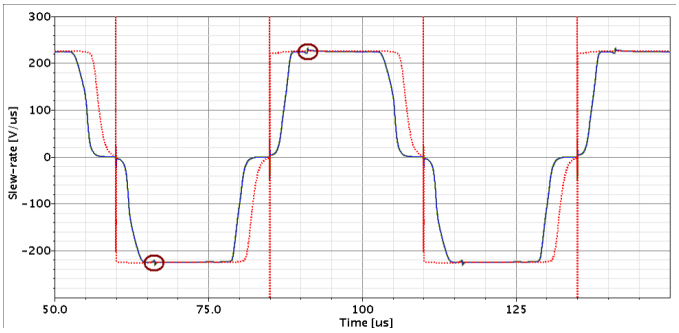

Fig. 4. Slew-rate curves of input and output waveforms of the circuit presented in Fig. 2.

waveforms at their voltage-range extremes. Both these solutions are focused on the highest possible signal-path shortening. The circuit presented in Fig. 1 combines a trapezoidal waveform generator with the edge-rounding circuitry, while the circuit in Fig. 2 rounds edges of already formed trapezoidal waveforms provided to its input.

Both these structures work, but with some speed or quality limitations. In case of the circuit presented in Fig. 1, operation speed and rounding strength are trade-offs. This circuitry rounds edges of the generated trapezoidal waveform by modifying current flow to the output capacitor, which forms a voltage signal proportional to a charge amount it accumulates. This circuit possesses a set of current-mode outputs that are connected to the output side of the accompanying trapezoidal waveform generator (not shown), so as to modify amount of current that charges/discharges the capacitor present at the output of this waveform generator. In an ideal case, the current flow to/from the output capacitance should gradually and smoothly vanish when the output waveform reaches its minimum and maximum voltages. However, due to the circuit structure it is necessary to leave some current flow ability/action when waveform voltage reaches its extremes, to speed up circuit operation in moments when the output waveform voltage starts to leave its extreme levels. Fully turned-off transistors of the current-stealing circuitry would need some extra time to turn on and bias to start their action.

The circuit of Fig. 2 consists of two connected 1-stage OPAMPs and its operation requires changing operating states of some transistors inside these OPAMPs. This behavior both limits operation speed and generates small distortions of the output signal. These distortions may be not easily observed in the output waveform itself (Fig. 3), but they are noticeable in slew-rate of this waveform (that is, in its derivative), as presented in Fig. 4.

Introductory works on waveform edge-rounding circuits suggested direction of following works. Above all, the signal-path of such circuits should be kept as short as possible [7]. Keeping the signal path short suggests, or even enforces, utilization of structures having most of their circuitry placed outside their signal-paths. Such a circuitry does not significantly limit the output waveform parameters such as its frequency or shape details, even though its internal structure can be fairly complex. Moreover, most of such auxiliary circuitry can work in DC conditions, which simplifies its design process.

The circuitry presented in Fig. 5 [7] shows such a structure for low-voltage applications. This circuitry is based on OPAMPs and a non-linear diode-resistor voltage divider. The input signal is a trapezoidal waveform of its slew-rate equal to the one required at the circuit output, and preferably with the highest possible voltage-range (even rail-to-rail, if possible in particular applications).

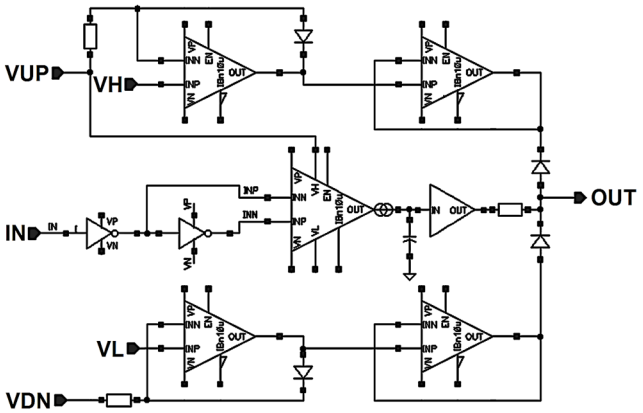

Fig. 5. Low-voltage edge-rounding circuitry with an extremely short signal processing path.

Other inputs of this circuit are bias voltages: VDN and VUP that are equal to minimum and maximum voltages of the input waveform. It can be seen, that feeding the input with rail-to-rail input waveforms simplifies this circuitry, as these bias inputs can be directly connected to ground and supply nodes. HL and HV inputs define lower and upper voltage extremes of the required output edge-rounded trapezoidal waveform.

The signal path is very short in this circuit. The input signal is provided to the non-linear diode-resistor voltage divider. This divider consists of two diodes and one resistor. This resistor is the only component that lies between the input and output nodes of this edge-rounding circuitry. This means that the output signal is a product of a non-linear voltage division process.

The divider diodes are connected between the output node and internal nodes that provide auxiliary bias voltages, as presented in Fig. 5. Way the output voltage-divider diodes are connected makes them remain in off state for middle part of the input signal voltage-range. Thus, if the output node is connected to a high-impedance capacitive-input voltage follower, practically no current flows through the divider resistor, which keeps the input and output node voltages equal.

When the input signal leaves the middle part of its voltage-range, one of the diodes starts conducting current and forms a highly non-linear voltage divider with the output resistor. It can be observed, that for proper operation of the circuitry, the voltage-range of the input waveform needs to be larger than the required voltage range of the edge-rounded output waveform.

Moreover, this edge-rounding process is the more efficient the higher voltage differences VL-VDN and VUP-VH are. In fact, what this non-linear voltage divider does is squeeze lower (VDN and close above) and upper (VUP and close below) voltage ranges of the input waveform so that the output waveform range is limited to a <VL; HV> voltage-range.

Because the performed voltage division operation is a highly non-linear one (diodes vs. resistor), the final effect of this input voltage "squeezing" is a rounded/bended shape of the output waveform in parts close to its voltage range extremes. Identical shapes (and slew-rates) of the input and output waveforms are retained for middle parts of their voltage ranges. The only side effect of such an operation rule is inability of obtaining properly edge-rounded output waveforms that would have voltage-range equal or similar to the full ground-to-supply voltage span between the power rails. This can be amended by limited (e.g. no more than twofold) amplification of the output waveforms.

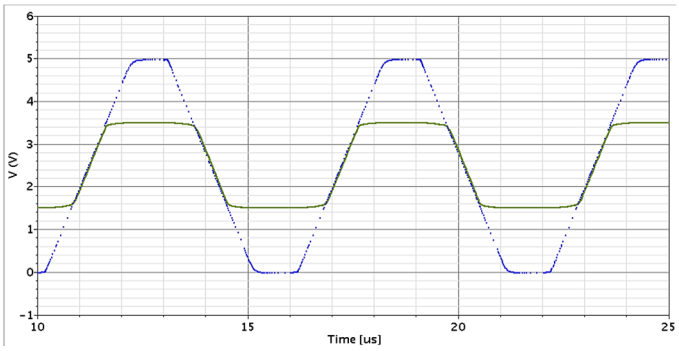

Fig. 6. Input and output waveforms of the circuit presented in Fig. 2.

Most of processing in this circuit happens outside the signal path and is focused on producing the correct bias voltages, to which the internal nodes of the output divider diodes are connected. Proper voltage values at these nodes are essential for obtaining the output waveforms precisely limited to the externally enforced <VL; VH> voltage range. If both one of the diodes and the resistor of the non-linear divider are conducting, same currents flow through these series connected devices.

This way of operation is used for producing the bias voltages for the internal nodes of the divider diodes. The VL-VDN and VUP-VH voltage differences are known, because all these voltages are provided to the circuit inputs in order to define operation details of the edge-rounding circuitry. Moreover, when the input and output waveforms reach their extremes, the current flow through the output voltage-divider devices can be easily derived, because only the divider resistor is present between the input and output nodes of the circuit.

Input side OPAMP-based circuits of the structure presented in Fig. 5 simply recreate these current flows by providing VL and VDN or VUP and VH voltages to opposite terminals of auxiliary resistors identical to the one used in the output voltage-divider. Generated currents flow through closed feedback-loops of the both OPAMPs. Properly directed auxiliary diodes identical to those in the voltage-divider are placed in feedback-loops of these OPAMPs.

Because the same current flows through both the voltage divider resistor and its diodes (one diode at a time), flow of the recreated current through each of the auxiliary diodes causes voltage drops identical to those present on the output voltage-divider diodes, precisely when both the input and output waveforms reach their extremes. The auxiliary bias voltages obtained this way are buffered by typical OPAMPs and provided to the internal nodes of the output voltage-divider diodes. When the input waveform reach its extremes, the operation of the output voltage-divider results in a voltage drop on its currently conducting diode that precisely sets the output waveform equal to the desired VL or VH value.

Fig. 6 shows exemplary input and output waveforms of the circuit presented in Fig. 5, while Fig. 7 shows slew-rates of these waveforms. It can be observed that the output waveform slew-rate curve follows the input waveform slew-rate as long as both of the output voltage-divider diodes are off and do not conduct any noticeable currents.

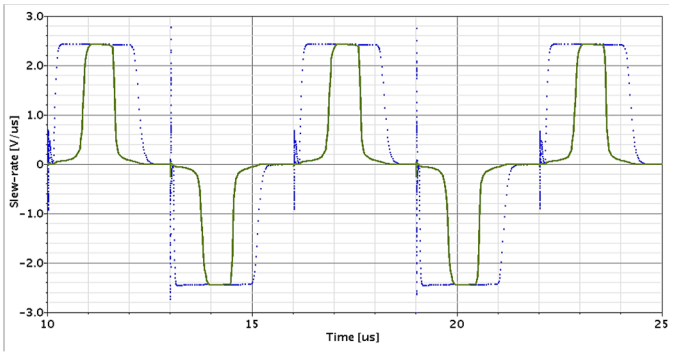

Fig. 7. Slew-rate curves of input and output waveforms of the circuit presented in Fig. 2.

III. High-voltage Adaptation of Low-voltage Edge-rounding Circuit

The circuit shown in Fig. 5 is of course a low-voltage circuit that provides low-voltage edge-rounded output waveforms. However, this structure could be used for high-voltage edge-rounded waveform generation applications by direct adaptation of its structure. Unfortunately, such an approach requires design of high-voltage OPAMPs. This is a task generally more complex than design of low-voltage OPAMPs. Especially, if input stages of such OPAMPs also need to work in a high-voltage domain.

The already presented low-voltage circuit structure could be directly used for high-voltage applications, if only the output voltage waveform would be amplified and its offset adjusted. It is possible to perform such operations, but this approach has important drawbacks. If a low-voltage output waveform is to be amplified, it means it should have lower slew-rate, as the amplification process will increase the final slew-rate value. Moreover, due to the waveform amplification process, noise also gets shifted to higher frequencies. This phenomenon contradicts main goal of the presented edge-rounding circuitry, which is limitation of high frequency harmonics of the edge-rounded output waveforms. The low-voltage edge-rounded output waveforms produced by the circuit presented in Fig. 5 have their voltage-range limited even in comparison to ground-to-supply voltage span of this circuit. Thus, adaptation of such output waveforms to high-voltage domain applications may mean significant factors of amplification, e.g. 5 or 10 times.

Another approach should be attempted for obtaining the edge-rounding effect in high-voltage systems. During works on high-voltage integrated systems, author has quite often been using a current-mode of signal processing. Some high-voltage semiconductor processes provide versions of low-voltage devices (e.g. MOS transistors) with isolated substrates that can float in voltage space, even ranging between ground and supply voltage levels. This is a typical asset of Silicon-on-Insulator (SOI) technologies. Currents in high-voltage systems implemented with use of such technologies can be processed by precise low-voltage devices (mainly transistors) and propagated with use of less precise high-voltage devices (e.g. acting as cascode and buffer transistors in high precision current mirrors). Higher precision of low-voltage transistors is here understood as their superior layout matchability properties, which means better and more predictable operation of fabricated circuits.

A basal version of the high-voltage circuit devised with the current-mode approach to signal processing [8, 9] is presented in Fig. 8. The circuit consists of two voltage-current converters devised and proposed by the author [10, 11], two high-voltage current-mirrors, a double high-voltage follower with high-resistance inputs (or two single followers of such kind). The author proposed such a follower [12] as it was necessary for application in various kinds of current-mode high-voltage function blocks [11]. The proposed voltage-follower was invented during design works related to a commercially focused contract and it was patented by a commercial company [13].

The general idea of the circuit operation is similar to the one used in its already presented low-voltage predecessor. Inputs of this circuit are: a trapezoidal waveform of possibly wide voltage-range; bias voltages VDN and VUP that are equal to the minimum and maximum (extreme) voltages of the input trapezoidal waveform; bias voltages VL and VH that define the voltage range of the output edge-rounded waveform.

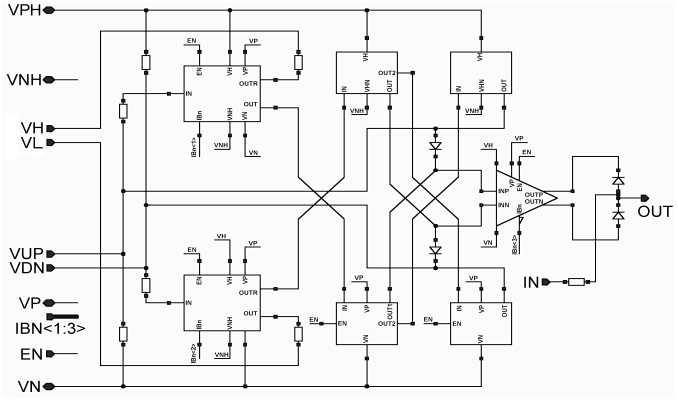

Fig. 8. High-voltage edge-rounding circuitry that uses operation principle derived from one used in the low-voltage circuit presented in Fig. 5.

Operation of the non-linear diode-resistor voltage divider and its role in this circuit is also identical as in its low-voltage counterpart presented in Fig. 5. Voltage differences VL-VDN and VUP-VH are converted into currents identical to those flowing through the output diode-resistor voltage-divider, when the input and output waveforms reach their extremes. To achieve this goal, resistors identical to the one in the output voltage-divider are used along with specially devised voltage-current converters based on regulated-cascode current-mirrors [10, 11]. Obtained currents are propagated in the high-voltage circuitry with use of four high-voltage current-mirrors, then these currents flow through two auxiliary diodes identical to those in the output voltage-divider.

Internal terminals of these diodes are connected to the buffered VL and VH bias voltages so that currents flowing through these diodes set their other terminal voltages to levels that are buffered [12] and provided to internal terminals of the diodes in the output voltage-divider. To ensure flow of proper currents through these auxiliary diodes, their driving currents are both pushed into and pulled from each of these diodes. Interconnections within the circuitry are able to cope with resulting small non-equilibrium currents that occur as a result of such a push-pull current control scenario.

Owing to application of the presented high-voltage edge-rounding circuitry, there is no need for significant amplification of the output high-voltage edge-rounded waveform. Highest voltage amplification that was required in such a kind of circuit implemented by the author was equal two. Such a small amplification factor causes only limited shift of noise in the frequency domain. Fig. 9 shows the input, internal and output waveforms obtained for the basal version of the high-voltage circuitry. Fig. 9 includes a waveform of an optional output signal amplifier, that can be used to increase voltage-range of the final output waveform. Fig. 10 shows slew-rates (waveform derivatives) of the waveforms presented in Fig. 9.

The simulation results presented in this section have been made for the circuit implemented with use of 0.8 μm SOI high-voltage semiconductor process.

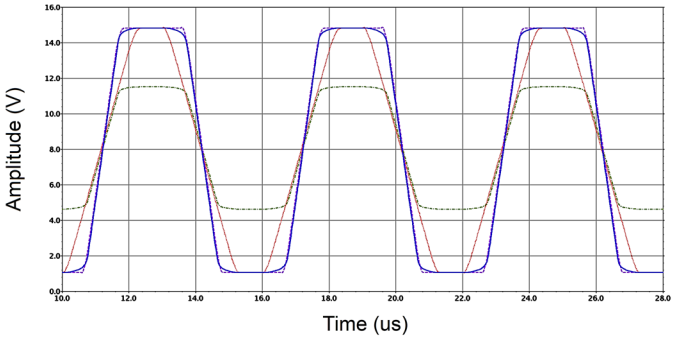

Fig. 9. Input and output waveforms obtained for first version of the circuitry, including waveform of optional output signal amplifier, that can be used to increase voltage-range of the final output waveform.

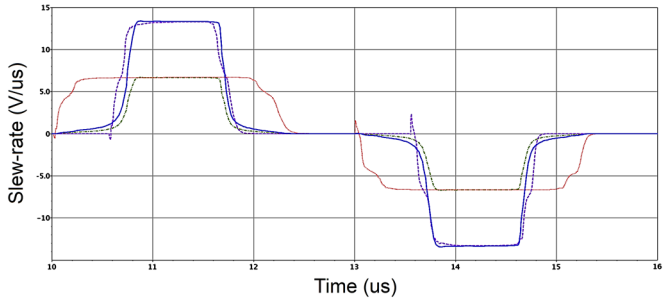

Fig. 10. Slew-rates (derivatives) of the waveforms presented in Fig. 9.

IV. New Implementation of High-voltage Edge-rounding Circuit and Its Functionality Enhancements

An important asset of the already presented high-voltage circuit is a possibility of largely increased shaping of its output waveforms. There are high-voltage drops that can safely (for the circuit operation) occur between nodes to which the auxiliary and the output voltage-divider diodes are connected. Thus, depth or strength of the edge-rounding process can be intensified or adjusted by application of several series-connected diode-like devices instead of a single one, if only proper devices are present in the technology process selected for the circuit implementation. In case of originally used high-voltage SOI process, some diode-connected high-voltage transistors were acting as diodes. Due to limitations of the original process, it was difficult to precisely adjust shape of the non-linearly voltage-divided output waveforms. Application of series-connected diode-acting devices posed significant process-related difficulties in the original semiconductor process and maximum number of such series connected devices was limited to just a few (the precise number has been related to the supply voltage value).

The circuit presented in Fig. 8 has been reimplemented and resimulated with application of the AMS 0.35 µm high-voltage CMOS process that offers some useful functionality extensions. Due to presence of extensive set of wells and tubs, this process offers so-called isolated low-voltage MOS transistors. Thus, it is possible to use low-voltage devices placed in isolated substrate tubs and floating inside extended ground-to-supply voltage-range. Among others, it is possible to power low-voltage PMOS transistor based circuitry from high-voltage supply node and auxiliary virtual ground devices.

AMS company presents these isolated low-voltage transistors as well suited for application of a floating digital logic circuitry [14]. However, several papers and dissertations state, that these isolated low-voltage MOS transistors can also be successfully used for analog applications. Several MOS low-voltage isolated devices have been reported to work in high-voltage current mirrors [15, 16], including current sourcing and sinking structures [17], high-voltage OPAMPs [15, 16] and level shifters [18].

Such design possibilities make this semiconductor process more akin to typical high-voltage SOI processes. Presented process extensions have enabled reimplementation of the circuit shown in Fig. 8 and originally based on a typical high-voltage SOI process. Simulations of the reimplemented circuit have shown that most of diodes and diode-connected transistors of the selected AMS process are inadequate for intended high-voltage operation. Luckily, some special diode-based safety devices of the AMS process can safely operate in the voltage-divider of the high-voltage edge-rounding circuitry. It was found that due to shapes of I-V characteristics of these devices it is possible to obtain required quality of the output voltage-divider operation. Moreover, it is possible to connect up to over 20 of these diode-based devices in series and (in spite of large voltage drops on such multi-diode structures) still have fully working circuitry with all voltage levels on the auxiliary and the output diode devices well within acceptable ground-to-supply voltage range. Thus, it is rather an area occupied by the utilized diodes what practically limits strength of the edge-rounding process.

Fig. 11 presents the input and edge-rounded output waveforms, obtained for different numbers of series-connected diodes in the reimplemented edge-rounding circuit. Fig. 12 presents a close-up of the edge-rounded output waveforms from Fig. 11, while Fig. 13 presents slew-rates of the edge-rounded waveforms from Fig. 12. It can be observed how precise tuning of the rounding action is possible with use of the reimplemented circuit. If even more profound rounding of the input waveform is needed or the multi-diode device consumes too much chip area, it is possible to reasonably limit voltage range of the output waveform and amplify it after it gets edge-rounded. Amplification process will both increase the voltage-range and the rounding effect of the output waveform.

Fig. 14 presents further close-up of the output waveform upper part obtained for different numbers of the series-connected diodes. Fig. 15 presents details of slew-rate values of the waveforms presented in Fig.14. Frequency domain comparison is presented in Fig. 16 that shows DFTs for the input trapezoidal waveform and for the output edge-rounded waveforms for selected numbers of series-connected rounding diodes. Fig. 17 presents descend of THD values for ascending number of series-connected diodes in the edge-rounding voltage divider of the circuit. The THD value for a diode number equal zero represents a reference waveform identical to the circuit input waveform in sense of its time delay and rising/falling slew-rates, but with voltage same as in the output waveforms of the edge-rounding circuit.

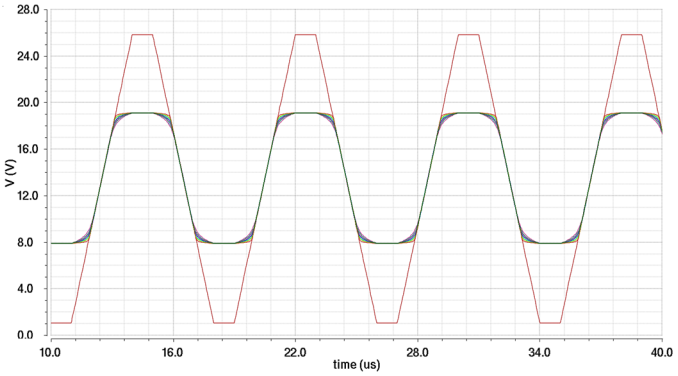

Fig. 11. Input waveform and edge-rounded output waveforms of the re-implemented circuit of Fig. 8, obtained for 3,5,7,9, 11,13,15,17,19,21 series-connected diodes.

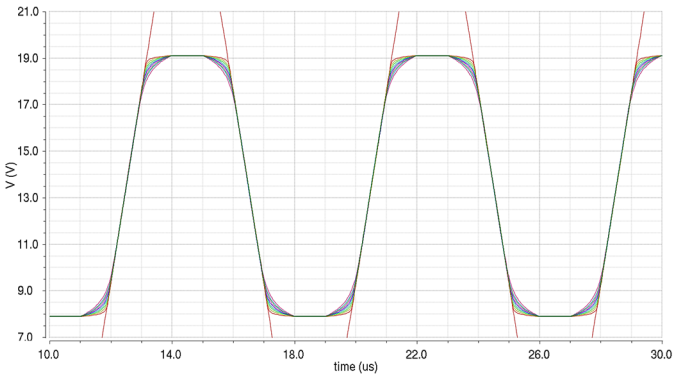

Fig. 12. Close-up view of edge-rounded output waveforms presented in Fig. 11.

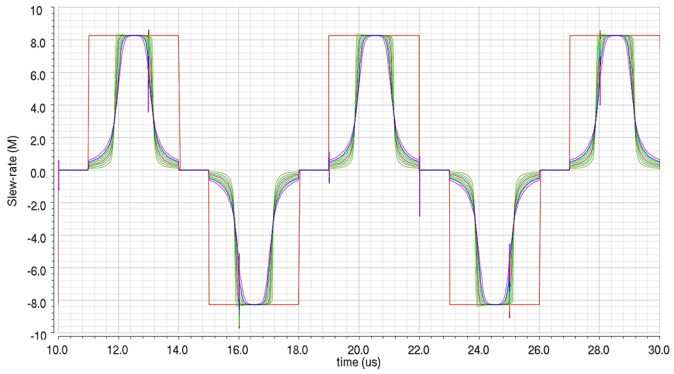

Fig. 13. Slew-rates of edge-rounded waveforms from Fig. 12.

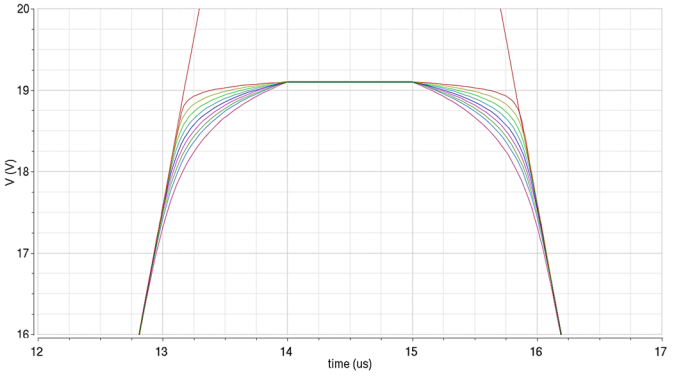

Fig. 14. Further close-up view of output waveform upper part obtained for 3,5,7,9, 11,13,15,17,19,21 series-connected diodes.

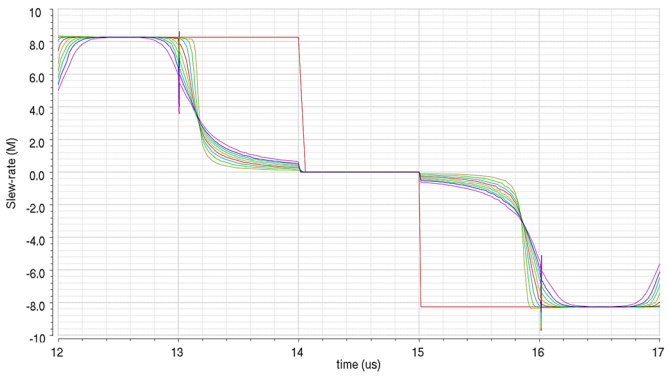

Fig. 15. Slew-rate curve of Fig. 15 waveforms.

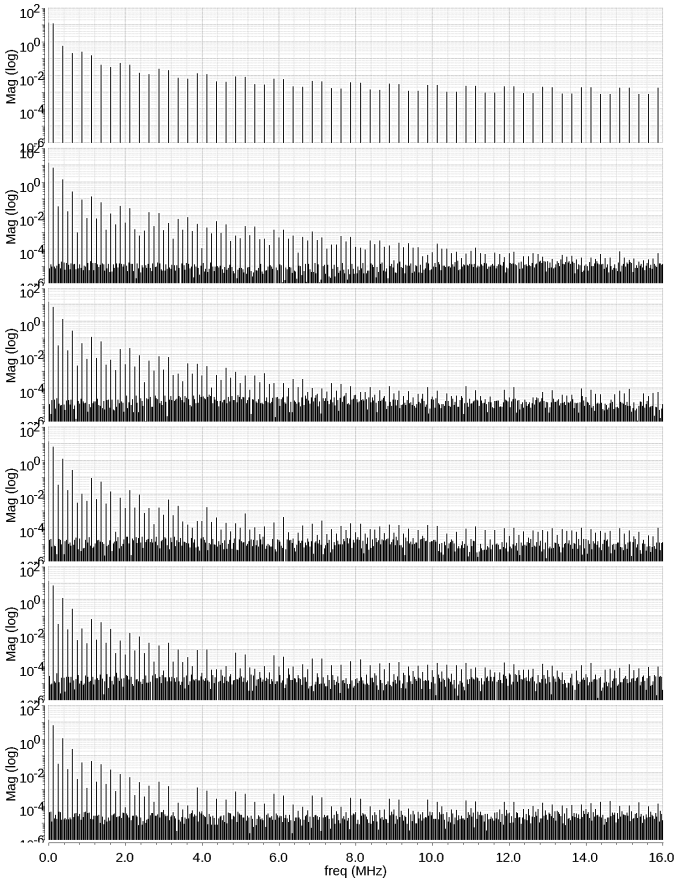

Fig. 16. DFT prepared for (top to bottom))input trapezoidal waveform and output edge-rounded waveforms for circuits with 5, 9, 13, 17, 21 series-connected rounding diodes.

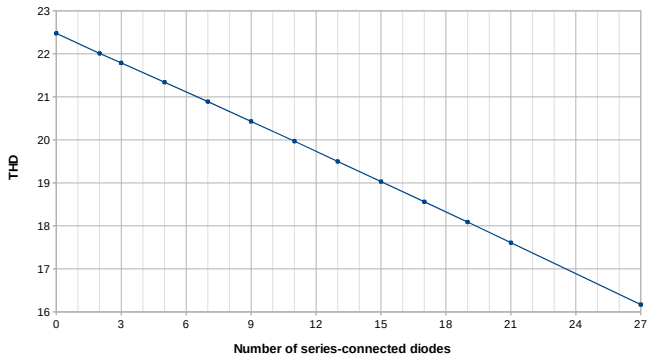

Fig. 17. THD values for a not rounded reference waveform (rounding diode number = 0) and the output edge-rounded waveforms for circuits with 2, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21 and 27 series-connected rounding diodes.

It can be seen that operation in the high-voltage domain gives much flexibility in shaping of the edge-rounded output waveforms of the reimplemented circuitry. It might be argued that the low-voltage circuit presented in Fig. 5 might provide similar edge-rounding properties, if reimplemented in the AMS high-voltage process. Unfortunately, because of much lower voltage-ranges and, thus, much lower acceptable numbers of series-connected diodes, similar flexibility and adaptability needed for detailed shaping of the output waveform is simply impossible in case of low-voltage circuits.

The reimplemented circuit (just like the original one) has two supply voltages. One for supplying low-voltage circuitry (VP) and one for high-voltage part of the circuit (VH). Most of the circuitry is based on current mirrors and other current-processing modules. Thus, a current consumption of the circuit is quite precisely defined by its input bias current flow. A simulated current flow through the low-level supply terminal is about 70 μA, while a current flow through the high-voltage supply terminal VH is equal about 1 mA, for the input bias currents equal 10 μA. Due to the mentioned internal structure, the overall current consumption of the circuit remains weakly related to changes of the supply voltages. Moreover, because of the generally current-driven operation of the circuit, the current consumption of its original SOI based version is quite similar, if identical bias currents are used.

The original circuit implemented with use of the 0.8 μm SOI process uses MOS devices able to operate with drain-source voltages up to 45 V and gate-source voltages up to 5.5 V. The circuit has been designed to work with supply voltages ranging from 16 V to 27 V, as it has been expected to be used in automotive systems powered with 24 V supply voltage. The reimplemented circuit uses devices able to work with drain-source voltages up to 25 V and 50 V and gate-source voltages up to 3.6 V and 5.5 V. Generally, the reimplemented circuit can work with its supply voltages similar to the ones of the original circuit. Though, application of lower voltage levels of the high-voltage VH supply tends to simplify design of ESD devices used inside the reimplemented circuit.

Conducted simulations show that reimplementation of the high-voltage edge-rounding circuit is able to properly operate for the input waveform frequencies above 1 MHz. Such a limit is acceptable for typical 125 kHz RFID systems and similar wireless close-range communication systems. Comparable frequency limits have been also found for the original SOI based version of the high-voltage edge-rounding circuit.

V. Conclusion

The paper has presented the reimplementation of the high-voltage edge-rounding circuitry that uses of a modern high-voltage CMOS process instead of the original high-voltage SOI process. First of all, application of the AMS high-voltage CMOS process with extended capabilities makes such reimplementation possible, at all. Moreover, capabilities of the process used for the circuit reimplementation enable replacement of the originally used high-voltage devices with the diode-based safety devices. Due to the transfer characteristics of these devices, it is possible to series connect multiple instances, and thus obtain much strengthened edge-rounding effects, while keeping the whole circuit fully operational.

Extended capabilities of the reimplemented circuit, accompanied by a straightforward operation inherited from the preceding circuit (the signal-path limited to a single resistor) make this circuit a sensible solution to a problem of a trapezoidal waveform edge-rounding and of a waveform bandwidth limitation, in general. Operation quality of this circuit makes it well fitted to bandwidth limitation of waveforms used (radiated and received) in some of close-range wireless communication and control systems, like these operating at 125 kHz base frequency.

References

[1] Jean-Michel Redouté and Michiel Steyaert, An EMI Resisting LIN Driver in 0.35-micron High-Voltage CMOS, IEEE Journal of Solid-State Circuits, vol. 42, no. 7, pp. 1574-1582, 2007.

[2] H. Funato, T. Mori, T. Igarashi, S. Ogasawara, F. Okazaki, and Y. Hirota, "Optimization of Switching Transient Waveform to Reduce Harmonics in Selective Frequency Bands," IEEJ J. Industry Applications, vol. 2, no. 3, pp. 161-169, 2013.

[3] S. Ogasawara, T. Igarashi, H. Funato, M. Hara, Optimization of switching transient waveform to reduce EMI noise in a selective frequency band," IEEE Energy Conversion Congress and Exposition, San Jose, CA, USA, 20-24 Sept. 2009.

[4] M. Kachare. J. Ramirez-Angulo, R. Gonzalez Carvajal, A J. Lopez-Marlin, "New Low-Voltage Fully Programmable CMOS Triangular /Trapezoidal Function Generator Circuit," IEEE Transactions on Circuits and Systems: regular papers. Vol. 52, No. 10, October 2005.

[5] Atichaya Klungtong et al., "Current-Controllable Square/Triangular Waveform Generators using Operational Transconductance Amplifier and Uniform Distributed RC," Proceedings of International Conference on Circuits, System and Simulation (ICCSS 2011), pp. 207-211, 2011.

[6] M. Jankowski, "Adjustable output voltage-range trapezoidal waveform generator with harmonics-reduction functionality," in Proceedings of the 9th International Conference TCSET'2008, Modern Problems of Radio Engineering, Telecommunications and Computer Science, Lviv-Slavsko, Ukraine, Feb. 2008, pp. 19-23.

[7] M. Jankowski, G. Jablonski, "Adjustable Generator of Edge-Rounded Trapezoidal Waveforms," International Journal of Electronics and Telecommunications, 2012, Volume 58, Issue 3, pp. 213-218, DOI: 10.2478/v10177-012-0029-z.

[8] M. Jankowski, A. Napieralski, „High-voltage Edge-rounded Trapezoidal Waveform Generators," NANOTECH - Advanced Materials & Applications. Washington, DC 2015, pp. 258-261.

[9] M. Jankowski, A. Napieralski, „High-voltage Trapezoidal Waveform Generator with Edge-rounding Functionality Implementations," MIXDES -Mixed Design of Integrated Circuits and Systems. Poland, Lublin, 19-21.06.2014, pp. 224-229.

[10] M. Jankowski, A. Napieralski, "Low-to-High Voltage Range Analog Converters based on Current-mode Signal Processing," 12th International Conference "The Experience of Designing and Application of CAD Systems in Microelectronics (CADSM), Lviv-Polyana, Ukraine, 19-23.02.2013, pp. 416-418.

[11] M. Jankowski, A. Napieralski, "Current-mode signal processing implementation in HV SoI integrated systems," MICROELECTRONICS JOURNAL, 2014, vol. 45, no. 7, pp. 946-959.

[12] M. Jankowski, A. Napieralski, "High-Voltage high input impedance unity-gain voltage buffer," MICROELECTRONICS JOURNAL, 2013, vol. 44, no. 7, pp. 576-585.

[13] M. Jankowski (author), Automatix spolka z o.o. (right owner), "Voltage Buffer Circuit," in Polish: "Układ bufora napięciowego," patent no WYN: (11)212837, issued by Polish Patent Office, granted: 19 June 2012, published: 22 June 2012.

[14] Rainer Minixhofer – Senior Manager R&D austriamicrosystems AG, "Semiconductor Manufacturing in Austria," Topical Workshop on Electronics for Particle Physics, Vienna, Sept. 26th, 2011.

[15] Jing Ning, “Design of An Integrated High Voltage Controller in CMOS-Technology for Tunable Multiport Microwave Devices,” Ph.D. dissertation, Elektro- und Informationstechnik Institut fur Datentechnik der Technischen Universit¨at Darmstadt, 2016.

[16] Noppasit Laotaveerungrueng, “A High-Voltage, High-Current Multi-Channel Arbitrary Waveform Generator ASIC for Neural Interface and MEMS Applications,” Submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, Department of Electrical Engineering and Computer Science, Case Western Reserve University, 2011.

[17] N. Dommel ; Y. T. Wong ; T. Lehmann ; P. Byrnes-Preston ; N. H. Lovell; G. J. Suaning2006 International Conference of the IEEE Engineering in Medicine and Biology Society, New York, NY, USA, 30 Aug.-3 Sept. 2006, DOI: 10.1109/IEMBS.2006.259605.

[18] Bo Wang ; Marco Riva ; Jason D. Bakos ; Antonello Monti, “Integrated Circuit Implementation for a GaN HFET Driver Circuit,” IEEE Transactions on Industry Applications, Volume: 46, Issue: 5 , Sept.-Oct. 2010, pp. 2056 – 2067, DOI: 10.1109/TIA.2010.2057499.

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