

DIRECT COMPARISON OF ANALOGUE AND DIGITAL FGPA-BASED APPROACHES TO SYNCHRONOUS DETECTION

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Abstract

This paper deals with a comparison between digital and analogue implementation of a synchronous detection algorithm. The commonly used implementation methods of synchronous detection are presented in the paper. The paper describes FPGA-based digital and analogue hardware approaches, focusing on the digital design. The characteristics of used analogue-to-digital converters are measured. Both proposed approaches are directly compared in terms of sensitivity and long-term stability. The achieved results, along with identified limitations and proposed improvements are widely discussed.

Keywords: synchronous detection, lock-in amplifier, digital signal processing, FPGA, measurement of impedance.

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1. Introduction

The synchronous detection (SD) is a technique that enables to extract small signals buried in the noise floor, or decompose them into real and imaginary parts depending on the reference signal [1]. The instruments implementing SD are well known as lock-in amplifiers (LIA). In many measurement systems, it is very useful to modulate an effective signal into a band with a lower noise level or a lower disturbing signal level [2–6]. For example, the light source modulation in the case of a light barrier is used to suppress negative effects of the ambient light. A narrow-band-pass filter could then be used to extract only the carried frequency. Such a narrow filter design can be very complicated, which is why LIA is used. In other words, LIA provides back demodulation of a modulated signal to obtain the DC signal.

Performing vector-based voltage measurements is the next typical application of LIA. In the field of electrical impedance measurements (Ohm-law method) knowing the entire vector of a measured voltage or current in respect to the reference vector is a necessity. The demodulator used in LIA multiplies an input signal with a signal of the same frequency as the reference signal. Depending on phase of the multiplying signal (0 or 90 degrees), LIA generates an output proportional to either the real or imaginary part of the input signal.

There are two basic approaches to choosing a waveform of the multiplying signal. The first method uses a square waveform signal with an amplitude of peak-to-peak value of ± 1 . The multiplication with such a signal can easily be done by using an operational amplifier with an

additional analogue switch providing the amplifier gain change. If the analogue switch is open, the amplifier gain is set to 1, otherwise it is set to -1 . The input of the analogue switch can be controlled from e.g. a microprocessor.

Some producers provide circuits with two integrated operational amplifiers with separately adjustable gain and with an input to control switching the amplifiers' outputs (e.g. AD630). This kind of integrated circuit is suitable for implementing a method of synchronous detection using the squared wave multiplication. The main advantage of this method is its simple implementation and relatively small complexity of used parts. On the other hand, the frequency spectrum of a modulator with the squared wave multiplication is distorted by odd harmonic frequencies. This fact could be very negative in the field of precise measurement and may cause an additional error of output DC value estimation.

The second method uses the sinus waveform multiplication (see Fig. 1) which eliminates the modulator frequency spectrum distortion. Then, the output signals are expressed by the equations:

$$U_X = \frac{1}{2} U_S U_R \cos [(\omega_S - \omega_R)t + \theta_S - \theta_R] - \frac{1}{2} U_S U_R \cos [(\omega_S + \omega_R)t + \theta_S + \theta_R], \quad (1)$$

$$U_Y = \frac{1}{2} U_S U_R \sin [(\omega_S + \omega_R)t + \theta_S - \theta_R] + \frac{1}{2} U_S U_R \sin [(\omega_S - \omega_R)t + \theta_S - \theta_R], \quad (2)$$

where U_S is an input signal, U_R is a reference signal, ω_S , ω_R are natural frequencies of the signals, and θ_S , θ_R are phase shifts of the signals. Assuming $\omega_S = \omega_R$ and after filtration of the frequency $\omega_S + \omega_R$ using LPF1 and LPF2 we obtain the output signals:

$$U_X = \frac{1}{2} U_S U_R \cos [\theta_S - \theta_R], \quad (3)$$

$$U_Y = \frac{1}{2} U_S U_R \sin [\theta_S - \theta_R], \quad (4)$$

that indicates that the input signal U_S is decomposed into real and imaginary parts.

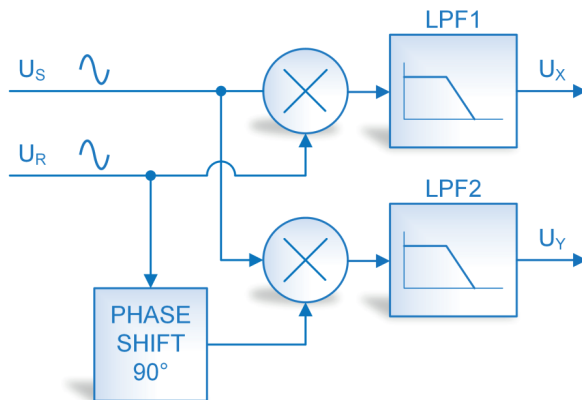


Fig. 1. A block diagram of sinus-based synchronous detection.

This improvement calls for higher demands to generate a sinus waveform signal. The mentioned methods can be implemented in the digital (FPGAs, microcontrollers) or analogue (operation amplifiers) form.

2. Digital test platform

The proposed algorithms and signal processing methods have been designed for implementation on a real digital platform. There are several similar implementations on other DSP platforms, like [7–9]. This paper is dedicated to the FPGA-based platform. The designed FPGA acquisition system is capable of a variety of signal processing tasks. The hardware is divided into two main parts. The control logic and communication interface are placed on an FPGA board, and analogue front-end parts – on a daughterboard, which is removable and can be easily changed. This part also contains the developed software blocks, like all-digital phase-locked loop (ADPLL) and LIA core. In addition, the firmware (FW) of software processor is introduced.

2.1. FPGA board

The core parts of digital subsystems are placed on a field-programmable gate array (FPGA) board. A block diagram is shown in Fig. 2a. To obtain an easy implementation of real-time parallel tasks and large scalability the FPGA architecture was chosen. An Altera Arria V GX device in the FBGA672 case provides a reasonable trade-off between functionality and price.

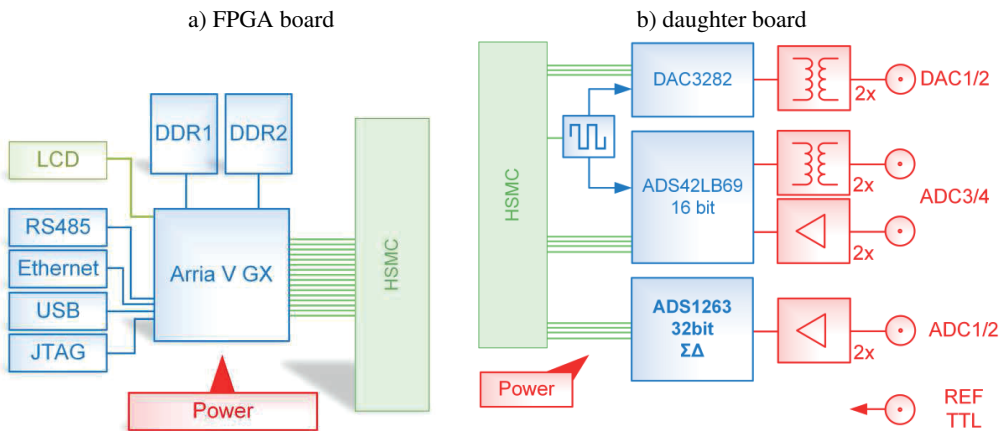


Fig. 2. A block diagram of of VHDL parts.

Two memory interfaces for DDR3, a large volume of internal RAM and high-speed GPIO interfaces are essential parts of such a design. In addition, the user is able to implement high-speed System-on-the-chip (SoC) systems using an Nios 2 Gen2 soft processor core from within this device family. The control between FPGA board and host/slave systems is ensured via several types of communication standards. The Ethernet 10/100 Mbit/s link is provided with an external TCP hard-wired stack from Wiznet. A W5500 chip provides up to 8 parallel full-featured TCP/UDP stacks. The internal medium-access-control (MAC) capability of Altera device is not used because of licensing policies. This solution provides a comparable data throughput and has to meet much less computation requirements to the host SoC inside the FPGA. A full-duplex isolated EIA485 interface is implemented for industrial standard communication via twisted-pair buses. For convenient PC-to-hardware (HW) communication, the FPGA board is equipped with a USB interface. The internal RAM of 8 Mbits could be expanded with two 64 MB DDR3 chips.

A High-Speed Mezzanine Card (HSMC) 160-pin connector is placed on the edge of the board to provide connection with the daughterboard. This interface consists of 19 differential gigabit links, 32 LVDS differential connections, 20 LVTTTL single general purpose pins and a power supply network.

An LCD character display and a JTAG connector can be used for debugging or simple visualization of results. The power circuits consist of a complex power supply unit for all FPGA systems, with a proper voltage ramping and powering sequence.

2.2. Analogue daughterboard

A block diagram of the designed analogue front-end board is shown in Fig. 2b. The board can be divided into three main parts. The first part is a high-speed digital-to-analogue converter, the second is a high-speed analogue-to-digital converter, and the last one is a low-speed precise analogue-to-digital converter. Only the low-speed precise ADC part will be described more in-depth in the following text because this hardware part was used in the comparison. The high-speed parts are intended for future high-speed application purposes. The interconnection with the board described in Section 2.1 is made with the mating type of the previously introduced HSMC connector. Proper voltage levels for all used parts are generated by the power supply directly on this board via the HSMC connector. In addition, the power input can be connected to a dedicated socket. The clock distribution and generation are provided by the Si5338 part, which could be configured for various clock voltage levels and frequency ranges.

The low-speed precise ADC part, which is used in the proposed algorithm and comparison implements the latest version of high resolution, high-performance ADS1263 sigma-delta converter with a 32-bit output data code and a sampling rate of up to 38.4 kSPs. The basic input voltage range is 5 Vpp. The input signal is passed via a precise voltage follower to preserve the signal. Both the theoretical and measured characteristics of this converter are described more in-depth in Section 2.3. An SPI bus is used for communication and control.

2.3. Analogue-to-Digital converter

An internal block diagram of the used converter can be found in [10]. For digital LIA purposes, only ADS1263 is used. The converter was tested in two types of connection. The first test was aimed at noise performance and ENOB (effective number of bits) determination, whereas the second one was aimed at determination of THD (total harmonic distortion), SNR (signal to noise ratio) and SFDR (spurious-free dynamic range). A Stanford Research DS360 was used as the signal source due to its low distortion feature. According to the specification given in [11], a sine waveform at 50 Hz frequency has the worst THD of -106 dB, while the typical THD value is better than -110 dB. Ground connections were made directly at the SMA connector input with a short adapter. Table 1 shows the complete results of testing. THD, SINAD, SNR values [12] were calculated directly inside MATLAB R2015b. Additional parameter values have been obtained from (5) and (6) below.

$$ENOB = \frac{SINAD - 1.76 + 20 \log \left(\frac{V_{FS}}{V_{IN}} \right)}{6.02}, \tag{5}$$

$$ENOB_{ADS} = \log_2 \frac{FSR}{V_{NRMS}}, \tag{6}$$

where V_{NRMS} is an input-referred noise level. $ENOB_{ADS}$ is calculated according to Eq. (8) in [10]. $ENOB_T$ is a theoretical value shown in Tab. 2 in [10]. No. of Samples is the volume of sampled data, f_{IN} is a frequency of the input signal, V_{FS} is a full-scale amplitude, V_{IN} is an input amplitude, FSR is a full-scale range and f_s is an actual sampling frequency.

Table 1. ADS1263 characteristics.

f_{IN} [Hz]	V [V _{pp}]	f_s [Hz]	No. of samples	THD	SINAD	ENOB	$ENOB_{ADS}$	$ENOB_T$
50	2.0	1200	4 K	-100.5	87.5	15.6	21.37	22.0
50	2.0	19200	4 K	-97.1	91.7	16.3	19.69	20.1
50	4.5	1200	4 K	-96.4	85.1	14.0	21.36	22.0
50	4.5	19200	4 K	-95.7	93.1	15.3	19.69	20.1
50	4.5	1200	16 K	-98.7	70.1	11.5	21.36	22.0
50	4.5	19200	16 K	-95.5	92.3	15.2	19.69	20.1
800	4.5	19200	16 K	-76.2	72.7	11.9	19.69	20.1
50	4.5	38400	16 K	-97.9	83.7	13.7	16.56	15.6

The measured data show that the calculated $ENOB_{ADS}$ closely matches the theoretically determined value of $ENOB_T$. A small difference of approximately 0.5 is probably caused by a non-ideal HW environment and external factors. The record length has almost no impact on calculating the measured parameters due to a sufficient number of sine wave periods in the data record of 4096 samples. The THD value was calculated at -97.13 dB at a sampling frequency of 19.2 kSPS and 50 Hz input signal frequency.

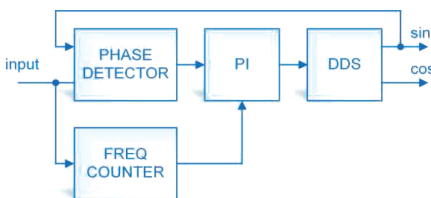
2.4. Algorithms

2.4.1. All-digital phase-locked loop

One of the most important parts of LIA is a phase-locked loop (PLL). The PLL generates a signal whose phase is related to the phase of the input signal [13]. The signal generated by the PLL is then used for multiplication of the input signal of LIA. The all-digital phase-locked loop (ADPLL) is used in the LIA implementation. The chosen FPGA described in Section 2.1 is equipped with internal PLL units. Unfortunately, its minimum input frequency is 15 MHz [14]. The designed LIA should be able to work at the bandwidth of low frequencies. Therefore, a customized ADPLL implementation was chosen.

A block diagram of the designed ADPLL is shown in Fig. 3a. The input signal is delivered into the phase detector. The detector compares the input and output signals of ADPLL and provides information about a phase delay between these two signals. The principle of a phase

a) a block diagram of all-digital phase-locked loop



b) LIA parts implemented in FPGA

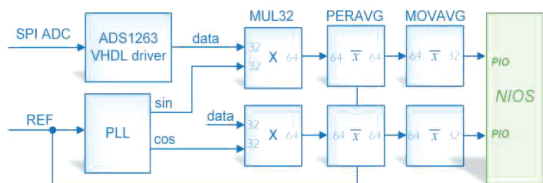


Fig. 3. A block diagram of VHDL parts.

detector is shown in Fig. 4. When a rising edge of the input signal is detected, the counter is enabled. The source clock signal of the counter is much higher than the input signal. In this case, the counter clock frequency is 40 MHz. The counter is enabled until a falling edge of the DDS output signal is detected, and then the counter register value is latched on the output of the phase detector. The minimum counter value belongs to the phase shift of $-\pi/2$ and the maximum value of the counter belongs to the phase shift of $\pi/2$. This value is delivered as an error quantity into the proportional-integral (PI) controller. Thus, the basic task of the PI controller is to maintain the counter value on its centre value that belongs to the zero phase shift between the input and DDS output signals. The PI controller directly drives the frequency of the signal generated by the direct digital synthesis (DDS) block. The proportional and the integral coefficients of the PI controller had been chosen experimentally. The fundamentals of DDS operation are out of the scope of this paper, and they can be found in [15]. A similar DDS FPGA implementation is described in [16] or [17]. The DDS block then provides two digital waveforms: the sine wave that is phase-locked to the input signal and the cosine wave that is phase-shifted by $\pi/2$ to the input signal.

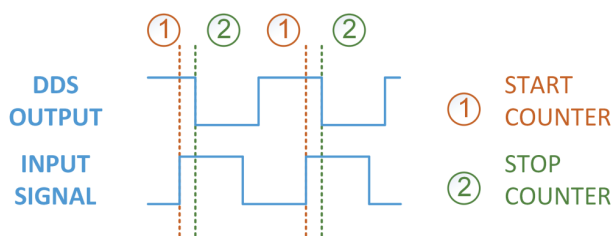


Fig. 4. The principle of a phase detector.

A frequency counter was added into the PLL design to accelerate the PI regulator loop settling time. The frequency counter simply counts input pulses in an interval of 1 second. That provides an approximate input signal frequency with a resolution of 1 Hz. The measurement result is delivered to the PI regulator. If a difference between the frequency counter output and the PI regulator output higher than 5 Hz is detected, the measured frequency value is preset in the PI regulator and settling starts from this point. The known approximate input frequency also enables to adjust the PI regulator coefficients depending on the input signal frequency. This feature provides constant dynamics of the PI regulator loop in a frequency range from approximately 25 Hz up to 1 kHz.

2.4.2. Lock-in parts

The majority of signal processing is accomplished inside FPGA. Fig. 3b shows the currently implemented blocks of the digital signal chain. For SPI data readout the ADS1263 VHDL driver has been written. This block ensures free running of sampled data from ADS1263 via the SPI bus with a correct data word generation. Besides this 32-bit data output, a 'data ready' signal is also produced for a correct synchronization of connected blocks. The output data are directly connected to MUL32 blocks. These blocks take care of calculating the product of the signal with the sine wave and the cosine wave. These data are generated by the PLL mentioned in Section 2.4.1. The output data word is 64-bit long due to the multiplication of two 32-bit numbers. To obtain a DC value of the resulting signal, a low-pass filtering must be implemented. This version of DSP chain consists of a mean value estimator PERAVG, which calculates the mean value from each period of the input signal. The calculated 64-bit value is latched after each period

to the output and is delivered to the MOVAVG block. This block counts the moving average from a predefined number of previously captured mean values of the signal period. The frequency characteristic of the implemented filter is similar to that of a moving-average filter. In our case, the cut-off frequency of the designed low-pass filter is $f_{-3\text{ dB}} \approx 0.5\text{ Hz}$. The results obtained from real measurements and presented in Chapter 4 have confirmed that this simple method of low-pass filtering is sufficient.

2.4.3. NIOS upper layers

Visualization and representation of data is accomplished inside the software processor NIOS 2 Gen 2. Several instruments like high-speed partial discharge meters [18] use soft-core processors to support DSP chains for communication and data exchange. The core is running at 100 MHz frequency. This SoC controls the Ethernet connection, the USB connection, as well as LCD visualization. In addition, it acts as the ADS1263 SPI master for mode settings in units, like a programmable-gain-amplifier (PGA), speed and input multiplexor. An SPI bus fusion is performed inside the VHDL blocks. An offset and gain correction of ADC is also configured. The output words from LIA parts described in Section 2.4.2 are connected to the parallel input-output ports (PIO) of NIOS. Converting these binary data to a readable form in terms of scale and units is performed inside the firmware written in C language. This method enables a variety of data post-processing operations with the support of a higher level programming language.

3. Analogue test platform

An analogue test platform implements the synchronous detector using analogue parts, such as operational amplifiers and analogue integrated circuits. This platform was developed for capacitance and dissipation factor measurement purposes [19]. A block diagram of the platform is shown in Fig. 5. The input signal is filtered using a band-pass filter BPF. The centre frequency of the BPF filter is adjusted to the value of carrier frequency of the input signal.

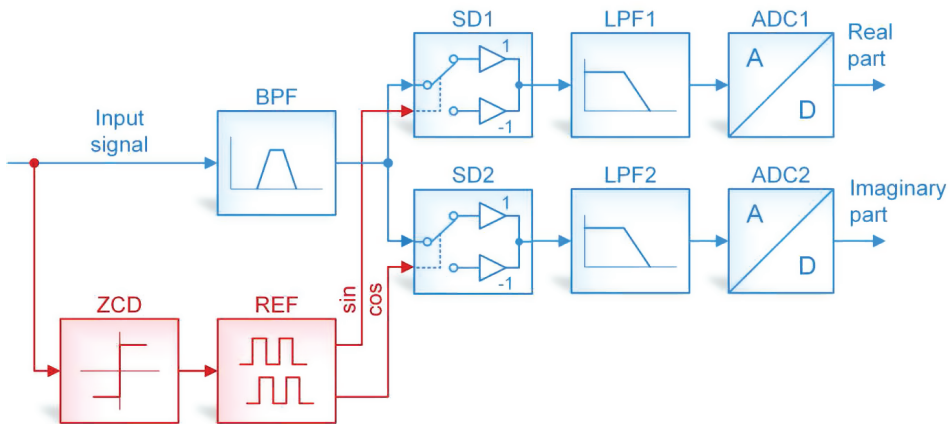


Fig. 5. A block diagram of the analogue test platform.

The filtered signal is delivered to two synchronous modulators SD1 and SD2. Each of the modulators consists of one AD630 integrated circuit. The circuit contains two operational ampli-

fiers with separately adjustable gains. These gains are adjusted to -1 and 1 for this application. Gain switching is implemented using control inputs. The control inputs are fed with two separated signals generated by a reference signal REF from the generator. Both signals are square-shaped with the same frequency as the input signal. The sine wave signal is phase-locked to the input signal, and the cosine wave signal is phase-shifted by $\pi/2$ to the sine wave signal. This topology provides decomposition of the input signal into the real and imaginary parts.

The outputs of modulators are filtered using low-pass filters LPP1 and LPP2 with a very low cut-off frequency to obtain the mean value of the modulators' signals. In this design, a cut-off frequency of 0.5 Hz and filter order of 8 were chosen. The filters are composed of four-stage operational amplifiers in Sallen-Key topology; each stage of the order 2 . The outputs of LPP filters are digitized using two analogue-to-digital converters ADC1 and ADC2. The AD7190 converters with sigma-delta architecture, 24 -bit resolution and maximum data rate 4.8 kHz were chosen. An effective resolution of this converter with a particular setting is 21 bits, according to Tab. 7 in [20].

4. Comparison

The proposed digital LIA has been compared with the classical analogue solution, as described below. Both instruments have been tested by several types of input signal. Various performance characteristics have been analysed and compared. All tests have been carried out with 50 Hz input signals. This frequency was chosen mainly to meet the requirements of the analogue instrument which is trimmed for this value. The analogue instrument and also the digital instrument will be used in the high-voltage diagnostic, and this frequency corresponds to the mains frequency in Europe. Long-term results of stability apart from immediate static tests' results were also examined.

4.1. Testing signals

Stability and noise levels have been analysed with shortened input and connected TTL reference input. The digital LIA was running and sending the values of real and imaginary parts to the computer for data acquisition. In addition, the linearity has been analysed. Both instruments measured the signal in the zero phase at various amplitudes. Special emphasis was put on sensitivity to very little changes of signal phase. The previously mentioned generator SR DS360 could not be used due to the lack of phase setting. Therefore, an Agilent 33522A was used in the phase sensitivity tests. This generator inherently supports the phase adjustment as low as 0.01° . For instance, in the case of dissipation factor measuring device this value corresponds to a change of $\tan \delta = 1.7453 \cdot 10^{-4}$. The digital solution was able to measure such a phase change with a substantial reserve. To prove the sensitivity for even smaller phase changes, a special approach was chosen. It was necessary to overcome the limitation in phase adjustments of the generator. Using RC filters to produce a stable phase change of 0.001° was excluded mainly due to their sensitivity to temperature and the impact of connections. Nevertheless, the used generator had a sampling rate of 250 MSa/s with a maximum number of one million points. In the case of 50 Hz signal and using the whole memory for one period of the signal, a single sample takes 20 ns. This time shift corresponds to a phase change of 0.00036° . The testing datasets consisted of the original period of sine wave signal and the signal with a shift of three samples. In other words, a phase shift of 0.00108° and a change of $\tan \delta = 1.9 \cdot 10^{-5}$ were achieved. Also, to examine a possibility of measuring a signal with a very poor SNR ratio, the last part of tests used arbitrary

input signals with -20 dB and 0 dB SNR ratios. All testing signals had a static amplitude of 500 mVpp. Only the linearity test varied the amplitude. The sampling frequency of the digital solution was 19.2 kHz. The majority of results describe the real part of voltage output as X and the imaginary part of voltage output as Y .

4.2. Results

4.2.1. Noise level

While the input is grounded, LIA takes more than 10 minutes for acquisition. Corresponding data for the real (X) and imaginary (Y) parts were analysed. Calculating the RMS value of noise and the peak-to-peak value gave the following results for the digital solution:

$$RMS_X = 87 \text{ nV}, \quad PkPk_X = 486 \text{ nV}, \quad (7)$$

$$RMS_Y = 90 \text{ nV}, \quad PkPk_Y = 479 \text{ nV}. \quad (8)$$

For the analogue circuit the results are following:

$$RMS_X = 719 \text{ nV}, \quad PkPk_X = 4380 \text{ nV}, \quad (9)$$

$$RMS_Y = 939 \text{ nV}, \quad PkPk_Y = 4934 \text{ nV}. \quad (10)$$

4.2.2. Linearity

The input of digital LIA was excited by a sine wave with an amplitude from 0.1 Vrms up to 1 Vrms. The squared value of correlation coefficient r^2 for both instruments was 0.999998 . Linearity is comparable in the stated range. According to the noise levels, the linearity range from much lower voltage levels can perform worse for the analogue circuit. Nevertheless, more emphasis was put on the following test signal results.

4.2.3. Sensitivity to phase shift

The first analysis was performed for a phase change of 0.01° , as this functionality is directly supported by the chosen Agilent generator 33522A. The results are shown in Fig. 6a for the dig-

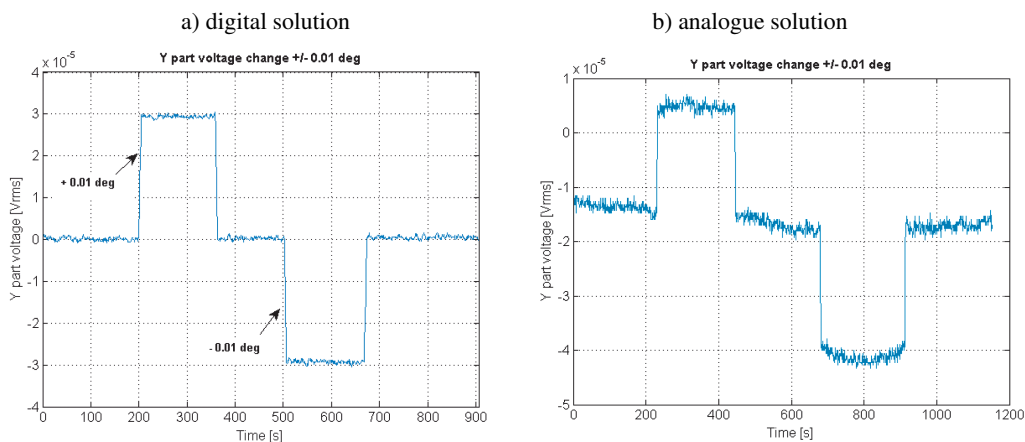


Fig. 6. Sensitivity to a phase change of 0.01° .

ital and in Fig. 6b – for the analogue solutions. The input signal had an amplitude of 500 mVpp. This phase change generates approximately a 30 μVrms amplitude change. The analogue instrument was able to sense such a phase change, but a higher noise level was present.

A phase shift of 0.00108° was generated according to 4.1. The results are shown in Fig. 7a for the digital solution and in Fig. 7b – for the analogue one.

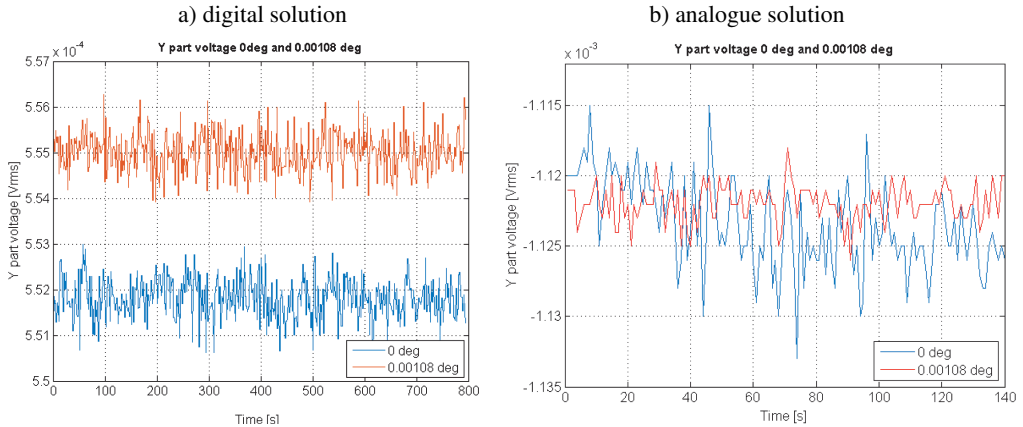


Fig. 7. Sensitivity to a phase change of 0.00108°.

These results show that the proposed LIA design is fully able to measure a phase shift as small as 0.00108°, whereas the analogue solution (Fig. 6b) fails to produce a reasonable result. A sensed phase change with a digital instrument generates approximately a 3 μVrms amplitude change. Calculating the difference of phase in (11) between two outputs in Fig. 6a corresponds to the adjusted generator phase.

$$\tan^{-1} \left(\frac{\bar{X}_{0.00108}}{\bar{Y}_{0.00108}} \right) - \tan^{-1} \left(\frac{\bar{X}_0}{\bar{Y}_0} \right) = 0.00105^\circ. \quad (11)$$

4.2.4. Long term stability

The measurement repeatability over a long time period was analysed with a static input signal. It was a sine wave with a phase shift of 0.00108°. The time frame was more than one hour. From the results shown in Fig. 8a, it is clear that the measuring chain is stable for a long period with no drifts or other defects. In other words, there is no need for frequent calibration of the device. This result is not attained for almost all analogue circuits used.

Figure 8a shows on the left y-axis the real (X) part (in blue) and on the right y-axis the imaginary (Y) part (in orange) of the signal for the digital solution. The right axis shows that the peak value of noise from mean value during long-term stability is about 1.5 μVrms which is sufficient for determination of phase changes as low as 0.00108° because this change was equal to 3 μVrms. On the other hand, the result of long-term stability test of the analogue instrument in Fig. 8b shows that the Y part voltage drifted by more than 60 μVrms, which can cause a problem even for sensing phase changes in a range of several 0.01°.

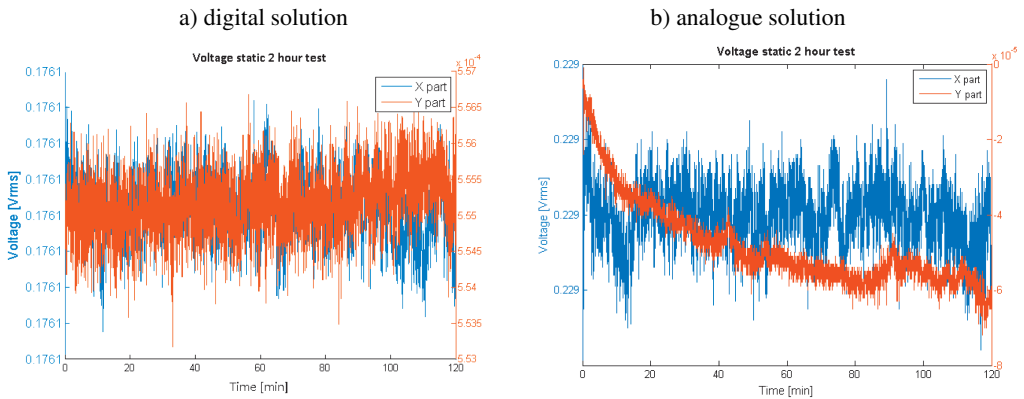


Fig. 8. Two hours' long-term stability tests.

4.2.5. Signals with low SNR

During the last test, the LIA measured two types of signal with poor levels of SNR: -20 dB and 0 dB. To obtain a reference value for comparison, an SR 830 lock-in amplifier was used. The results with standard deviation values measured during a 2-minute period are given in Table 2.

Table 2. Testing results for input signals with poor SNR.

SNR [dB]	U_X [VRMS]			σ [μ V]	
	SR830	digital	analogue	digital	analogue
0	0.16124	0.16125	0.16512	8.18	30.01
-20	0.16125	0.16126	0.16510	4.14	12.63

5. Limitations of digital solution

The proposed solution of digital LIA was implemented purely in the VHDL language. The NIOS part of design is intended only for data visualization. The design can be applied to any FPGA device with no limitation. Embedded multipliers are the key parts of the proposed design. The presence of DSP block also in modern CPLD devices like Altera MAX 10 can be used to keep design and manufacturing costs as low as possible. The implementation on a single-chip microprocessor platform has specific limitations. A selected CPU should support advanced HW multiplication unit to achieve the real-time signal processing capability. Generation of the DDS algorithm in the microprocessor requires a very precise time base setting. The VHDL form of the algorithm is sampling frequency-independent and limited only by the chosen FPGA design. The sampling frequency is the main limiting factor for the microprocessor implementation.

In contrast with the classic LIA designs, this solution does not need to implement any kind of input filter inside the FPGA. Implementation of this part will be examined in the future. It will be checked whether it brings any improvement to the LIA performance.

6. Conclusion

This paper deals with the design of a fully digital lock-in amplifier with emphasis put on a direct comparison of the proposed solution with the existing analogue design. A high-performance FPGA device Arria V was used as the digital platform. A new high-performance, high-resolution ADS1263 analogue-to-digital converter provides an interface between input signals and the digital domain. Higher layer data can be calculated by C-language procedures supported with an NIOS II SoC processor. All other resources are written in pure VHDL language which can be helpful in any future work on various FPGA or CPLD platforms. The designed hardware and firmware offers outstanding parameters in terms of sensitivity, stability, and repeatability of measurement. The hardware design and layout is a much more compact in comparison with the classic analogue devices. The testing results of the digital platform are shown in Fig. 8. On the other hand, an analogue circuit can be used only in a noise-free environment, namely in laboratories. For instance, the user must provide a signal with a larger amplitude to overcome noise problems along with stability issues. For example, measurements of low voltages and small phase changes are almost impossible. A relatively high number of analogue parts needs a special selection along with tuning of parasitic parameters. From an implementation point of view, the analogue circuit is more sensitive to the PCB layout quality, and even the cost of selected analogue components can exceed that of FPGA design of digital LIA.

In the future work there will be analysed a possibility of implementing more advanced digital filters inside FPGA to obtain even better parameters. The hardware will be equipped with an input front-end to achieve the capability of measuring higher voltage ranges. This device can be employed in calibration or metrology applications mentioned in [21]. Another area of application can be the non-invasive diagnostics.

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