A Comparative Study of Super-Regenerative Receivers for BAN Applications

Sherif Saleh and Ghada Hamdy

Abstract—Super-regenerative receivers have regained attention due to their unique properties making them suitable candidates for applications necessitating simplicity and ultra-low power consumption such as Body Area Networks (BAN) targeting medical devices and near body entertainment devices. In this paper, several super-regenerative receivers are proposed showing the flexibility and the ability to accommodate proper demodulation of on-off-keying (OOK) and Multi-level (M-ary) PSK modulated signal with a very limited power budget. Circuit implementation and simulation results are shown.

Index Terms—Super-regenerative receiver; phase detector; on-off keying; QPSK demodulator; phase detector

I. INTRODUCTION

OVER the last decade, Wireless Sensor Networks (WSN) and Body Area Networks (BAN) have gained a considerable interest, resulting in the prolific increase in the research and development in this field. Contributing factors leading to this increase include continued efforts to achieve miniaturization using low power circuits, devices and computations, as well as standardization efforts to develop short-range communication such as IEEE 802.15.6, which targets healthcare applications.

Several frequency bands have been defined for the use in healthcare applications, as Medical Implant Communication Service (MICS) band, defined in 402-405 MHz frequency range. This features lower propagation attenuation through the body tissue compared to the 2.4 GHz frequency band [1], which favors using MICS band in implanted and in-body devices, this urges for long term operation translating into extreme low power consumption during both operation and idle periods. When looking at the wireless transceiver part of the sensing node, achieving low power consumption drives the adoption of different design techniques where reviving the old forgotten super-regenerative reception concept is one of those techniques.

The basic idea behind super-regenerative reception is based on how the oscillator responds to an injected RF signal in its own tank and under periodic switching between ON and OFF state, which is called quenching. Super-regenerative oscillator starts-up faster when an RF signal is injected at the oscillator tank, the stronger the RF signal, the faster the oscillator starts-up. This stands for the amplitude to time conversion property of the super-regenerative-oscillator (SRO). The regenerative action builds a strong oscillator signal from a weak RF signal that is why super-regenerative receivers (SRR) offers high gain while consuming much less power than an equivalent amplifier

with the same gain, [2]. Another interesting property of SRR is its phase preserving property, where the signal generated in the super-regenerative oscillator (SRO) preserves input phase information at the time it is quenched to oscillate, [3]. In this paper, two super-regenerative receivers operating at MICS band will be presented, where one is tailored for receiving OOK modulated signals, while the other approach is tailored for receiving quadrature-phase-shift-keying, and 8-Multi-level-phase shift keying (QPSK/8-PSK) modulated signals. The proposed receivers will be compared in terms of their targeted application, circuit implementation and performance results.

II. ON-OFF KEYING SUPER-REGENERATIVE RECEIVER

A. Receiver Architecture

The architecture of the SRR is presented in Fig. 1, [4]. It consists of an isolator amplifier (IA), SRO, an envelope detector (ED), quench oscillator, and the demodulator which is realized here as a comparator. The use of a quenching rate equal to the bit rate has a great advantage in improving the receiver selectivity. As a result, synchronizing the quenching signal with the input signal becomes more important.
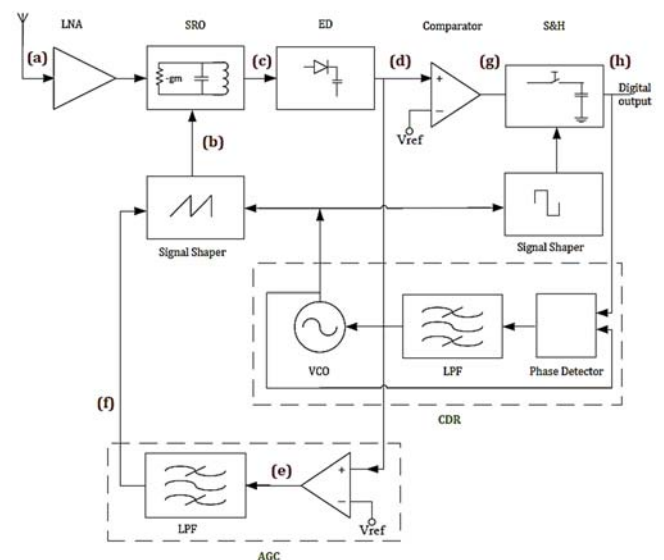

Fig. 1. Block diagram of the proposed On-Off keying super-regenerative receiver, the design includes the automatic gain control, the synchronization feedback loop to detect the phase difference between the output signal and the voltage-controlled-oscillator (VCO) output, the low-pass filter (LPF) that controls the frequency of the VCO [4]

S. Saleh and G. Hamdy are with the Department of Microelectronics, Electronics Research Institute - ERI, Al-Tahrir Street, Dokki, Giza, Egypt (e-mail: sherif_36@yahoo.com).

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An Automatic gain control (AGC feedback loop is applied to control the SRO biasing current according to the incoming signal, to settle the output of the envelope detector. It is designed to draw the minimum current value, which is enough for a suitable swing and envelope detector output. Due to the feedback concept introduced for the internally quenched signal generation, the design of this type (linear-mode) is more complex than traditional linear-mode.

B. Quenching Signal

The shape and the frequency of the quenching signal have a great influence on the performance of the receiver. From this argument, the optimal quenching signal is supposed to have three phases. The first phase is the Q-enhancement phase that stabilizes the receiver just below the critical level where it has maximum selectivity. Then this is followed by the super-regenerative phase, that allows the current to exceed the critical level with the minimum slope and so enables the self-oscillations to be built up. The last phase is the cut-off phase where the current is completely off to save power when there is no need for current.

The optimum quenching signal, shown in Fig. 2 can be achieved by using two transistors in parallel, working as current source for the Colpitt-oscillator, one of them working in saturation region but the other works in sub-threshold region, with a saw-tooth gate voltage, results in the exponential increase as shown in Fig. 2. The saw-tooth quenching current can be achieved by controlling the current source of the Colpitt -oscillator by saw-tooth gate voltage. This gate voltage is generated by charging a capacitor with a constant current source to give linearly increasing voltage. The capacitor is suddenly connected to the ground by a switch, which is controlled by the square signal, as presented in Fig. 3.

C. Simulation Results

From the simulation results depicted in Fig. 4, a quench signal (b) is to trigger the oscillator to sense the input (a). When there is an input signal beginning from 15nV (-96dBm), the oscillation built-up (c) giving a suitable envelope (d) whose amplitude is controlled by the two feedback signals of the AGC: the comparator signal (e) and LPF signal (f) shown in the figure. This envelope is then reformed to give the final output (h) to get the final output (i). The synchronization loop is able to adjust the required bit rate till 13μs when a change happened to the circuit that changes the LPF output value (h) to ground. Afterwards, when there is no change, the loop readjust itself again to give the required bit rate from the VCO.

The total power consumption is adjusted to be around 1mW at the minimum input power level -96 dBm. The dependence of the overall consumed power on the input signal power is very small. This is because the on-time of the receiver is only 30% of the whole period. As noticed, the sensitivity of this design is very competitive compared to that of previous work. In addition, the consumed power has an excellent value compared to the previously reported works. Despite all of these advantages, the designed receiver has a too large bandwidth (BW) compared to the previous work. This is because the BW is dominant by the low quality factor of the inductor of the process used.
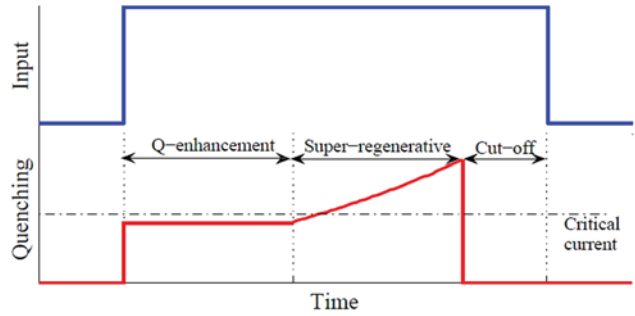

Fig. 2. Optimal quenching signal. It is a signal that is designed for improving the quality factor of SRO. It consists of Q-enhancement phase, super-regenerativephase, and cut-off phase
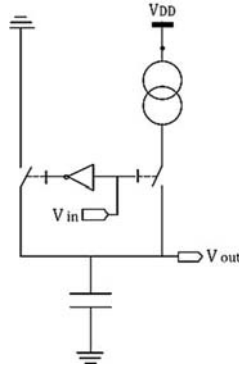

Fig. 3. Schematic circuit design for generating saw-tooth quenching signal from a square quenching signal (Vin). It consists of a capacitor that is being charged by a constant current during the pulse of the square quench and it is connectedto zero for the rest of the cycle
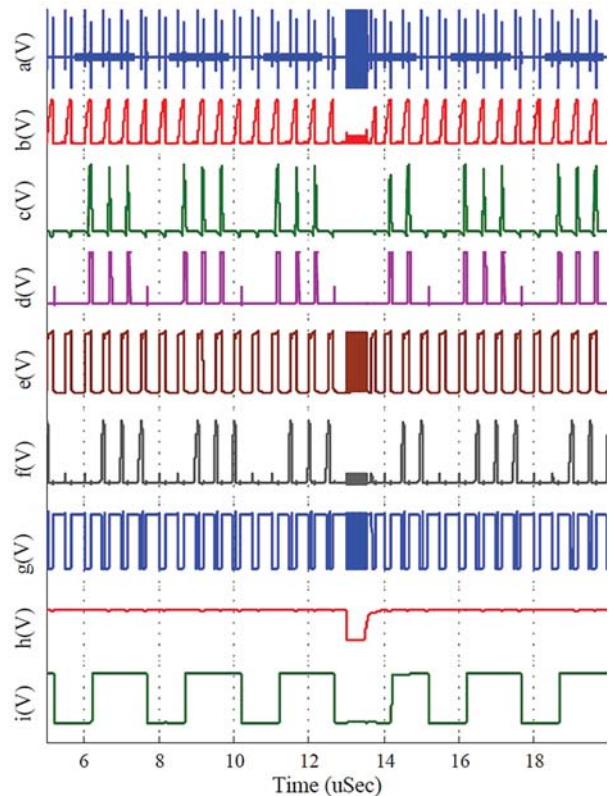

Fig. 4. Waveforms of Linear-mode SRR including the synchronization and AGC loops. Signal (a) presents the input patterns, saw-tooth qunching signal is presented in (b), signals (c and d) show the built-up oscillations and their envelope. The feedback control signals (e and f) are used for the AGC loop. The final output (h) is detected by using (g) as an input for a S&H element (h) shows the LPF output, finally, (i) indicates the final output bits

The designed receiver based on On-Off keying presents a good sensitivity of -96dBm at 403MHz; the data rate is considered 1Mbps while the power consumption is 1mW. Despite these advantages, the designed receiver introduces disadvantages, where the bandwidth is large, due to the low quality factor of the designed inductors. The existence of the clock and data recovery system saves the need of an external oscillator, while the AGC loop improved the sensitivity to reach -96dBm.

III. M-ARY PSK SUPER-REGENERATIVE RECEIVER

A. The Concept of M-ary PSK Phase Detection

To extend SRO capabilities to detect QPSK modulated signals, the same mechanism of synchronous quenching with a rate that equals symbol rate is used. During each symbol period, as the SRO is quenched to oscillate, the phase information in input RF excitation will be regenerated in the resulting SRO oscillations. The result is a full swing sinusoidal signal that preserves the symbol phase information modulated in the input weak RF excitation.

So, the next step is to try to extract (i.e. demodulate) the phase information in this full swing sinusoidal signal using simple detection concepts while avoiding classical down-conversion steps to reduce complexity. The proposed concept will be explained by QPSK modulation case, and then extended to 8-PSK, any other M-ary PSK would be a straightforward extrapolation.

The basic idea of detection method can be illustrated in Fig. 5(a), where SRO output oscillations are conditioned to generate four quadrature phases to clock four identical counters. Depending on the detected symbol phase, one of the counters will lead the rest. Knowing the leading count, the detected phase can be translated to a demodulated symbol value, [2].

This can be further clarified by observing the constellation diagram of a QPSK signal, shown in Fig. 5(b). It is known that any of those constellation points, which represent the possible phases of the QPSK symbols, can be viewed as rotating in the counter clockwise direction. Ref1 to Ref4 denote four quadrature axes located at an arbitrary angle, $\phi°$. If the sent symbol is "00", Ref1 will be the first axis to be crossed by the rotating phase signal, and then Ref2 will be the next. If the transmitted symbol is "11", Ref3 will lead instead, and so on.

The four counters of Fig. 5(a) create the four axes Ref1 to Ref4 of Fig. 5(b). The counters are reset for every sent symbol and started to count, depending on the sent symbol, a particular counter will lead. One issue with this scheme is the arbitrary angle $\phi°$ which is a function of many parameters including the time instant when the counters are enabled. The ambiguity of $\phi°$ can lead to a rotation of the demodulated constellation. However in most communication schemes, the constellation can be properly demodulated in physical layer using information from the pilot.

For proper implementation of the above logic, an enable (En) signal is used to enable counters at a certain t1 time shift from the time t0 where SRO is quenched to oscillate, as shown in Fig. 6; this is for allowing enough time for the SRO to build strong enough oscillations in order to clock the digital counters.

Note that the term "enough time" can be a variable rather than a fixed delay. This comes from the fact that the time for the SRO to build oscillations strongly depends on input RF signal power levels. A strong input RF signal leads to fast building of SRO oscillations, which would enable the reduction in t1 delay value, consequently reducing quench cycle, which reduces average power consumption by SRO. This can be seen as an automatic gain control feature inherent in the SRO operation.

The time shift t1 relative to t0 is a main factor defining the relative phase angle $\phi°$, this time shift t1 should be long enough to allow oscillations to build up. When En signal goes high, the counters will start and the counter corresponding to the proper RF phase will lead the rest, as explained earlier. When the leading counter reaches a predetermined terminal count, all counters are disabled, thereby freezing the state. Depending on this state, the leading counter is easily determined and the corresponding RF phase is easily identified. This is shown in Fig. 6. Looking closely, we can conclude that the duration of Tc is not critical. The time t1 does not need to be set to an accurate quantity; however it needs to be repeatable from cycle to cycle, to ensure a fixed set of reference axes with respect to constellation.

An 8-PSK modulated signal can be demodulated by extending the above concept. Now, eight phase shifted versions from SRO output oscillations need to be generated, [5], as can be seen in Fig. 7(a), this requires two cascaded stages of RC/CR networks rather than a single stage in case of QPSK demodulation, this is shown in Fig. 7 (b). Counters has been replaced with shift registers to simplify logic and reduce associated power consumption.
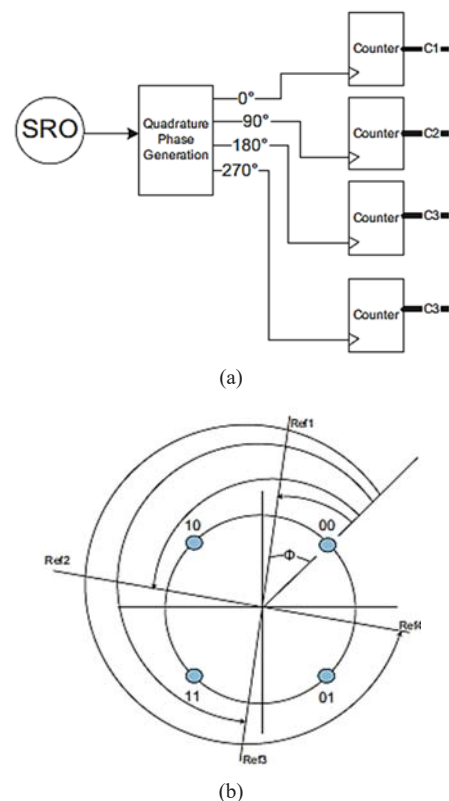

(a)

(b)

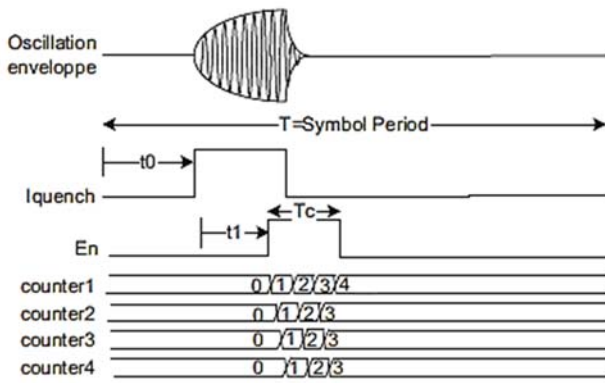Fig. 5. (a) QPSK detection scheme (b) Equivalent QPSK constellation and reference axis
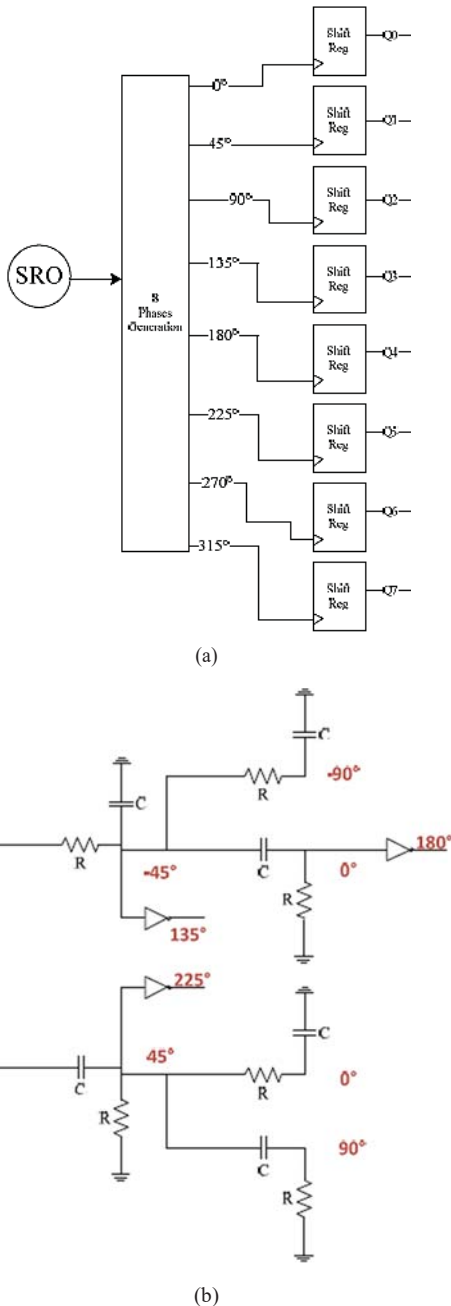
Fig. 6. QPSK detection and timing diagram

B. Simulation Results

Both super-regenerative receivers were designed using a 0.13μm technology, with off-chip inductors for the SRO Colpitts oscillator circuit to have higher quality factor and lower power losses. Circuit simulations show proper demodulation of both QPSK and 8-PSK modulated signals.

Fig. 8 shows the simulation results of the complete 8-PSK SRR, where Fig. 8(a) shows how a distinct shift register leads the others for each symbol values of the eight values of an 8-PSK modulated signal, Fig. 8(b) shows the proper reconstruction of sent data. The total power consumption for the QPSK SRR is 135μW at the minimum input sensitivity signal of -80dBm for a sent data rate of 2Mbps which is equivalent to 62.5PJ/b. while the 8-PSK SRR reported a power consumption of 135μW at the same sensitivity level but for a 6Mbps equivalent to 22.5PJ/b. This shows that both simplifying detection logic and going to a higher M-ary modulation scheme has resulted in a more energy/bit efficiency.
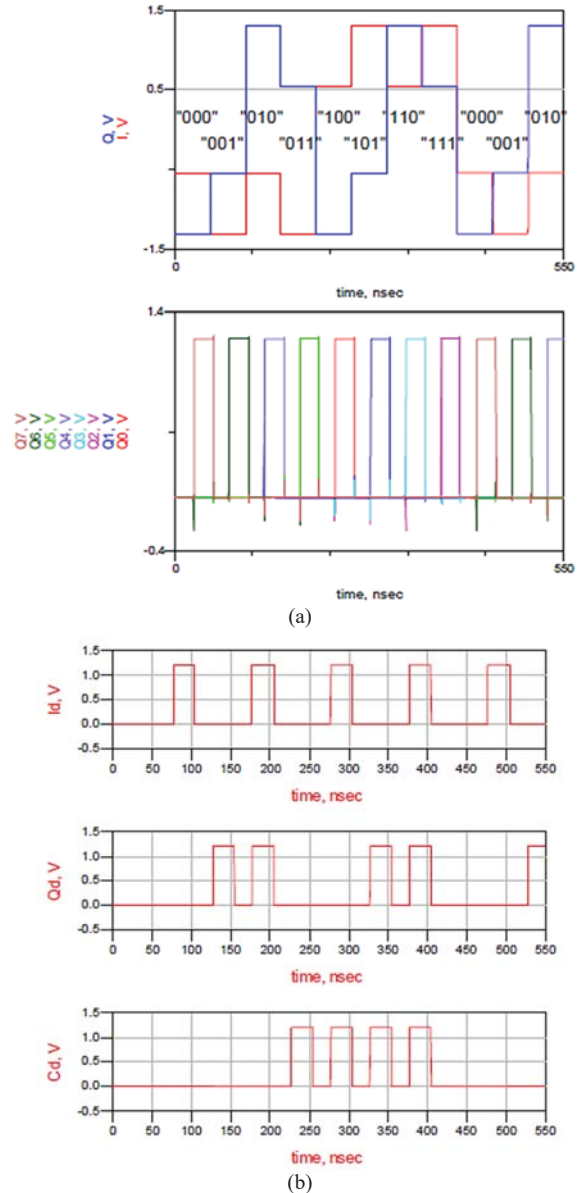

(a)

(a)

(b)

Fig. 7. 8-PSK detection scheme, (b) phase generation circuit

(b)

Fig. 8. (a) shift register output for each symbol value for 8-PSK phase detection case (b) reconstructed (demodulated data)

IV. LAYOUT OF THE PSK RECEIVER

The layout of the complete PSK receiver is shown in Fig. 9, in a 0.13μm UMC technology featuring one poly layer, eight metal layers with two top thick metals. The whole receiver occupies 0.646 mm². The digital part, enclosed in the black box is only 105μm x 90μm, adding minimal added area. While the layout of the combined IA and SRO circuit comprising the receiver front-end comprises the rest of the active area, where the gain transistor and cascode transistor are in the middle, input matching on the left and output matching followed by buffer stage on the right, the total front-end area is 800μm x 600μm.

The SRO output signal is buffered using a simple CMOS buffer. This is followed by an eight phases generation block realized here by a simple RC/CR networks. It is important to note that RC/CR networks provide 90 degree phase shift over all frequencies, regardless of absolute values, as long as they are matched, which is almost guaranteed with current CMOS technologies that provide mismatches near 0.01%. Such small mismatches would result into negligible phase mismatches that can be easily tolerated in our system as there exist 45 degree phase steps in QPSK modulation scheme. On the other hand, amplitude imbalances don not have any impact on system operation as the resulting signal are conditioned to clock digital blocks.
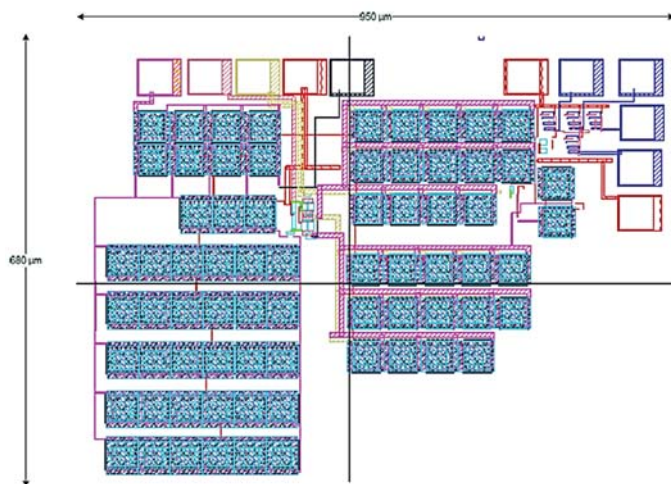

Fig. 9. Layout diagram of the PSK receiver

V. MONTE CARLO VERIFICATION OF THE ASK RECEIVER

To verify the performance of the design Monte Carlo simulation is done. Monte Carlo simulation investigates the ability of the circuit to give the required output in case of process and temperature variations. Therefore, Monto Carlo simulation is carried out. For Monte Carlo investigation, a pattern of zeros and ones is used as an input for the linear-mode SRR. The power of the input signal is varying with time so that the response of the receiver is detected according to the input power. A discrete values of input power is selected to be -40dBm, -20dBm, -6dBm, and 0dBm. The results of the Monte Carlo simulation can be shown in Fig. 10, where 100 iterations are investigated. Figure 10 shows the transient output pattern with the assigned input power of each range in curve (a). Also, it shows the different output patterns that can be found as an

output instead of that in curve (a) due to the process variations. As explicated in the curves (b), (c), (d), and (e), the ability of the receiver to detect small signals decreases from -40dBm, -20dBm, -6dBm, to 0dBm, respectively. For the 100 iterations of the process variations, the receiver can detect 72% of the signals around -40dBm. While it can detect 80% of the signals at -20dBm. Then the ability for detecting more powerful signals begin to saturate until it reach maximum 82% for the signals above 0dBm. The rest 18% of the final outputs indicates the inability of the receiver to return the output at all. This is either because the receiver is unable to differentiate between zero and one and oscillate in all cases, or because the receiver is not able to oscillate when there is input power. This is mainly because of two parts of the receiver, the VCO and the LNA. The VCO has variations in its periodic time that may reach to ±20% of the original desired periodic time. This is due to the variations in the current value charging the capacitor in the delay element.

These variations are large enough to make the oscillator either oscillate at every bit due to large periodic time, or unable to oscillate at all when the periodic time is too small. The dimensions of the VCO components are made larger to improve its functionality, but it does not improve more. LNA has a significant effect on the incoming signal due to the process variations. As a result, another kind of delay element has to be introduced to the VCO that does not have these large variations. Moreover, more adjustments are needed for the LNA to reduce its variations satisfying its requirements at the same time.
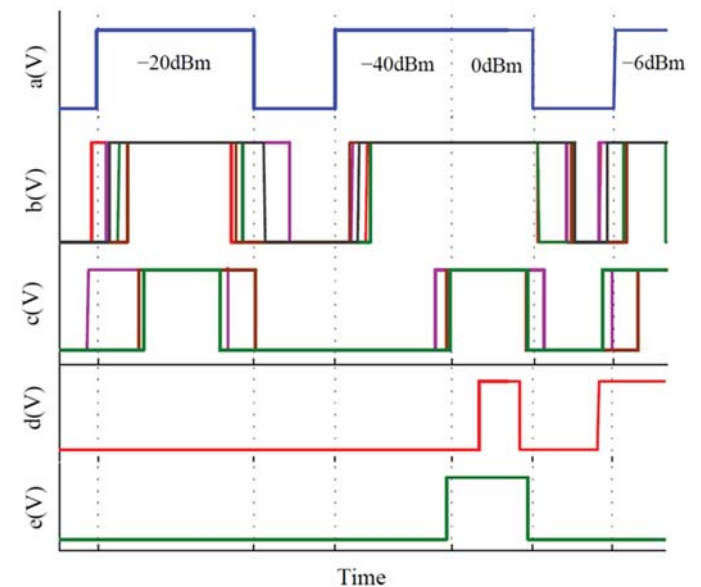

Fig. 10. Monte Carlo simulated waveforms of linear-mode SRR. (a) indicates the output transient pattern. The output patterns of the SRR when the receiver can detect the data correctly is shown in (b). (c) shows the patterns when the receiver can only detect a minimum power of -20dBm. The patterns for the receiver that can only detect from -6dBm and above is shown in (d). For the minimum detectable input power of 0dBm, the output pattern is presented in (e).

VI. DISCUSSION AND CONCLUSION

A comparative study between the designs of a low-power fully integrated linear-mode OOK super-regenerative receiver and M-ary PSK super-regenerative receiver with a very limited power budget is presented in this paper. The OOK SRR is designed to be simple, occupying less area, and consuming a

very low power of 1mW, while receiving OOK data of 2Mbps at 403.5MHz. The design and the simulation results are presented in details. Quenching of the SRO and LNA has been employed to minimize the total power consumption. Automatic control of the dynamic range loop is addressed, which avoids the need of an external oscillator. Meanwhile, an AGC loop has been used, in order to improve the receiver's sensitivity, to detect a minimum input power of -96dBm.

M-ary PSK super-regenerative receiver with a very simple phase detection scheme allowing very low power consumption were reported, however quench generation and AGC loops are not yet implemented.

REFERENCES

[1] L. Zhanget, al., "A Reconfigurable Sliding-IF Transceiver for 400 MHz/2.4 GHz IEEE 802.15.6/ZigBee WBAN Hubs With Only 21% Tuning Range VCO", IEEE JSSC, vol. 53, pp. 2705-2716, Nov. 2013

[2] G.H. Ibrahim, A. Hafez, A. H. Khalil, "An ultra low power QPSK receiver based on super-regenerative oscillator with anovel digital phase detection technique ", Int. J. Electron. Comm. (AEÜ), vol. 67, pp. 967–974, Nov. 2013

[3] P. Palà-Schönwälder, F. X. Moncunill-Geniz, al., "BPSK super-regenerative-receiver. Preliminary results", IEEE ISCAS, pp. 1537–1540, May 2009

[4] S. Alsaegh, S Saleh, al. "Design of 1mW CMOS OOK Super-Regenerative Receiver for 402-405 Medical Applications," IEEE ISCAS May, 2014

[5] G.H. Ibrahim and Amr N. Hafez, "An 8-PSK Digital Phase Detection Technique For Super-Regenerative Receivers," in press

Sherif Saleh Mohamed received his BSc and MSc in Electrical Engineering, with emphasis on Electronics and Communications in 1999 and 2003, respectively, with honor degree from Al-Minia University, Egypt. Sherif Mohamed received the Dr.-Eng. degree from the Albert-Ludwigs-University, Freiburg, Germany, in 2012, both with highest honors. In 2000, he joined the Electronics Research Institute, ERI, Cairo, Egypt, where he was working as a research assistant in the field of low power analog circuit designs. In 2001, he awarded a scholarship from the Information Technology Institute, ITI, to study the VLSI diploma supported by the company of Mentor Graphics, Cairo, Egypt. In 2006, he moved to the Institute of Microsystem Technology, IMTEK, Albert-Ludwigs-University, where he was working toward the Ph.D. degree in the field of RF wireless receivers for medical implantable communication systems until 2012. Since March 2012 Dr. Mohamed is a Posdoc at the chair of microelectronics, IMTEK at the University of Freiburg. Dr. Mohamed' main research interests include analog-signal circuit design, RF wireless transceiver circuits for biomedical applications and Organic Thin-Film Transistors. He is an associate professor at the Electronics Research Institute.

Ghada Hamdy Ibrahim was awarded Bsc, Msc. and PhD from Faculty of Engineering, Cairo University, Electronics and Communications Department, 2000, 2005 and 2013 respectively. During this period, Ghada worked for R&D department, Bahgat group and then moved to Electronics Research Institute, Microelectronics department, where her research interests focused on RF circuit design for wireless sensor networks applications. Ghada joined MIMOS BHD, Malaysia from 2006 to 2008. Currently, Ghada is a junior fellow at Freiburg University, Germany, funded by FRIAS cofund program. She has more than 18 published papers. Her research interests spans RFIC design, printed electronics and MEMS design and microfabrication