Silicon-on-Insulator Technology for Imaging and Application to a Switching Photodetector

Nisrina Abdo, Denis Sallin, Adil Koukab, Magali Estribeau, Pierre Magnan, and Maher Kayal

***Abstract*—This paper analyzes some advantages of Silicon-on-Insulator (SOI) based photodetectors for low light imaging. It shows that SOI based sensors not only solve the bulk carriers problem, it can also act as a very selective spectral filter by acting as a resonant cavity, which is useful in application with a very narrow spectrum of interest, such as bioluminescence imaging. The SOI implementation of a switching photodetector based with an hybrid MOS-PN structure is presented and its advantages in terms of dark current minimization and SNR improvement highlighted.**

***Index Terms*—Photodetectors, Silicon-on-insulator**

I. Introduction

ULTRA-LOW noise photodetector systems are required for applications involving extremely small light intensities, such as astronomy or bioluminescence measurements. Recently, the use of CMOS photodetectors to replace bulky cooled-down charge-coupled device (CCD) sensors enabled the fabrication of small and low-cost bioluminescence labs-on-chip [1-3]. Nevertheless, those systems involve complex analog integration and filtering circuits in order to be able to process the minuscule and noisy signals generated by CMOS detectors. Those analog circuits account for a substantial share of total area and power consumption of the complete system.

In this context, the use of Silicon-on-Insulator (SOI) technologies can be advantageous for two main reasons. First, the presence of the buried oxide (BOX) blocks the so-called "slow-carriers" which are photo-carriers that are generated deep in the silicon and reach the active area of the detector very slowly, introducing non-linearity. Second, differences in refraction indexes of the different constituting materials of an SOI stack create interference effects, which lead to resonance phenomena that significantly increase the quantum efficiency (QE) for certain wavelengths. The resonance can, therefore, be tuned by modifying the width ratios between the active area and the BOX. The latter effect is especially positive in narrow light spectrum application.

In bioluminescence for instance, the wavelength of the emitted light (due to the activity of the enzyme luciferase) is fixed and peaks around 490nm. By placing a resonance at this wavelength, not only the QE for the signal of interest would be boosted, but also the effect of parasitic or ambient light would be mitigated due to the poor QE outside of the resonance, thus effectively acting as a filter.

Previous research [4] on CMOS hybrid MOS-PN detectors showed that they are a good alternative to traditional photodiode-based detectors. Such a photodetector is shot-noise dominated and the output signal is in time domain, with a sharp turn-on and a high magnitude current, which is independent on light intensity. Hence, any analog amplification or filtering is avoided and the total area and power consumption are greatly reduced. However, on bulk CMOS, such a detector needs a ground anchor to operate and its characteristics are highly dependent on the distance to the ground connection and substrate resistivity [5]. This limitation also precludes the fabrication of an array with good performances.

A solution to those problems is to design the same kind of detector on a SOI process. The buried oxide permits to have high potential barriers and virtually no leakage without the need of a ground anchor. Moreover, since each photodetector can be electrically isolated from its neighbors by the use of Deep Trench Isolation (DTI), the design of a crosstalk-free array is relatively easy.

II. Interference and Wavelength Tuning with SOI

Silicon-on-insulator (SOI) technology is an interesting alternative for the integration of photo-detectors due to the geometrical structure of the substrate. On the one hand, SOI is considered as a possibility to avoid the slow diffusion current, which is caused by carriers being generated by light with long wavelengths beneath the depletion region of a sensing component. In fact these carriers diffuse back to depletion region adding a low speed component to photocurrent and degrading the dynamic behavior of the sensing component in bulk CMOS. In contrast, the BOX in SOI isolates the sensors and avoids the slow diffusion current from reaching its sensitive depletion region. On the other hand, due to the contrast of refractive index between silicon and silicon dioxide, the stack of SOI material (Fig. 1) results in a confinement of light in the active region for a certain wavelength range and thus a significant improvement of the quantum efficiency.

This work was supported by the Swiss National Science Foundation under Grant 200021_140447.

D. Sallin, A. Koukab and M. Kayal are with the Institute of Electrical Engineering (IEL), École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland (email: denis.sallin@epfl.ch).

N. Abdo, M. Estribeau and P. Magnan are with the Integrated Image Sensor Laboratory, ISAE-SUPAERO, 10 Av. E. Belin BP 4032, 31055 Toulouse Cedex 4, France.

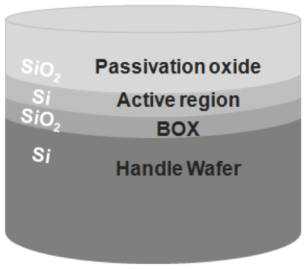

Fig. 1. Structure of a SOI process.

According to the transfer matrix formalism [6-8] every layer can be modeled by a two dimensions transfer matrix in which each element modulates its reflectance, transmittance and absorbance. A stack of layers can be modeled by the product of each constituting layer matrix. We can easily find that the product $n_i \times d_i$ is the main element that defines the type of a layer in the way of reflectivity and transmissibility. n_i is the refractive index for a fixed wavelength λ_0 and d_i the layer thickness. For example, in the case of quarter-wave layer where $n_i \times d_i$ is proportional to $\lambda_0/4$, there is a non-reflecting layer and a maximum interferential effect. In a multilayered system like a SOI stack, a high confinement of light in the active region can be achieved by adjusting layer dimensions, resulting in an improvement of the external quantum efficiency (which is defined by the ratio of generated charges in the active area to incident photons. Recombination rate is assumed to be zero). If a front side illumination is considered, this could be achieved when the stack of SiO_2-Si-SiO_2 structure exhibit simultaneously a minimum reflectance and transmittance and a maximum absorbance. In this case two main elements affect the absorbance and the reflectance of the stack:

- The penetration depth of photons in silicon (Fig. 2) which is modulated by the imaginary part of the refractive index of silicon varying with wavelength.
- Constructive optical interference in the active region induced by multiple reflections of optical beam due to interfacing with SiO_2 layers.

The wavelengths range of interest and their absorption depth in silicon are thus the principal criteria in the choice of SOI technology and mainly its active layer thickness. The thickness of the silicon under the BOX is less important since the absorbed optical power there doesn't contribute to sensor signal due to the oxide isolation.

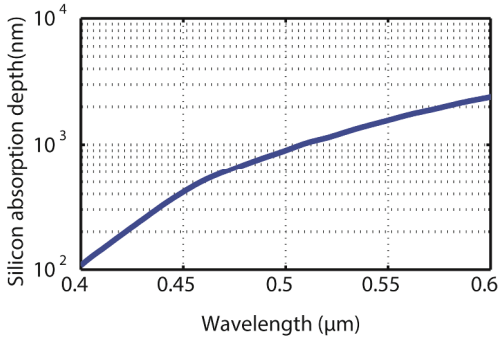

Fig. 2. Optical penetration depth of photons in silicon for wavelengths ranged between 400 and 600 nm.

As a case study, a detection domain for wavelengths ranged between 450 and 500 nm, which is around bioluminescence detection wavelengths, is considered. Fig. 2 shows that the penetration depth of silicon is ranged between 400 and 800nm, so the silicon active region should have at least 400nm thickness. In addition, due to the presence of SiO_2 layer, optical interference phenomena can contribute to the optimization of the optical response or its deterioration. In order to study these issues and find optimal SOI substrate, the external quantum efficiency of the structure is computed by using the transfer matrix formalism with a normal incidence front illumination. Fig. 3 shows the periodic influence of BOX thickness d_{BOX} on the value of external QE. This influence shows modulation peaks. We can obtain very good peaks for detection at 490 nm where external QE reaches more than 70% which is very interesting for bioluminescence imaging. To find the optimal associated dimensions of SOI and BOX layers for bioluminescence detection, external QE vs d_{BOX} and d_{SOI} is depicted in Fig. 4. It shows that due to the presence of BOX layer, high peaks of detection efficiency are obtainable, even when silicon active layer thickness is less than its optical absorption length.

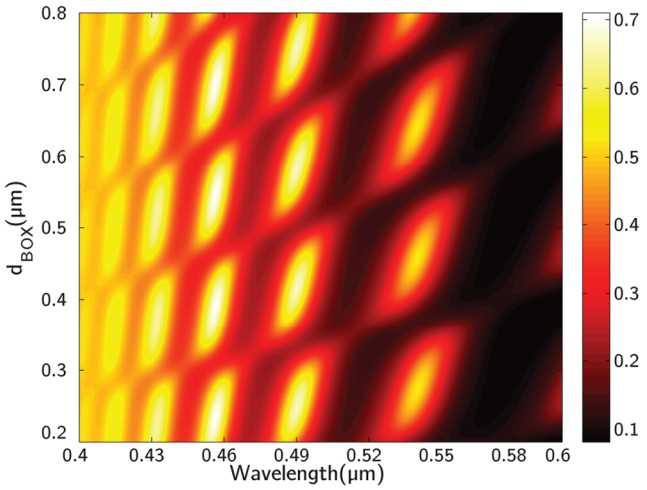

Fig. 3. External quantum efficiency for a silicon active region thickness of 395nm Vs Box thickness d_{BOX} and wavelength.

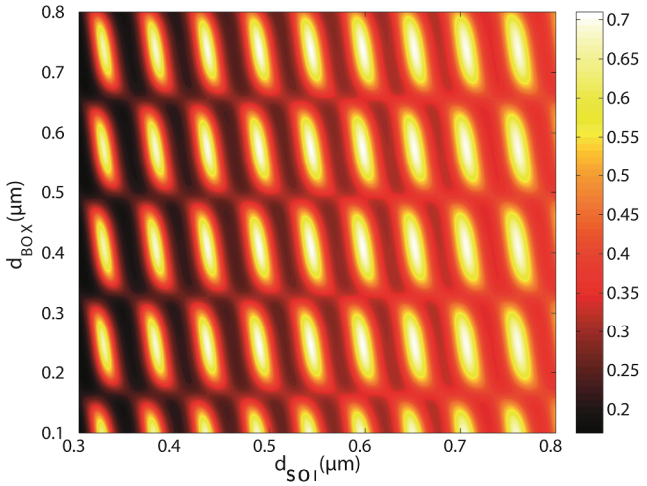

Fig. 4. External QE vs thickness of SOI layer d_{SOI} and BOX layer d_{BOX} for wavelength of 490nm.

An example of application of this parametrical study is shown in Fig. 5, where optimal detection peaks are tuned by d_{BOX} and d_{SOI}. The curves show clearly the optimization of the QE for different wavelength and its correlation with the BOX thickness.

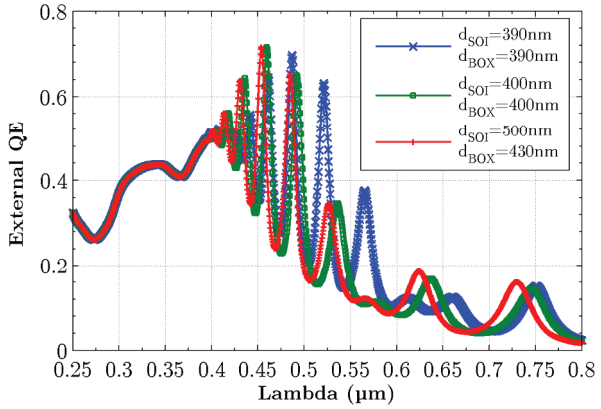

Fig. 5. Wavelength tuning by variation of different layer thicknesses.

III. Application: SOI MOS-PN Photo-Detector

The analysis presented in section II is independent of the type or the structure of the photodetector. These results can thus be used in the optimization of the new hybrid MOS-PN detector, recently presented in [4]. It will even be demonstrated that this type of detector is particularly well suited for an SOI implementation.

The structure of the detector, shown in Fig. 6, is CMOS compatible. It consists of a p+ diffusion (anode) and n+ diffusion (cathode) forming the diode and a gate directly adjacent to the p+ diffusion that create a charge integrator.

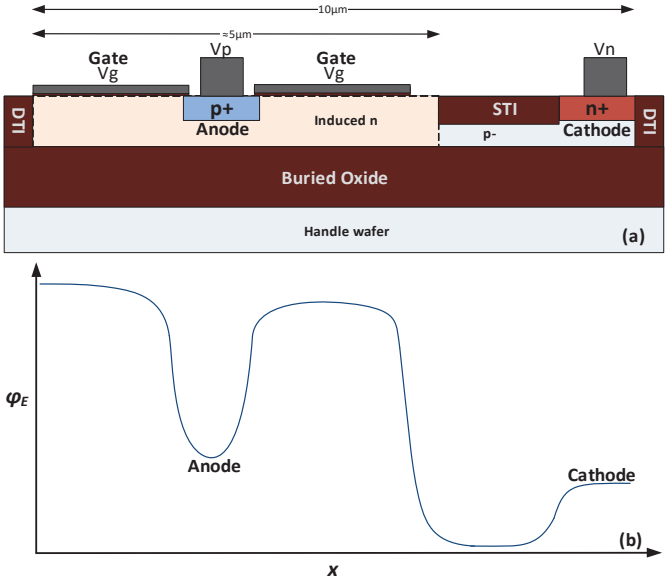

Fig. 6. a) Structure and operation of the photodetector (Vp and Vg switched to a positive voltage, with depletion region). b) Illustration of the electrostatic potential (ϕ_E) across the device, with depletion-induced potential barriers.

A. Operation

When a positive voltage step Vg is applied on the gate, a space-charge region as well as a potential barrier is created around the anode as shown in Fig. 6. The structure can then be understood as a thyristor (p-n-p-n), which has the property to latch-up. At the same time, a positive voltage step is also applied on the anode, while the cathode is kept grounded. Due to the potential barrier, there is no current flowing between the anode and the cathode. The device is now in a non-equilibrium state. Over time, electrons generated in the device (either photo-generated, thermally generated, or leaking over the cathode barrier), will accumulate under the gate and decrease the potential barrier as well as the strength of the electric field. When a sufficient amount of carriers have accumulated (dependent on gate voltage), the potential barrier decreases enough and the anode starts to inject holes, which will initiate the latch-up process of the p-n-p-n structure, with a very steep increase in current magnitude. The device can thus be understood as a charge integrator and comparator: the device turns on when an amount of charge Q_{tot} is accumulated. The transition to the conductive state is characterized by a steep increase in current with a high magnitude as demonstrated by TCAD simulation in Fig. 7 [4]. In order to reset the device, the gate and anode are grounded, while a positive voltage step is applied on the cathode.

The photodetector and its readout circuits, shown in Fig. 8 was already implemented in Bulk CMOS (UMC 0.18 um) and its operation experimentally demonstrated (see [4, 5] for more details).

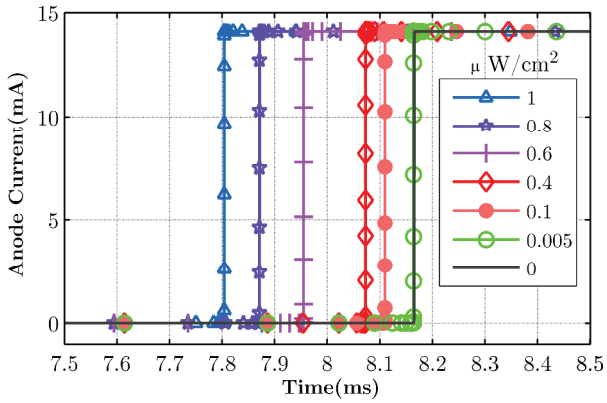

Fig. 7. TCAD simulation of current versus time for different light intensities. Bulk CMOS implementation of the detector.

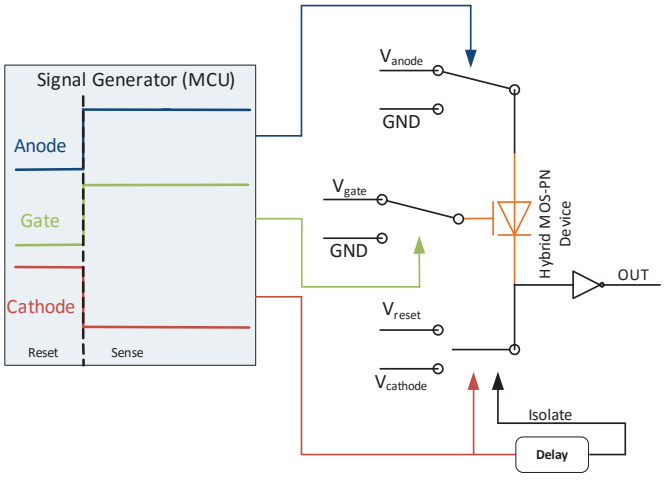

Fig. 8. Simplified schematic of the Sensor Front-End and its different phases (photodetector in orange).

B. Modelling

In the ideal case, the time to latch-up, also called triggering time (T_{trig}), can be expressed in terms of the required charge Q_{tot}, the accumulation rate of photo-generated electrons - or photo-current (i_{phot}), and accumulation rate of dark-generated electrons (i_{dark}).

$$T_{trig} = \frac{Q_{tot}}{i_{phot}+i_{dark}} \quad (1)$$

This relation can be rewritten in terms of light intensity (I_{light}), taking in account the photoactive area of the device (A), the quantum efficiency (QE_λ) and the energy of each photon (E_{ph}=hc/λ), or the responsivity of the detector (R_λ).

$$T_{trig} = \frac{Q_{tot}}{\frac{A \cdot QE_\lambda \cdot q}{E_{ph}} I_{light}+i_{dark}} = \frac{Q_{tot}}{A \cdot R_\lambda \cdot I_{light}+i_{dark}} \quad (2)$$

Those equations show that there is an inverse relationship between T_{trig} and I_{light}. The readout of the sensor can thus use pulse modulation or frequency modulation signal processing to detect light [10].

Equation (2) also shows that, in order to have a good sensitivity of the detector, i_{dark} should be minimized. Moreover, decreasing the dark current improves the intrinsic SNR of the device, especially for low light intensities. Indeed, any decrease in dark current automatically translates into a decrease of its associated shot noise ($\sigma(N)=N^{1/2}$). The expression of the intrinsic SNR can be easily derived from the ratio between the number of integrated photo-charges (N_{phot}) and the total noise in the device [11].

$$SNR_{intrinsic} = \frac{N_{phot}}{\sqrt{\sigma_{dark}^2+\sigma_{phot}^2}} = \frac{\sqrt{Q_{tot}/q}}{\frac{i_{dark}}{i_{phot}}+1} * \quad (3)$$

From (3), it is clear that any decrease in i_{dark} translates in an increase of the SNR. The effect is especially important for low light intensities (e.g. in bioluminescence imaging).

C. Advantages of SOI

In a standard bulk CMOS implementation, the p-substrate has to be grounded. The reason for this is twofold. First, if the device is co-integrated with circuit, the substrate is mandatorily grounded. Second, substrate grounding is necessary to guarantee high enough potential barriers for the photodetector to operate with good performances even with a non-perfect shielding of the p+ diffusion [5]. Unfortunately, one side effect is an increased leakage current from the anode towards ground, which has a negative impact on power consumption. This drawback can be attenuated by designing a system the photodetector is driven by a pulsed voltage [9].

Another issue with standard CMOS implementation is the lack of strong device isolation that could lead to crosstalk in the case of a sensor array.

Those issues do not exist on SOI. In fact, the use of deep trench isolation (DTI) in SOI process make the photodetector is totally isolated. Second, the anode shielding by the depletion region is greatly improved since the silicon region between the gate and the BOX is almost totally depleted. That way, there is no room for anode leakage currents. This in turn almost cancels cathode leakage dark current, which leads to a better SNR, as explained in the following sub-section.

D. Poly-gate effect on quantum efficiency

On the other hand, the absorption of polysilicon gate could be very detrimental or QE if the sensitive part of the MOS-PN photodetector is limited to its MOS part. In order to estimate the sensitivity of the different zones of the MOS-PN photodetector, performances have been simulated for three illumination zones: gate, central and cathode sides, as illustrated in Fig. 9.

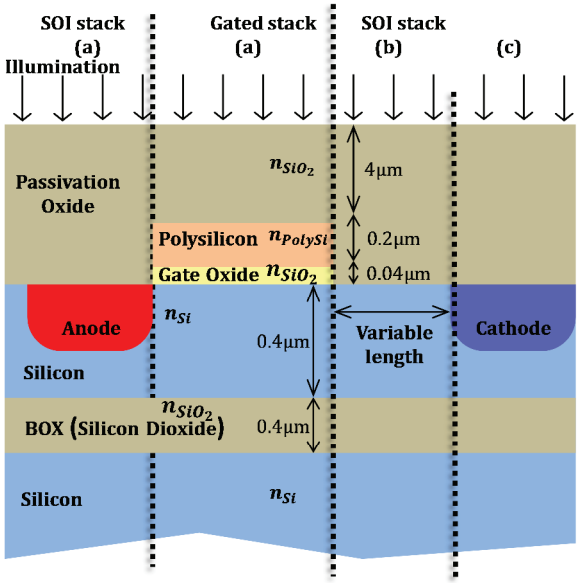

Fig. 9. SOI-MOS-PN photodetector structure used in TCAD and its different illumination regions: (a) for gate and anode side illumination; (b) for central illumination and (c) for cathode side illumination. TCAD simulations are shown in Fig. 10.

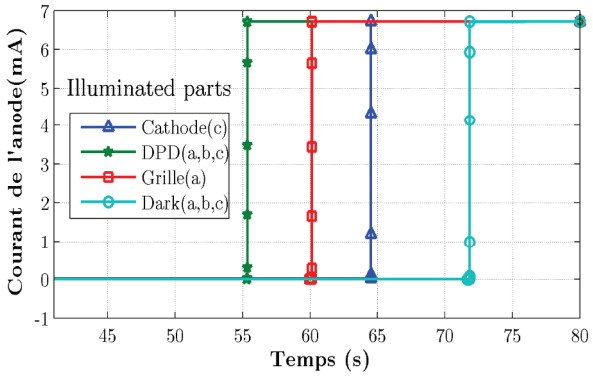

Fig. 10. TCAD simulation of the anode current versus time in dark and after the illumination of the different parts of the SOI-MOS-PN structure shown in Fig. 9.

The effective number of photo-generated electron-hole pairs (n_{phot}) can be expressed in terms of the triggering time (T_{trig}) and total number of integrated charges required for triggering ($N_{tot}=Q_{ref}/q$) as [4]:

$$n_{phot} = N_{tot}\left(\frac{1}{T_{trig}} - \frac{1}{T_0}\right) \tag{4}$$

where $T_0 = \frac{N_{dark}}{n_{dark}}$ is the self-triggering time.

The number of efficient photo-generated electron-hole pairs participating to the triggering could, therefore, be estimated by simulating the triggering time for each configuration. In fact, the electron-hole pairs generated in or close to the depletion region (e.g. (a) in Fig. 9) are separated by the electric field. The electrons drift quickly under the gate, creating an inversion layer that shields the electric field coming from the gate, thereby decreasing the MOS depletion region and gradually de-isolating the anode, which in turn increases the hole current and lowers even more the cathode barrier.

The positive feedback is thus created, turning the device into its conductive state. However a part of the electron-hole pairs generated in the zones where no electric field exists will recombine immediately and thus will not participate to the triggering.

TCAD simulations, shown in Fig. 10, reveal that, for the same surface, the illumination of the regions (a) and (b) of the SOI-MOS-PN photodetector of Fig. 9 result in practically the same triggering time. The illumination of the region (c), on the other hand, results in a triggering time close to the dark triggering T_0. From this analysis we can estimate that the poly-gate effect will deteriorate the effective photo-generated electron-hole pairs (n_{phot}) by about 40 to 50 %. The signal to noise ratio of a MOS-PN photodetector can be expressed as [11]:

$$SNR = \frac{\sqrt{N_{tot}}}{\frac{n_{dark}}{n_{phot}} + 1} \tag{5}$$

where n_{dark} the dark carrier generation by temperature and cathode leakage [charges/s]

This equation reveals that the poly-gate absorption will decreases the SNR by about two. This detrimental effect is, however, compensated by the elimination of leakage current and thus the attenuation of n_{dark} in SOI implementations.

It is worth noting that the triggering time increases by about three orders of magnitude for SOI-MOS-PN photodetector (Fig. 10) in comparison to Bulk-MOS-PN photodetector (Fig. 7). This huge difference is only due to the elimination of the leakage in SOI implementation.

IV. Conclusion

This paper analyzed the advantages of SOI based photodetectors in the case of low-light and narrow spectrum imaging. Notably, it is demonstrated that the active area of the photodetector acts as a resonating cavity that increases the absorption level for specific wavelength while decreasing it for others. It acts therefore as a spectral filter. The application of SOI technology to the hybrid MOS-PN sensor was then discussed. Principally, the advantages in terms of crosstalk and leakage current were explained. The diminution in dark current translates into an increase in SNR.

References

[1] H. Eltoukhy, K. Salama, and A. El Gamal, "A 0.18-µm CMOS bioluminescence detection lab-on-chip," *IEEE J. Solid-State Circuits*, vol. 41, no. 3, pp. 651–662, Mar. 2006.

[2] D. Ho, M.O. Noor, U.J. Krull, G. Gulak, "CMOS Tunable-Color Image Sensor With Dual-ADC Shot-Noise-Aware Dynamic Range Extension," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 8, pp. 2116-2129, Aug. 2013.

[3] R. R. Singh, B. Li, A. Ellington, and Arjang Hassibi, "A CMOS Σ-Δ Photodetector Array for Bioluminescence-Based DNA Sequencing," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2011, pp. 96-97.

[4] D. Sallin, A. Koukab, and M. Kayal, "Hybrid MOS-PN photodiode with positive feedback for pulse-modulation imaging," *Opt. Express,* vol. 22, no.12, pp. 14441-14449, Jun. 2014.

[5] D. Sallin, A. Koukab, and M. Kayal, "MOS-PN Hybrid Device with Minimum Dark Current for Sensitive Digital Photodetection," *IEEE Photon. Technol. Lett.*, vol. 26, no. 20, pp. 2062-2065, Oct 2014.

[6] M. Born and E. Wolf, *Principles of Optics* MacMillan, NewYork, 1964, p. 254.

[7] Z. Knittl, *Optics of Thin Films,* Wiley, London, 1976, p. 41.

[8] M. G. Moharam, T. K. Gaylord, D. A. Pommet, and E. B. Grann, "Stable implementation of the rigorous coupled-wave analysis for surface-relief gratings: enhanced transmittance matrix approach," *J. Opt. Soc. Am. A*, vol. 12, no. 5, pp. 1077-1086, May 1995.

[9] D. Sallin, A. Koukab, and M. Kayal, "Toward direct light-to-digital conversion using a pulse-driven hybrid MOS-PN photodetector," *Opt. Lett.,* vol. 40, no.4, pp. 669-672, Feb. 2015.

[10] D. G. Chen, D. Matolin, A. Bermak, C. Posch, "Pulse-Modulation Imaging – Review and Performance Analysis", *IEEE Trans. Biomed. Circuits Syst*., vol. 5, no. 1, pp. 64-82, Feb 2011.

[11] D. Sallin, A. Koukab, and M. Kayal, "Design of a Direct Light to Time Converter and its Noise Analysis," in *IEEE Proc. of the 21st International Conference on Electronics Circuits and Systems—ICECS2014*, Marseille, France, Dec. 7-10, 2014.

Nisrina Abdo received the master's degree in electrical engineering from the University of Toulouse in 2011. She is currently pursuing the Ph.D. degree in the University of Toulouse. During her PhD, she did a doctoral internship in EPFL electronic lab of Lausanne. Her research focuses on SOI technology applications to CMOS image sensors, with a particular focus on optical effects.

Denis Sallin received the B.Sc. degree in electrical engineering in 2009 and the M.Sc. degree in electronics and microelectronics in 2011, both from the École polytechnique fédérale de Lausanne (EPFL), Switzerland. In 2012, he joined the Electronics Laboratory (Elab) of EPFL in order to pursue a PhD degree under the supervision of prof. Maher Kayal. His current research interest are photosensors and front end-circuits as well as mixed-signal electronics. He received the PhD in 2016.

Adil Koukab received the M.S. degree (DEA d'Opto-Electronique) from the University of Nancy, France, in 1993 and the Ph.D. degree in electrical engineering from the University of Metz and Supélec, France, in 1997. He is currently a Research Associate with the Department of Electrical Engineering of the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland.

Magali Estribeau (M'11) received the M.S.(2000) and Ph.D. (2004) degrees in E.E from SUPAERO, Toulouse. She is currently a Research Scientist with the ISAE Image Sensor Research Team. Her research interests focus on solid-state image sensors and include analysis and modeling of charges collection, sensitivity and image quality, radiation effects on charge collection and transfer, and electro-optical performances characterization methods development.

Pierre Magnan (M'99) received the degree in electrical engineering from the University of Paris, in 1980. After being a Research Scientist involved in analog and digital CMOS design up to 1993 in LAAS-CNRS, he moved to image sensors research in SUPAERO, now called the Institut Suprieur de l'Aronautique et de l'Espace SUPAERO, Toulouse, France. Since 2002, he is a Full Professor and the Head of Image Sensor Research Group involved in CMOS image sensor basic and applied research. He has supervised 15 Ph.D. students and co-authored over 70 scientific papers. He has served in the IEEE IEDM Display Sensors and MEMS Subcommittee in 2011 and 2012 and the International Image Sensor Workshop (IISW) TPC in 2007, 2009, and 2011, being the General Technical Chair of 2015 IISW

Maher Kayal received M.S. and Ph.D degrees in electrical engineering from the Ecole Polytechnique Fédérale de Lausanne (EPFL, Switzerland) in 1983 and 1989 respectively. He has been with the Electronics laboratories of the Ecole Polytechnique Fédérale de Lausanne (EPFL, Switzerland) since 1990, where he is currently a professor and director of the "Energy Management and Sustainability" section. He has published many scientific papers, coauthor of three text books dedicated to mixed-mode CMOS design and he holds 10 patents. His technical contributions have been in the area of analog and Mixed-signal circuits design including highly linear and tunable sensors microsystems, signal processing and green energy management.