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DC LINK CONDITION MONITORING METHOD FOR TWO-LEVEL AC/DC/AC CONVERTERS*

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Abstract: Power electronics is one of the most important elements of today's industry. Many of converters applications are being considered as critical for plant production process. Offering enhanced functionality in modern AC drives is a way to gain a competitive advantage in power converters market. One of the values to the customers comes from low cost condition monitoring of critical equipment and from optimized maintenance costs. DC bus is one of the elements of power converters. Although the designers pay a lot of attention when designing DC-link circuit, breakdowns and failures of the DC circuit components can still happen. Unfortunately this means that the whole converter must be shut down in emergency mode to be repaired. Nowadays, monitoring of the bus capacitor is becoming one of the desired features from customer side, as well as from the converter manufacturer. Proposed approach presents a method which assures the online evaluation of the equivalent series resistance (ESR) of a DC-link capacitor. The ESR increase trend is an important indicator of accelerated aging process or incoming failure of the capacitor. The important feature of the proposed condition monitoring method is that it does not require any additional sensors. For estimation purposes already installed sensors and other internal converter's signals are used. Particularly the method employs the DC-link voltage measurement with the DC-link current reconstruction.

Keywords: *DC link, condition monitoring, AC/DC, power electronics, converter*

1. INTRODUCTION

Condition based monitoring has become one of the drivers for developing new sophisticated maintenance services. The industry requirements towards electronic equipment are more and more demanding, the need for modern condition monitoring is rising [9]. Assuring rapid faults discovery, preventive maintenance, failure foreseeing are slowly becoming a standard approach for many of the devices and applications. For frequency converters, which in many cases are being considered as critical for plant production process, offering enhanced functionality in modern ac drives is a way to gain a competitive advantage in power converters market.

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The ever-increasing demands for greater efficiency and reliability of variable frequency converters, force the introduction of novel methods for improving their performance. One of the values for the customers comes from low cost of critical equipment of condition monitoring and from optimized maintenance costs. DC link is one of the elements of power converters circuits [1, 2]. Although the designers pay a lot of attention when designing DC link, breakdowns and failures of the DC link can still happen. Unfortunately this means that the whole converter must be shut down in emergency mode to be repaired.

Nowadays, monitoring of the DC link is becoming one of the desired features from customer side, as well as from the converter manufacturer. One of the ways is to provide a detailed condition monitoring features for the elements of the converter, ensuring tracking of entire device status. Assuring proper monitoring of the DC link capacitance level is one of the solutions for converter status determination. The capacitor deterioration usually is manifested by an increase in ESR (equivalent series resistance) and decrease in an effective capacitance. Earlier detection of the ESR change allows preventive mitigation actions, i.e. scheduling shutdown and repairs. Moreover it also helps with evaluation of the expected operational time until failure may happen. Preventing the growth of ESR values over a specified level provides maintaining the quality of converted power and protects the converter from DC-link failure.

2. DESCRIPTION OF THE METHOD

The proposed algorithm is based on determination of equivalent series resistance of the converter DC link. The ESR is the total ohmic resistance that contributes to power loss, represented by a single resistance in series with the ideal capacitor. Typically given at 25 °C at 10 kHz and 100 kHz in units of milliohms. The value of the ESR depends on many different factors:

- capacitor type (electrolytic, ceramic etc.),
- capacitor rated voltage and capacitance,
- ambient temperature and possible cooling,
- ac spectrum frequency and ripple current,
- mechanical stresses/vibration and shock
- mechanical shape/dimensions/connections.

There are of course unwanted phenomena such as overvoltage, overcurrent, dynamic charging and discharging. The overall aging process is strictly non-linear, which shows the difficulty in exact determination of the future ESR value and remaining life of the capacitor. The manufactures provide tables or figures on the capacitor aging, ESR determination assuming constant, non-disturbing aging process. The resistance is obtained by means of DC link voltage and current. The DC voltage is measured directly on the

whole DC link and current is being reconstructed, thus no additional sensors are required. Knowing the switching function values and measuring the input and output three phase current, it is possible to reconstruct the converters DC currents. For the rectifying part the formula is as

$$I_{\mathrm{REC}} = S_{\mathrm{aREC}} I_{\mathrm{aREC}} + S_{\mathrm{bREC}} I_{\mathrm{bREC}} + S_{\mathrm{cREC}} I_{\mathrm{cREC}} \tag{1}$$

where S_{aREC}, S_{bREC}, S_{cREC} are corresponding legs switching functions, and I_{aREC}, I_{bREC}, I_{cREC} are corresponding measured rectifier phase input currents. For the inverting part, the formula is as follows

$$I_{\mathrm{INV}} = S_{\mathrm{aINV}} I_{\mathrm{aINV}} + S_{\mathrm{bINV}} I_{\mathrm{bINV}} + S_{\mathrm{cINV}} I_{\mathrm{cINV}} \tag{2}$$

where S_{aINV}, S_{bINV}, S_{cINV} are corresponding legs switching functions and I_{aINV}, I_{bINV}, I_{cINV} are corresponding measured inverter phase output currents. For checking the accuracy of DC current reconstruction, an example of measured and reconstructed rectifying unit DC current can be seen in Fig. 1. As is seen in the figure, the reconstruction works very well. The reconstructed signal is shifted by one cycle.

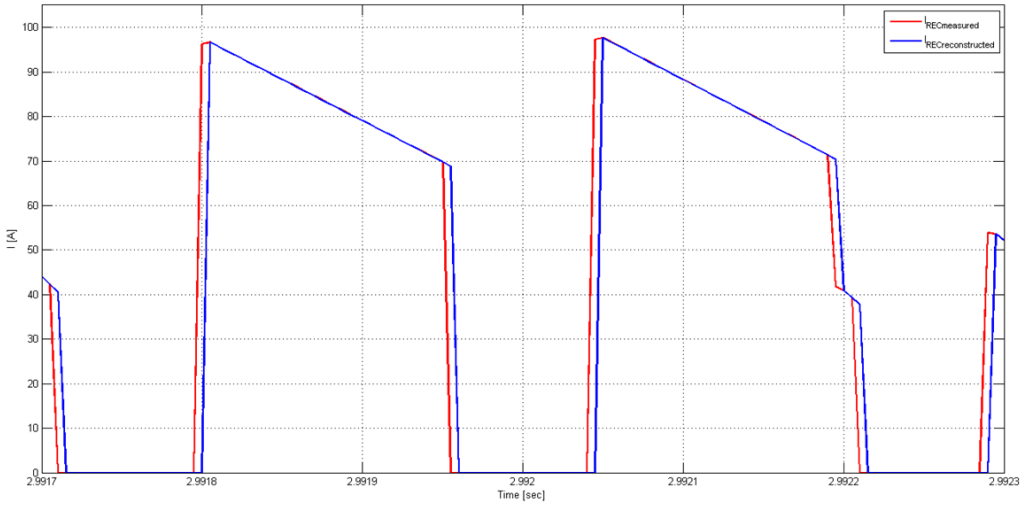

Fig. 1. Measured and reconstructed rectifying unit currents

The proposed method which has been submitted as patent [10] allows monitoring DC link state using internal measurements of the converter. By this method, the calculation process is simplified and thus does not require a significant calculation power. Also by using synchronization with the inverter switching signal, further simplification in software by reducing algorithm complexity and in hardware by reducing number of elements is achieved.

2.1. DIAGNOSTIC PRINCIPLE

The developed monitoring method is an advantageous in relation to the common, existing methods [3, 4] as it allows monitoring of the DC link using fewer number of measurements inside the power converter, namely only DC link voltage measurement. Moreover the method provides simplification in the calculation process, and thus it does not require a significant calculation power. The use of synchronization with inverter switching signal can further simplify software by reducing algorithm complexity.

The algorithm starts from measuring a DC link voltage U_{DC} and measuring three phase I_a, I_b, I_c input current of the power electronic converter. The next step is to take the calculated inverter switching signals S_{aINV}, S_{bINV}, S_{cINV} of the inverter unit and rectifier switching signals S_{aREC}, S_{bREC}, S_{cREC} of the rectifier from the converter control unit. The switching signals may come from measurements by known control methods such as: field oriented control method, scalar control method, direct torque control method etc. The method is independent of the control strategy. The switching signals can take the following values, as in

$$S_{aREC} = \begin{cases} 1, \\ 0 \end{cases} \qquad S_{bREC} = \begin{cases} 1, \\ 0 \end{cases} \qquad S_{cREC} = \begin{cases} 1, \\ 0 \end{cases}$$
$$S_{aINV} = \begin{cases} 1, \\ 0 \end{cases} \qquad S_{bINV} = \begin{cases} 1, \\ 0 \end{cases} \qquad S_{cINV} = \begin{cases} 1, \\ 0 \end{cases} \tag{3}$$

where S_{aREC}, S_{bREC}, S_{cREC} are switching signals for each of the legs of the rectifier part of the converter and S_{aINV}, S_{bINV}, S_{cINV} are switching signals for each of the legs of inverter part of the converter. The next step is to compare each individual switching signal of inverter unit with all remaining switching signals, and when

$$S_{aINV} = S_{bINV} = S_{cINV} \tag{4}$$

Then triggering signal $S_{TRIG} = 1$ is generated. After that, the determination of triggered time duration t for the trigger signal S_{TRIG} is performed, where triggered time duration t is defined as the time between start T_{on} and stop T_{off} of the trigger signal S_{TRIG} (Fig 2) and described according to the formula

$$T_{on}(k) < t < T_{off}(k) + \ldots + T_{on}(k+1) < t < T_{off}(k+1) \tag{5}$$

where k till n are consecutive numbers of triggered time duration t. Knowing the time, one can determine the switching signals S_{aREC}, S_{bREC}, S_{cREC} of the rectifying unit from the converter control at the triggered time t as $S_{aREC}(t)$, $S_{bREC}(t)$, $S_{cREC}(t)$ and measure the DC link voltage U_{DC} and converter input currents I_a, I_b, I_c of at the triggered time t as $U_{DC}(t)$, $I_a(t)$, $I_b(t)$, $I_c(t)$. The next step is the DC link current reconstruction according to the formula

$$I_{DC}(t) = S_{aREC}(t) I_a(t) + S_{bREC}(t) I_b(t) + S_{cREC}(t) I_c(t) \tag{6}$$

where $I_{DC}(t)$ is the reconstructed DC link current at the triggered time t and $S_{aREC}(t)$, $S_{bREC}(t)$, $S_{cREC}(t)$ are switching signals of rectifying unit at time t and $I_a(t)$, $I_c(t)$, $I_b(t)$ are converter input currents at time t.

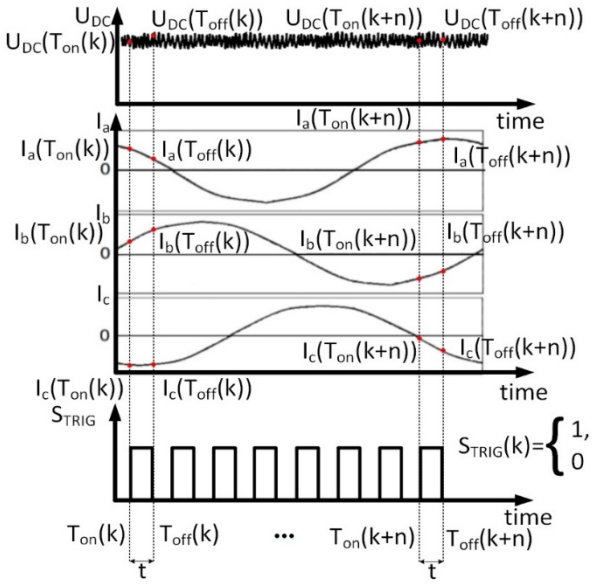

Fig. 2. Determination of the trigger signal S_{TRIG}

Then then ESR value can be calculated using

$$ESR(t) = \int_{T_{on}}^{T_{off}} \left(\frac{\frac{dU_{DC}(t)}{dt} - \frac{I_{DC}(t)}{C_{init}}}{\frac{dI_{DC}(t)}{dt}} \right) dt \tag{7}$$

where $I_{DC}(t)$, $U_{DC}(t)$ are the DC link current and voltage measured at the triggered time t, C_{init} is the initial DC link capacitance stored in the converter control unit and T_{on}, T_{off} are the start and stop time of the triggered signal S_{TRIG}. Subsequently, the total DC link capacitance C (expressed as a percentage value) is calculated using the equation

$$C = \frac{\left(I_{DC}(t) ESR(t) - U_{DC}(t)\right)^2}{U_{DC}^2(t)} \times 100\% \tag{8}$$

where $I_{DC}(t)$, $U_{DC}(t)$ are the DC link current and voltage measured at the triggered time t, ESR(t) is the determined equivalent series resistance. After that the obtained value of the capacitance is compared to the initial DC link capacitance, as in

$$C < k_p C_{init} \tag{9}$$

where the value of k_p is a threshold value given by user dependent on a nominal power of the converter and capacitor types. If the inequality (9) is true, than an alarm is generated and a command is send to set the switching signals S_{aREC}, S_{bREC}, S_{cREC} of the rectifier and switching signals S_{aINV}, S_{bINV}, S_{cINV} of the inverter to 0, which signals automatically switch off the converter.

2.2. FULL SCALE CONVERTER

Knowing the exact values of rectifying and inverting unit currents (both coming from reconstruction, not measurements), one can easily calculate the DC link current at each time instant. The formula for the DC link current is

$$I_{cap} = I_{REC} - I_{INV} \tag{10}$$

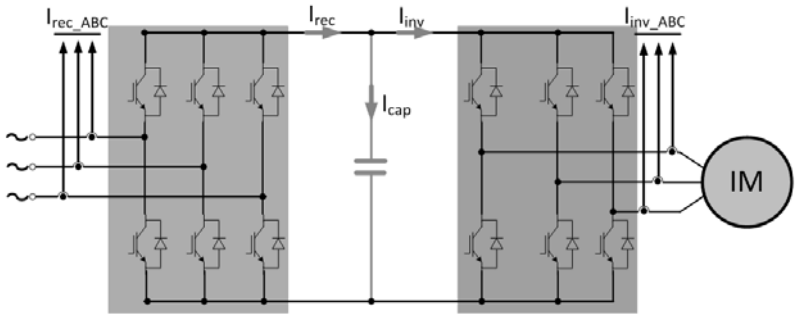

Fig. 3. Current flow in case of having a full-scale converter

Taking into account that this method needs measurements of the inverter and rectifier unit phase currents (which are available in most of the cases), simplification of the proposed solution can be considered. Reconstructing the currents in a time instant of zero voltage vectors (switching states are the same – all 0 or 1) appearance of one of the units (rectifying or inverting) allows using measurements of one unit only (namely the input currents of the rectifying unit). In this case, only three phase input currents are measured. The DC link current is obtained from the relation: $I_{cap} = I_{REC}$.

2.3. CONVERTER WITH A DIODE RECTIFIER

Having an uncontrolled rectifying part (diode rectifier) results in lack of knowledge of the diode switching states. In reality, it is possible to determine the diode switching

states by the means of using the grid angle. Having in mind that the drive has to be synchronized to the grid, one can explicitly assume that the information on the grid value is available.

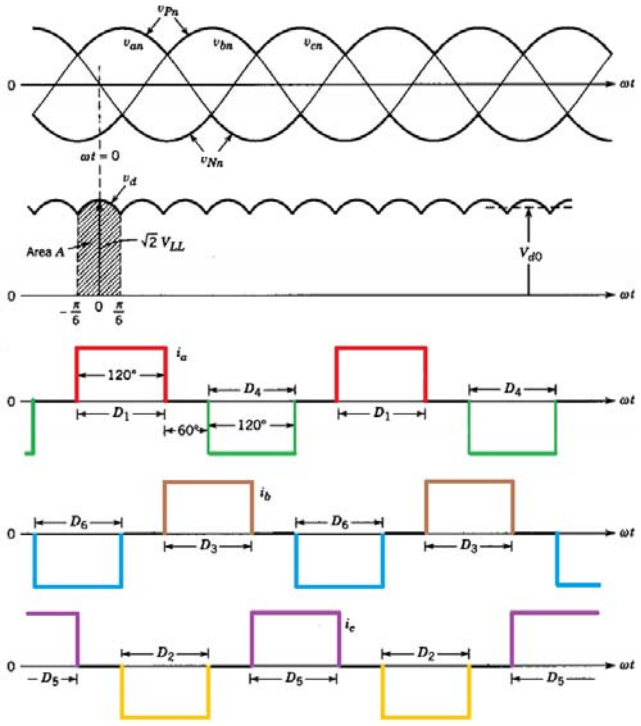

Fig. 4. 6-pulse diode rectifier conducting scheme [5]

When the grid angle is known, and the input inductance is ignored, and the DC-side current is assumed to flow continuously. One can state that diodes 1, 3, 5 belong to upper group and the diodes 4, 6, 2 belong to the lower group. To facilitate the flow of the DC current at least one diode from each group must conduct. In the upper group all of the diodes are connected via their cathodes. This yields that the diode connected to the most positive voltage will conduct and the other two will be reversed biased. In the lower group, the diodes are connected through their anodes. As a consequence, the diode connected to the most negative voltage will conduct and the other two will be reverse biased. Each diode, based on the description above, conducts during 120° (Fig. 3). The diodes in Fig. 4 are numbered in a fashion representing sequential conduction mode: 1, 2, 3 and so on. It is obvious that having information on the voltage angle, it is possible to determine the exact switching state of each diode. Switching states are summarized in Table 1. Also in this case the reconstruction of the DC link current works well.

Table 1. Switching states depending on the angle

Angle	Switching states		
	S_a	S_b	S_c
$\theta \in (-60°, 60°)$	1	0	0
$\theta \in (60°, 180°)$	0	1	0
$\theta \in (-180°, -60°)$	0	0	1

3. SIMULATION

For validation of the algorithm, a proper simulation model has been conducted where ESR was time dependent. The increase of the DC link ESR is simulated by artificially adding a resistance connected in series with the DC link.

3.1. CONVERTER WITH A DIODE RECTIFIER

The deterioration of the DC link capacitance can be expressed by increase of internal series resistance [5, 6]. The time dependent equation describing the growth of ESR is as follows [6]

$$\frac{1}{ESR(t)} = \frac{1}{ESR(0)}\left(1 - kte^{-4700/(T-273)}\right) \tag{11}$$

where, T – aging temperature, K, t – aging time, ESR(0) – ESR resistance at time $t = 0$, k – a constant dependent on design and construction of the capacitor. It is known that during the entire lifecycle of the capacitor, the internal resistance is considerably increasing [7]. The usefulness of the capacitor, its life time is considered complete when its capacity falls below the 75% threshold [8]. For simplicity, in power converter applications, the impedance of the DC link module can be derived from the abridged equation [6]

$$Z = ESR + j\omega ESL + \frac{1}{j\omega C} \approx ESR \tag{12}$$

The stray inductance and capacitance components are being neglected. The above assumptions lead to the following expression]

$$u_{C,\,ac} = ESRi_C \tag{13}$$

In summary, the increase in the ESR can be reflected as a continuous capacitor resistance increase. For the simulations, this approach is realized by setting a predefined resistance value to be added in series with the capacitor during the simulation time [5, 6]. In the case of experiments, the approach is similar – additional resistance is connected in series with the DC-link capacitance.

3.2. SYSTEM CHARACTERISTICS

Depending on the application needs, there are different types of converter topologies but for the purpose of this investigation, a grid connected full scale converter topology was used. The model of the system consists of a 15 kV power grid source, a coupling transformer, a power converter divided into three subparts (a rectifying power unit, a DC link, and an inverting power unit) and a load. The chosen solution to be modeled as an example is a traction converter, but other systems such as a wind power turbine could also be considered.

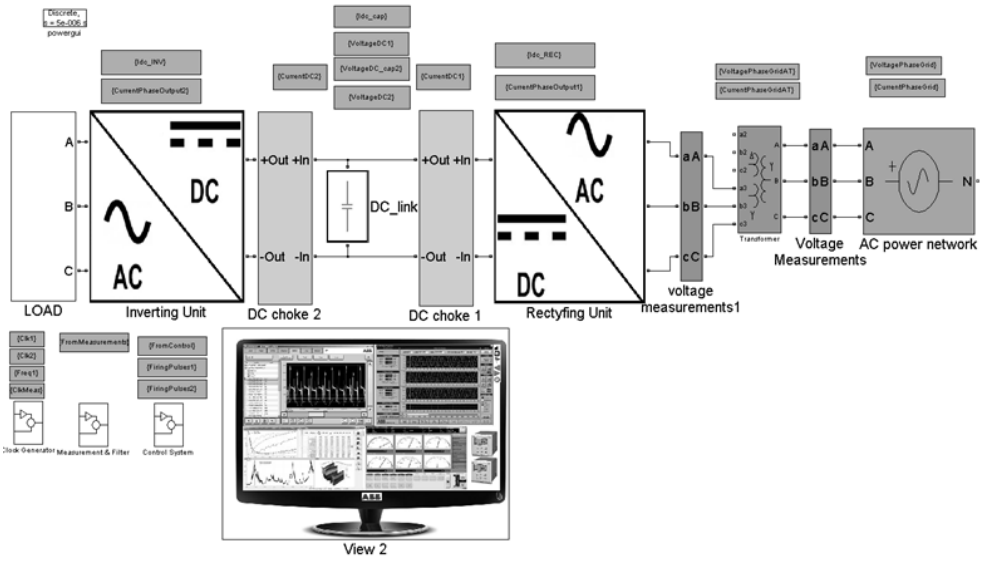

Fig. 5. System model in Simulink

The task of the rectifying power unit is to keep the DC link voltage at a constant reference level, while the inverting unit purpose is to provide a sufficient amount of the AC load current as required by the application. The control of the converter is designed and realized in a synchronous reference frame. This allows using PI controllers for the rectifying part, the DC link voltage control and the inverting unit control. Since the purpose of this work was to focus on the condition monitoring for DC link part of the converter, the control strategies will not be discussed any further. Figure 5 presents the outline of the Simulink simulation. The increase in the ESR is simply modeled as a steady capacitor resistance increase. This is done by setting a predefined resistance value to be added in series with the capacitor during the simulation time [6, 7]. All the main components are modeled using standard blocks available in Simulink SimPower System Library (including semiconductor devices).

3.3. RESULTS OF SIMULATION

The validation of the method has been performed as follows. The load has specific current demand (30% of the rated current). To fulfill this demand, the converter is transferring power from the grid to the load, sustaining required level of the DC voltage. While running, an increase in DC link ESR occurs. This performed as a step change rise of the resistance value at defined time of simulation. Figure 6 presents the results of the simulation. It can be observed that the algorithm is able to track the increase of the DC link ESR. The response time for the calculation of the ESR value during a step change of resistance is 25 ms and the error is around ±1%.

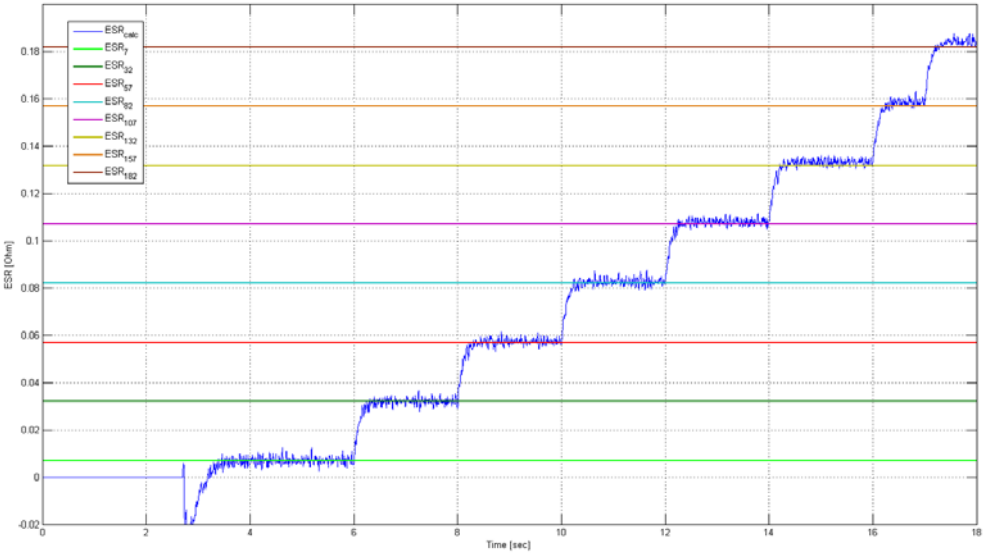

Fig. 6. The determined DC link ESR (compared to actual added resistance)

Taking into account the above figure one can state that this method gives accurate, and thus acceptable results. However the performance of the algorithm should be verified during experiments – what is showed in the next section of this article.

4. EXPERIMENTAL VERIFICATION

This section focuses on providing information on performed verification tests for the developed algorithm of the DC link condition monitoring. It introduces and explains in details how the experimental test stand was constructed, how the algorithms were implemented, and discusses the obtained results.

4.1. DESCRIPTION OF THE SYSTEM

Figure 7 presents a detailed overview of the used experimental test rig. The construction of the test stand follows the best practices in designing voltage inverters.

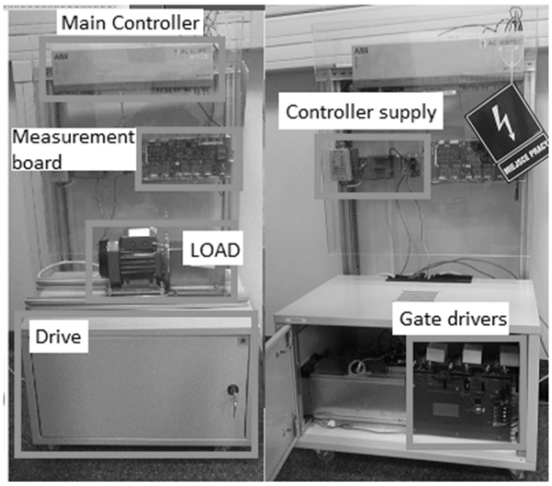

Fig. 7. the test rig – an overview

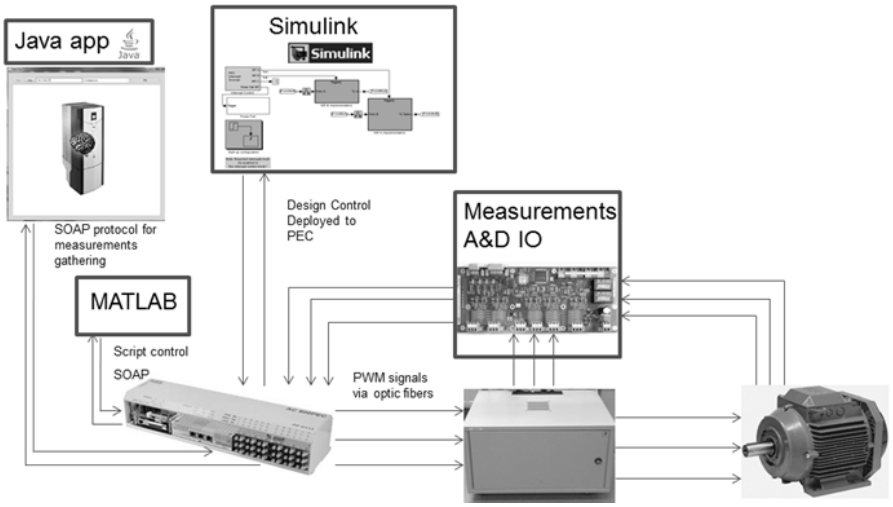

Fig. 8. Data flow in the system

The core of the unit is a powerful AC800PEC controller which introduces programing paradigm which is common in the ABB. The control hardware is split into two parts. The former one is a standard PowerPC processor and the latter – Virtex-II FPGA. This

structure allows one to split subroutines into two categories. The former one is fast functions and procedures which can be executed within nanoseconds. That part is harDCoded in VHDL or Verilog languages. This part covers both protection circuits and communication modules. The latter part is a regular microprocessor which performs general program with subroutines executed within microseconds. The program can be written in any language but by the choice of constructors the Simulink/MATLAB platform was selected as the developing environment. This solution gives high flexibility to create algorithms in well-established framework and graphical environment. The controller is capable to control gate drivers of the inverter transistors which fulfils the controllable part of the device. The rest – measurement interface is fulfilled by the MI board which can work with industrial-type current sensors – LEMs.

That covers the integration of the controller with real signals. The flow of operation is presented in Fig. 8.

4.2. RESULTS

The values of resistance added to converter DC link are given in Table 2, where also the estimated values of ESR have been compared with the expected value. The values within the table have been calculated taking into account the performance of the algorithm. It is clearly visible that the ESR depends on the resistor inserted in DC-link.

Table 1. Switching states depending on the angle

Ordinal number	Added resistance [ohm]	Estimated value [ohm]	Expected value [ohm]
ESR_1	0	0.15	–
ESR_2	0.02	ca. 0.18	0.17
ESR_3	0.03	ca. 0.185	0.18
ESR_4	0.11	ca. 0.23	0.26
ESR_5	0.42	ca. 0.52	0.57

It can be assumed that the value of ESR in the first test (lowest) is the initial resistance (ESR1). This value will serve as a base value for other test points. The unwanted phenomena, such as overvoltage, overcurrent, dynamic charging and discharging, introduce additional difficulties. The overall aging process is strictly non-linear, which shows the difficulty in exact determination of the ESR value. Nevertheless, the proposed method allows determining the increase in ESR in the easiest way.

The maximum relative error is 11%. It is assumed that taking into account only few points in accuracy determination may improve the relative performance (i.e., the resistors accuracy). By the method, one of the simplest, but reliable approaches has been adopted based on simple relation presented in Eq. (7). The results are satisfactory.

4.3. DISCUSSION

There are many different methods for DC link condition monitoring, which have been developed in recent years – a comprehensive list of methods and approaches can be found elsewhere [11]. Le et al. [12] proposed an online estimation scheme for the ESR of the DC-link capacitors in AC machine drive systems. The regenerative operation of the machine is utilized, which increases the DC-link voltage, causing blocking the diode rectifier. Then, the DC-link current can be directly calculated based on the stator currents and the switching times of the VSI. Injecting the AC regulated current component into the q-axis stator current induces AC current and voltage components in the DC link as well as in the ESR of the capacitor, where the RLS algorithm is applied to achieve a reliable estimation of the ESR. A simple offline monitoring technique is presented in [13], where signal generator is injecting known waveform to the DC circuit and measurements are performed using an oscilloscope. A condition monitoring method based on artificial neural network (ANN) algorithm is shown in [14].

The paper presents a monitoring method, which is simplified by means of used sensors and implementation (similar to that by Le et al. [12] but without focusing on regenerative operation and injection of AC regulated current). It is shown that for accurate ESR determination by DC voltage measurement (which is currently available) and DC-link current measurements or reconstruction are needed. In many cases, DC-current measurements in the converter are not available. It is assumed that three phase current measurement are available in protective relays that are installed before the drive. The advantage of the solution lies in the fact that the ESR can be determined while the converter is in operation.

5. CONCLUSIONS

The aim of this paper was to present a developed method for monitoring DC link capacitance in power converters. The approach implies using a DC link ESR as a health condition indicator. Classical approach is to measure the DC link current and DC link voltage. The proposed solution is based on DC-link voltage and input current measurements, measured anyway for control purposes. The DC link current is obtained by means of current reconstruction. It has been proven that the developed DC-link monitoring method can be implemented in an easy manner and that it can bring sufficient performance in terms of DC-link ESR monitoring. In future, studies on improvement of the method should be conducted consisting in decoupling the algorithm from disturbances appearing in the DC link voltage and current or on use this information as an additional disturbance indicator.

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