Analysis and Design of a Chopped Current Mode Instrumentation Amplifier

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***Abstract*—This paper presents the design of a chopper stabilized current mode instrumentation amplifier and analyzes the performance limitations imposed by chopping technique in detail. The amplifier targets to be the read out circuitry of a high precision temperature sensor. Since the required bandwidth in this kind of applications is very low, nested chopping technique is used to provide continuous offset reduction and eliminate $1/f$ noise. The amplifier is designed in 0.18μm CMOS process. The resulting input referred noise is $20nV/\sqrt{Hz}$, the offset is $582nV$ and the CMRR exceeds 110dB. The power consumption of the total design is 420μW.**

***Index Terms*—Current mode instrumentation amplifier, nested chopping, chopping improvements.**

I. Introduction

ADVANCES in IC processing lead to the need of very accurate interface circuits for analog signal processing. From an economical point of view, standard CMOS technology is the preferred technology for designing sensors, since it is relatively low cost. However, these sensors tend to have lower sensitivity than those implemented in specialized sensor technologies. Therefore, the need for designing precise and reliable instrumentations amplifiers is of great concern.

A major disadvantage of instrumentation amplifiers is DC offset, which deteriorates the total performance of the whole system. The input offset of the amplifier determines the minimum detectable signal, degrades its noise performance and increases the non-linearity [1]. One of the widely used methods to drastically minimize the effects of the input offset is chopping technique.

Conventional instrumentation amplifiers based on voltage operational amplifier topology exhibit gain dependent bandwidth and common mode rejection ratio (CMRR), due to the fixed gain bandwidth product of the operational amplifier. Moreover, these topologies require precise resistor matching to achieve high CMRR [2], [3]. Better performance with respect to frequency range of operation, CMRR and matching issues provide the current mode instrumentation amplifiers [4]- [6].

Current mode circuits are excellent alternatives to voltage mode circuits. If the information is conveyed as a current, the square root in MOS transistor circuits is proportional to the square root of the signal, if saturation region operation is assumed for the devices. Furthermore, all nodes are near virtual ground resulting to low impedance at each node and then very small time constants and high values of parasitic poles. For these reasons, the current mode approach leads to simpler circuit realization and lower power consumption. For taking advantage of these benefits, a current mode instrumentation amplifier is proposed and examined in this work.

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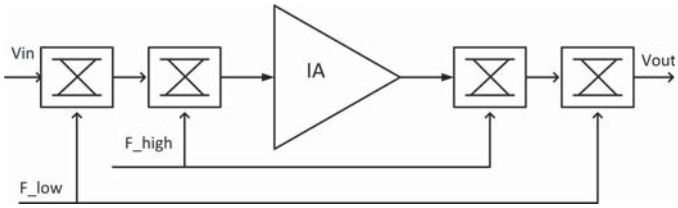

Fig. 1. Nested chopped current mode instrumentation amplifier

The outline of this paper is as follows. In Section II, we explain the principle of nested chopping technique and the noise performance of the instrumentation amplifier. Section III describes the source of the residual offset and design improvements. The proposed circuit and post-layout results are presented in sections IV and V, respectively. Conclusions are drawn in Section VI.

II. Theory of Operation

A. Nested Chopping Technique

One way to reduce low-frequency noise and residual offset is the nested chopping technique. In this technique, the input signal is modulated twice by two square wave signals mixing it to the odd harmonics of the chopping frequencies. The choppers are implemented by a set of switches, which surround the amplifier, as shown in Fig. 1. The inner choppers significantly suppress the inherent offset and 1/f noise by modulating them to a high chopping frequency where the unwanted signals are separated from the desired signal. In this contribution, the outer choppers further reduce the remaining residual offset by modulated it to a lower chopping frequency. In our work we apply nested chopping to an instrumentation amplifier to demonstrate the effectiveness of this technique also in current mode circuits.

B. Noise considerations

A typical noise power spectrum for CMOS amplifiers becomes Gaussian at high frequencies (thermal noise) whereas for low frequencies the noise spectrum is characterized by flicker (1/f) noise. The frequency at which the flicker noise becomes dominant over thermal noise is called the 1/f noise

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corner frequency. The input referred noise spectral density for a MOSFET is given by [7]:

$$u_{ni}^2(f) = 4kT\frac{2}{3}\frac{1}{gm} + \frac{K_f}{WLC_{ox}f} \quad (1)$$

The first part of the sum refers to thermal noise and the second part to the flicker noise. From the Eq. 1 we can derive that the thermal noise contribution is inversely proportional to the MOSFET transconductance gm. As the thermal noise remains after chopping performance uninfluenced, a lower level of thermal noise can be achieved by sizing the input transistors with a very high (W/L) ratio as well as biasing them in weak inversion.

The noise power spectral density (PSD) after chopping is given by [8]:

$$S(f) = A_o^2(\frac{2}{\pi})^2\sum_{-\infty}^{+\infty}\frac{1}{n^2}S_n(f - nf_{chop}) \quad (2)$$

where Ao is the amplifier gain, and fchop is the chopping frequency. The lower level of output PSD is achieved by choosing the chopping frequency to equal the amplifier corner frequency.

The contribution of the 1/f noise to the total output noise PSD is given by the following expression [8]:

$$S_{\frac{1}{f}}(f) = (\frac{2A_o}{\pi})^2\sum_{-\infty}^{+\infty}\frac{1}{n^2}\frac{S_o f_o}{\mid f - nf_{chop} \mid} \quad (3)$$

So denotes the wideband thermal noise floor. Eq. 3 reveals that the first order aliased components carried the most noisy aliased noise. In our implementation the noise corner frequency was observed approximately at 100kHz and thus the high chopping frequency selected to be at this value. Finally the baseband noise of chopper amplifiers is almost equal to the wideband white noise [9]. Also the chopping frequency should be greater than twice the bandwidth of the input signal.

III. Sources of Offset in Chopped Amplifier

Chopping technique has been proved that is an effective technique to tackle the input offset problem and minimize the 1/f noise, however, the non-idealities in the total system limits the offset performance. In this section we discuss the potential sources of residual offset.

A. Charge injection spikes from choppers

The residual offset of a chopper amplifier originates mainly from the non-idealities of the input modulators [10]. The clock feedthrough introduced by the switches in the input modulators is the dominant source of offset. At each switching instant a certain amount of charge Q is injected on the input capacitance, causing a spike equal to Vinj=(Q)/(Cin).The amount of the injected charge is calculated by,

$$\Delta Q = \frac{WLC_{ox}}{V_{ck} - V_{in} - v_{th}} \quad (4)$$

where W, L, Cox vth, are transistor parameters, Vin and Vclk are the signal and clock amplitudes respectively.

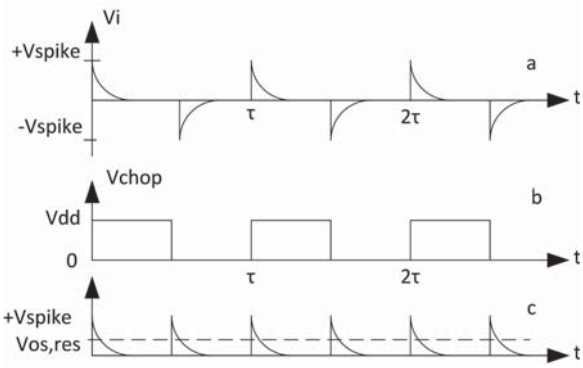

Fig. 2. Residual Offset caused by a. A spike signal b. Demodulation signal c. Demodulate signal

This parasitic signal, spike, is periodic with T=1/fchop , as well as the demodulation signal. Therefore, a substantial part of this spike energy will be amplified and then translated back to dc resulting to a residual offset. This offset is given by,

$$V_{of} = \frac{2\tau}{T}V_{sp} \quad (5)$$

where τ is the time constant of the spikes and Vsp is their amplitude. Consequently, the residual offset is determined by the number of the spikes and theirs energy content.

In the nested chopping technique, since the one pair of the input modulator operates at high frequency and suppresses the 1/f noise, the other pair can operate at lower frequency. Therefore, the residual offset caused by these choppers is much lower.

The corresponding signals of the nested-chopper amplifier are shown in Fig. 2. The spikes of the high chopping frequency are modulated by the low chopping frequency diminishing the total offset. For better offset performance, the designer should minimize as much as possible the lower chopping frequency and minimize the dimensions of the choppers transistors. In this way, the charge injection is getting less. Furthermore, a symmetrical layout of the choppers should be high priority of the designer, since the component mismatch arise additional spikes.

B. Nonidealities in Chopping Waveforms

Another potential source of residual offset in chopped amplifier can be the different rise/fall times and the clock skew among the chopping waveforms. In the nested chopping technique any skew between the input and the output chopping waveform will be translated into a DC component in the output. Well defined chopping waveforms result in more symmetrical spurs at the output and more effective filtering. Using low chopping frequencies minimizes the average value of the mismatch or skew in one period.

C. Efficient Filtering

The choice of chopping frequencies determines also the specifications of the low-pass filter that follows after the instrumentation amplifier. An ideal low pass filter removes all the harmonics except the first one. This is the optimum

offset reduction that can be achieved. However, this transfer function is difficult to be implemented. The filter should be able to suppress as much as possible the unwanted signals. The chopping technique produces several undesired spurs that are located to the frequencies of the chopping waveforms.

The amount of attenuation required from the low-pass filter will depend on the magnitude of these spurs and their location in frequency domain. If the ripple from these spurs should be low enough then a demanding filter should be designed. Thus, there is a trade-off between the complexity of the filters design and the low-noise performance.

IV. Circuit Imlpementation

A. Architecture of the Instrumentation Amplifier

The proposed instrumentation amplifier has been implemented as shown in Fig. 3. The circuitry is the essential part of the read out system for a temperature sensor. Given that the bandwidth in the temperature sensing application is very low, the nested chopping technique can be used to eliminate the 1/f noise and suppress the offset. The detectable signal is on the range of microvolt and thus imposes severe noise conditions.

The amplifier consists of two input modulators, the current mode amplifier and two output modulators. The topology of the amplifier is based on current conveyors CCIIs. The instrumentation amplifier transfers its input voltages Vy from the high impedance terminals to terminals X developing a current across the resistor Ri. This current is conveyed at the output terminals Z and is converted into voltage across the resistor Ro. The gain is determined by the ratio of the resistors an is expressed as

$$A_o = \frac{(Vin_+) - (Vin_-)}{(Vout_+) - (Vout_-)} = \frac{R_o}{R_i} \tag{6}$$

The inner choppers (Φihigh) operate at high frequency of 100kHz in order to remove 1/f noise and the outer choppers (Φilow) operate at a much lower frequency of 40Hz. The low chopping frequency flow imposes limitations to the input signal frequency. The maximum input signal frequency is reduced to the half flow. However, a bandwidth of a few tens of Hertz is sufficient for our application.

B. Design of Modulators

The choppers are implemented by a set of switches surrounded by half-sized dummy transistors [10] as shown in Fig. 4. The switches alternate the signal path using a clock Φ and its complementary signal Φ to implement the chopping principle. The dummy transistors are MOSFETs with shorted drain-source and the use of them in the signal path is to compensate the channel charge when the switch changes fast state. The control signal of the dummy transistor is the complementary signal of the switch that surrounds and therefore, the dummy MOSFET charge will cancel the charge in source and drain terminal of the main switch.

The input choppers are the most noise critical part of the total instrumentation amplifiers as it receives directly the input signal. The thermal current noise spectral density due to the resistive channel in the MOSFET is given by [7]:

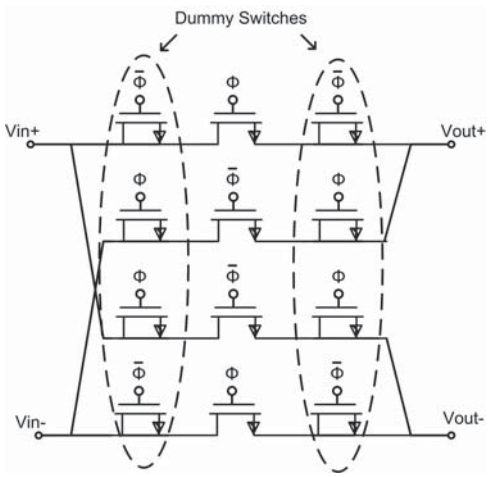

Fig. 4. One pair of modulator schematic

TABLE I
MOSFET DIMENSIONS OF THE CCII

M1,M2	120μm/7μm	M7	150μm/0.4μm
M3	65μm/5μm	M8	50μm/0.4μm
M4	115μm/5μm	M9, M10	50μm/2μm
M5,M6	150μm/2μm	M11,M12	4μm/16μm

$$i_{ni}^2(f) = 4kTk_{p/n}\frac{W}{L}V_{eff} \tag{7}$$

From the Eq. 7 can be derived that the dimensions of the switches can change the level of the thermal noise. NMOS devices are more appropriate than PMOS due to speed consideration. Since the switches contribute to the total thermal noise, the switches need to be sized to have lower thermal noise floor than the actual amplifier.

The output choppers are not noise critical as they handle the output amplified signal. Hence, the main switches set to twice the minimum size and their dummies set to minimum sizes.

C. Design of CCIIs

CCII is an excellent alternative to be used as basic building block for the instrumentation amplifier. It can be seen as three port device containing a voltage and current follower. Using CCIIs to design the amplifier provides stability to the circuit as the whole topology is designed without any external feedback loop. The proposed current conveyors architecture is depicted at Fig. 5 and is based on [12]. The input transistors M1 and M2 are implemented with PMOS transistors and large gm1 and gm2 for better flicker-noise performance. Increasing the input transistors size reduces the flicker-noise corner frequency, however, the input capacitance is increased by the same amount leading to a higher offset. The detailed transistors dimensions are shown in IV-C. Simple current mirrors retain the power consumption low. By connecting the negative output to node X the circuit converted into a non-inverting CCII.

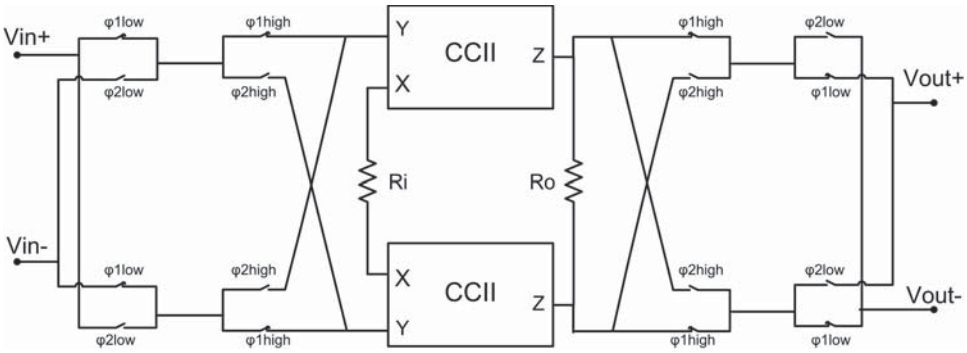

Fig. 3. Chopping Instrumentation Amplifier

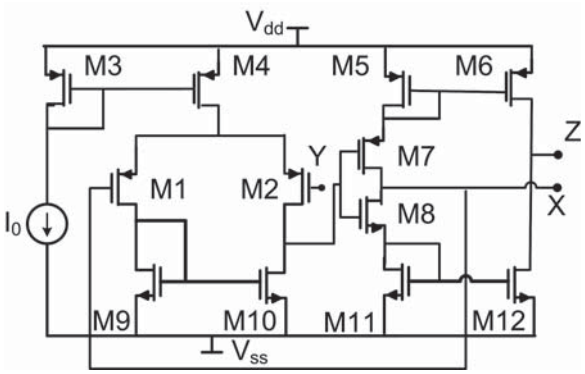

Fig. 5. Second generation current conveyor

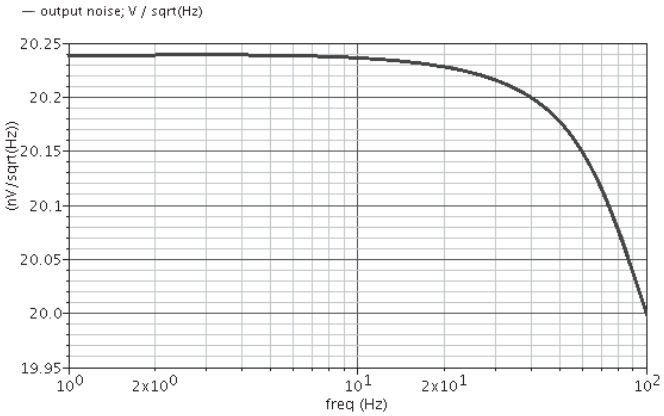

Fig. 7. Noise spectral density with chopping

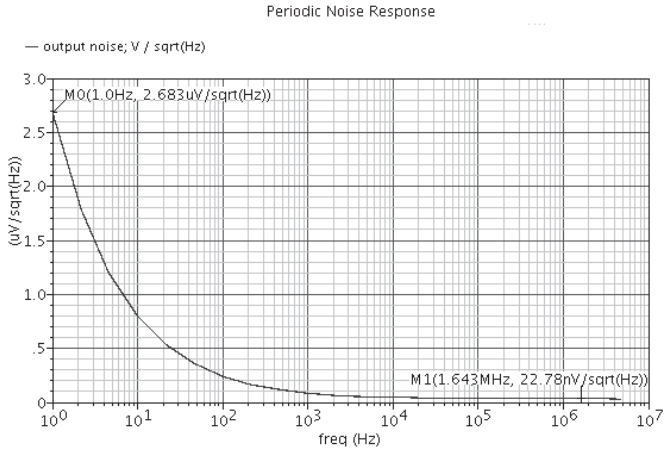

Fig. 6. Noise spectral density without chopping

V. Simulation Results

The proposed chopped instrumentation amplifier was designed, verified, and laid out with 0.18μm CMOS process using SPECTRE simulator.

The periodic steady-state (PSS) and periodic noise analysis (PNOISE) capabilities are used to simulate and compare the noise performance of the instrumentation amplifier spectre with or without chopping. Choosing the high chopping frequency at the same value as the flicker noise-corner frequency and the low chopping frequency twice the bandwidth we expect better noise performance. On the other hand, setting the chopping frequency the same as the noise corner frequency would degrade the residual offset performance.

The amplifier input referred noise response is initially extracted without chopping and illustrated at Fig. 6. The noise corner frequency is at 100kHz and the white noise is 22nV/$\sqrt{Hz}$. Without chopping, the 1/f noise is dominant at frequencies below 100KHz. Fig. 7 shows the noise spectre when the choppers are enable. The high chopping frequency selected to be at 100kHz and the low chopping frequency at 40Hz. The input signal at the differential input of the instrumentation amplifier during the noise performance had a frequency at 20Hz.

The noise performance of the instrumentation amplifier Fig. 6 and Fig. 7 prove that chopping concept works with excellent results. The white noise floor is dominant both to the low and high frequencies.

The residual offset of the instrumentation amplifier is measured by Monte Carlo analysis and is shown in Figure 8 The amplifier has an average offset of 582nV.

The CMRR of the instrumentation amplifier plays important role to the sensitivity of the total sensor system. Since the input signals are too small a high CMRR is required. Fig. 9 depicts the CMRR distribution of the IA. The mean value of the CMRR is 110dB.

The total performance characteristics of the proposed instrumentation amplifier are summarized in V.

The proposed design achieves an excellent noise perfor-

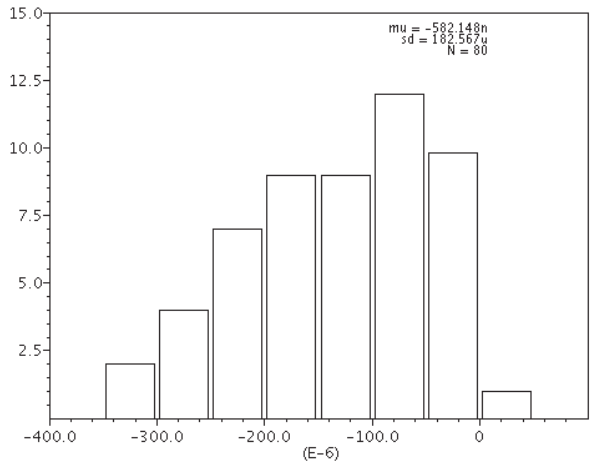

Fig. 8. Offset distribution of the designed IA

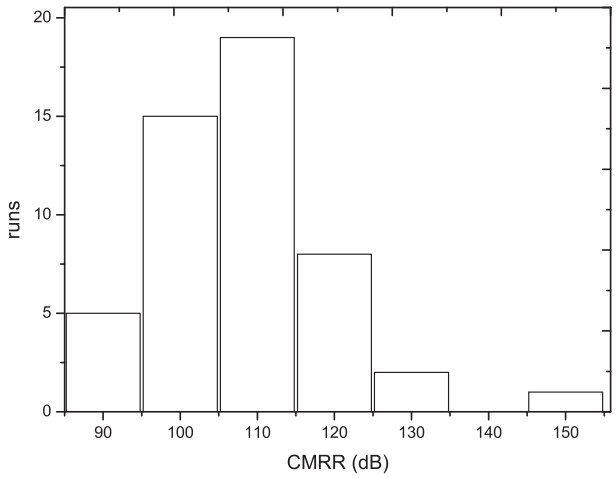

Fig. 9. CMRR of the Instrumentation Amplifier

TABLE II
SIMULATION PERFORMANCE OF THE IA

Supply Voltage	1.65 V
Input Noise Density	22nV/$\sqrt{Hz}$
Input Offset Voltage	582 nV
Noise Corner Frequency	100kHz
CMRR	110dB
Power Consumption	420μW
Input Common Mode Voltage	-0.91 V

mance and a significant low offset. Since the CMRR is independent of the resistors matching, the good CMRR performance of the current mode instrumentation amplifiers is also verified in this design. Moreover, it should be highlighted that the full instrumentation amplifier consumes only 420μW. The instrumentation amplifier layout is shown in Fig. 10. The layout was designed as symmetric as possible to eliminate mismatches between the differential parts of the device. Common centroid techniques were implemented for better performance.

V shows a performance comparison between the proposed and currently used instrumentation amplifiers [13], [14] .It

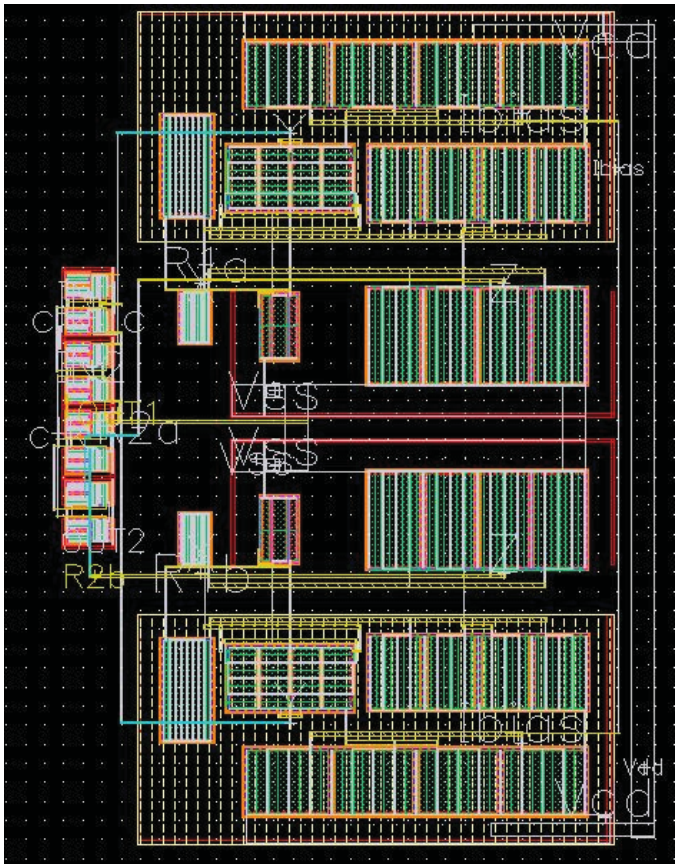

Fig. 10. Layout of the designed IA

TABLE III
COMPARISON BETWEEN OTHERS IA CIRCUITS

	This work	[13]	[14]
Input offset voltage	582nV	1μV	3μV
Input noise nV/$\sqrt{Hz}$	22	60	27
CMRR	110dB	134dB	140dB

can be seen that this work acheives the lowest input offset. Also, we can observe that the proposed circuit has a lower input noise voltage than other topologies [13], [14]. Thus, it has a wider dynamic range and higher signal-to-noise ratio when compared with [13] , [14]. Notwithstanding that this work provides the lowest CMRR, its CMRR performance is considered satisfactory for many applications.

VI. CONCLUSION

In this paper, an extended analysis of chopping technique and its performance limitations have been discussed. The nested chopping technique is applied to a current mode instrumentation amplifier to prove that the technique works excellent and has better performance than the voltage mode amplifiers. In the proposed amplifier significant low offset and low noise performance are acheived. The non-existence of the ground connection contributes to high CMRR. However, many improvements could be investigated in relation to the output low impedance using an output buffer and power consumption as it is one of the critical characteristic for sensors application.

ACKNOWLEDGMENT

The research activities that led to these results were co-financed by Hellenic Funds and by the European Regional Development Fund (ERDF) under the Hellenic National Strategic Reference Framework (NSRF) 2007-2013, according to Contract no. MICRO2-49 of the Project Development of Innovative sensor systems offering distributed intelligence MEMSENSE within the Programme Hellenic Technology Clusters in Microelectronics Phase-2 Aid Measure.

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