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METHOD OF HIGH TIMING RESOLUTION PULSE SYNTHESIS BASED ON VIRTUAL SAMPLING

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Abstract

Adjustable-width pulse signals are widely used in systems such as test equipment for hold time, response time and radar testing. In this study, we proposed a pulse generation method based on virtual sampling with ultra-high pulse width resolution. In the proposed method, the sampling rate of a digital-to-analogue converter (DAC) was adjusted to considerably improve pulse width resolution. First, the sampling rate was matched with the target pulse width resolution to digitally sample the ideal signal and generate digital waveform sampling points. Next, the signal bandwidth of the DAC was matched using a low-pass digital filter. Finally, the waveform sampling points were downsampled using an integer factor and output after digital-to-analogue conversion. The waveform pulse width information generated by high-frequency digital sampling was passed step by step and retained in the final output analogue signal. A DAC with a sampling rate of 1.25 GSa/s was used, and the pulse width resolution of the pulse signal was 0.1 ns. Theoretically, a sampling rate of 10 GSa/s is required to achieve 0.1 ns resolution. This method is simple, has a low cost, and exhibits excellent performance.

Keywords: pulse synthesis, high resolution, virtual sampling, digital-to-analogue conversion, downsampling.

1. Introduction

Pulse and *pulse width modulation* (PWM) play crucial roles in electronics and are widely used in computers, communications, automatic control and measurement [1–3]. Typically, *direct digital synthesis* (DDS) is used to generate waveforms in waveform generators [4–6]. DDS is low-cost and exhibits low power consumption, high resolution and a fast conversion time [7]. As a key technology of digitisation, DDS is widely used in telecommunications and electronic instruments [8]. The following components are used to realise conventional waveform DDS: a frequency tuning register, a phase accumulator and a waveform *look up table* (LUT) [9–12]. The input *frequency tuning word* (FTW) is loaded and registered in the frequency control register. The phase accumulator accumulates the phase in each clock cycle according to the FTW to

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provide a phase value. Next, the high N bits of the phase value are considered as the address of the LUT to obtain waveform samples. The DAC receives the waveform samples and generates the desired waveform. If pulse waves are stored in the LUT, a pulse can be generated. Currently, if DDS is used to generate pulse and PWM signals, a clock cycle, typically of fixed nanoseconds, is used. The use of an analogue time delay chip in pulse synthesis based on the relative delay ensures a 1-ps pulse width resolution [13]. Thus, high pulse width resolution can be achieved through this method. Eftichios K. *et al.* proposed a PWM method based on a *field programmable gate array* (FPGA) to achieve a pulse width resolution of 1.56% of the duty cycle [14]. The count clock in the FPGA is generally up to approximately 500 MHz, and the corresponding pulse width resolution is 2 ns. Sharma A. *et al.* proposed a re-configurable digital-synthesis-based pulse generator to output a pulse waveform with its edge time, width and period set to 5, 7.5 and 15 ns [15]. Qin *et al.* proposed a pulse generator that can continuously output pulse with a 50-ps time resolution and a dynamic range from 5 ns to 2 s [16]. However, the pulse generator required customisation for the pulse waveform. De Matino M. *et al.* generated a pulse waveform by counting a DDS-generated clock periods. However, the pulse width resolution was limited to the period of the counting clock [17]. Morales J. I. *et al.* proposed a pulse generating circuit based on a digitally controlled delay element to achieve a variable time interval of up to 54 ps [18].

Based on the conventional DDS waveform synthesis technology, this study proposed a pulse wave generation method based on virtual sampling. The proposed method can considerably improve the timing resolution, including the rise time, fall time and pulse width of pulse signals when the performance of the DAC is limited. This method can increase the timing resolution by ten times or even a hundred times, without increasing the sampling rate and bandwidth of the DAC. As a method of waveform synthesis based on DDS, it can be applied to function generators, waveform generators and other equipment with pulse signal generation functions. As the data rate of the serial buses increases, the standard digital signal becomes susceptible to jitter in the transmission process, which results in a high *bit error rate* (BER) [19, 20]. The proposed method can be used as a time modulation method to implement jitter control on pattern data to realise the generation of digital signals carrying standard jitter sources [21, 22]. Digital and the analogue filters were combined, and the step-by-step transmission of the high timing resolution of the sample points was achieved by filtering the spurious signals using the zero-order hold sampling of the DAC [23]. Improved pulse width resolution can enhance PWM. This rest of this article is organised as follows: Section 2 introduces pulse synthesis based on virtual sampling. In Section 3, a theoretical verification of the proposed method is performed through simulation. In Section 4, the feasibility of the method is assessed experimentally. Section 5 provides a summary of this method and a direction for future studies. The main innovation of this paper is to achieve pulse waveform synthesis with a timing resolution beyond the sampling interval. In the hardware circuit, only minimal logic resources and a simple circuit are required to synthesize pulse waveforms with high timing resolution.

2. Pulse synthesis based on virtual sampling

The pulse is defined as displayed in Fig. 1. A pulse consists of a period, a pulse width, a rising edge and a falling edge [24]. The high and low levels of the pulse are V_H and V_L, respectively. The pulse period $1/f$ defines the time between two consecutive pulses from the start of the leading edge to the start of the next leading edge. The edge time sets each edge transition time (rising and falling) of the pulse. For each transition, the edge time represents the time from the 10% threshold to the 90% threshold. Pulse width refers to the interval between 50% of leading edge and 50% of

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the trailing edge. An ideal pulse wave can be determined by these six parameters. This definition is used for the proposed synthesis method.

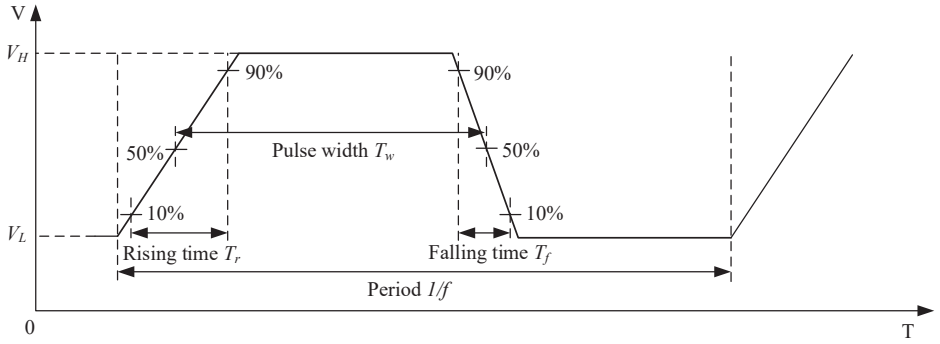

Fig. 1. Definition of a pulse waveform.

Fig. 2 displays the block diagram of the pulse synthesis method based on virtual sampling. The user inputs the waveform parameters through the host computer control software, converts them, and sends them to the local interface through the communication bus. The waveform parameters should include pulse frequency f, pulse width T_w, rising edge time T_r, falling edge time T_f, high-level V_H, low level V_L and pulse width resolution t. In this method, virtual sampling frequency Nf_s depends on pulse frequency f and pulse width resolution t. Here, Nf_s is less than $1/t$, and f_s is an integer multiple of the pulse frequency. The local interface is used to receive waveform data and waveform parameters, decode them into a local bus format, and send them to the parameter control module. The parameter control module distributes the local bus data to the waveform sample generator, digital filter and waveform downsampling modules of the system.

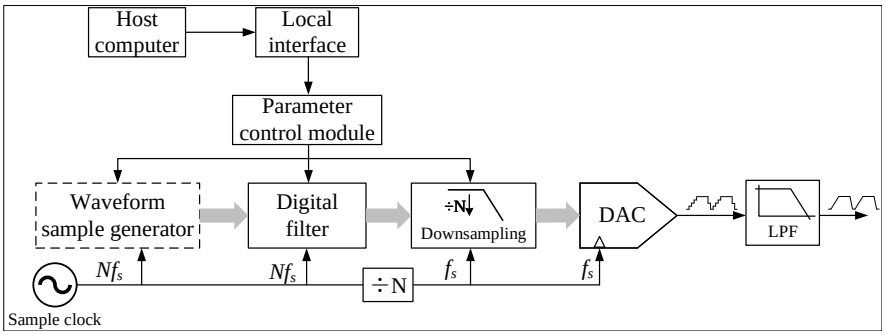

Fig. 2. Pulse synthesis based on virtual sampling.

The waveform sample generator is the key component of this method. Original waveform sample points are generated in a generator driven by the sampling clock and sent to the digital filter for bandwidth limitation. The sampling frequency of the waveform generator is Nf_s. Because Nf_s is less than $1/t$, original waveform samples can achieve adjustment of pulse width higher than the pulse width resolution. Because f_s is an integer multiple of pulse frequency f, and Nf_s is also an integer multiple of f, a fixed number of waveform samples exist in each pulse period generated by the waveform sample generator. Thus, jitter from the source caused by the difference of the number of samples per cycle is avoided.

The original waveform samples generated by the waveform sample generator are sent to the digital filter to realise bandwidth limitation of the original waveform samples, and the waveform samples matching its bandwidth are obtained using DACs. The prerequisite for a DAC reconstructing the pulse wave without distortion is that the bandwidth corresponding to the waveform samples should be less than the DAC bandwidth. The digital filter sends the filtered waveform samples to the downsampling module. The sampling frequency of the digital filter is Nf_s, and the higher harmonic of the waveform samples of the waveform sample generator are filtered out to align the bandwidth of the DAC. The various parameters of the digital filter considerably affect the quality of the pulse.

After the waveform samples are filtered using a digital filter, they are sent to the downsampling module. The filtered samples are downsampled by the downsampling module to obtain waveform samples matching the sampling rate of the DAC, and the downsampled samples are next sent to the DAC. The input sampling rate of the downsampling module is Nf_s, and the output sampling rate is converted to f_s through resampling. Among them, the sampling clock f_s is divided by N from Nf_s sampling clock.

The downsampled waveform samples are sent to the DAC. The sampling rate of the DAC is f_s, and the waveform samples downsampled by the downsampling module are converted to output an analogue pulse. Because of the zero-order hold characteristics of the DAC, the output analogue signal contains spurs including the image frequency. The unwanted harmonics and spurs can be filtered to obtain a near-ideal pulse. The *low-pass filter* (LPF) filters out harmonics and image frequencies outside the pulse signal bandwidth to obtain a high-resolution pulse wave with a controllable pulse width.

3. Simulation

The simulation experiment for this method is based on MATLAB, and the consecutive simulation steps are as follows:

1. Generate original waveform samples according to waveform parameters.
2. Design a digital filter to limit the bandwidth of the original waveform samples.
3. Design the downsampling module.
4. Construct a real pulse wave with downsampled samples.
5. Sample and analyse the pulse wave using the oscilloscope simulation of SIMULINK in MATLAB.

The waveform generation and measurement process in hardware circuits can be simulated in these five steps. In the simulation, the sampling rate of DAC was set to 1.25 GSPS, which results in the sampling interval of 800 ps. The original waveform samples were generated through virtual sampling which is eight times the DAC sampling rate, and the resolution of timing parameters such as the rising time, falling time and pulse width can be improved from 800 to 100 ps. Each step is explained in detail.

3.1. Generation of original waveform samples

The first simulation step is to generate original waveform samples and the key to generating them is the development of the sample calculation formula according to the parameters of the pulse wave. The objective of this simulation is to achieve a timing resolution of 100 ps with a DAC sampling rate of 1.25 GSPS. A timing resolution of 800 ps was achieved at a sampling interval corresponding to 1.25 GSPS. For realising a 100-ps timing resolution, the virtual sampling rate should be eight times the DAC sampling rate, which is 10 GSPS.

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Fig. 3 displays the dotted box diagram, *i.e.*, the waveform-sample-point generating module, of Fig. 2. As displayed in Fig. 3, the pulse control module exhibits phase accumulation driven by the sampling clock Nf_s, and the phase parameters are pulse width T_w, rising time T_r, falling time T_f and pulse frequency f. The pulse control module switches the sample source and outputs the waveform samples alternately and sequentially from the rising edge compute module, falling edge compute module and high-level and low-level modules. Switching is based on the result of comparison between the phase accumulation and the calculations with pulse parameters which are displayed in the following equations. Here, K is the value any time the accumulator is triggered by the sampling clock. The rising edge calculation equation is as follows:

$$V_{\text{sample}} = \frac{0.8}{T_r} \times (V_H - V_L) \times \frac{K}{Nf_s}\,. \tag{1}$$

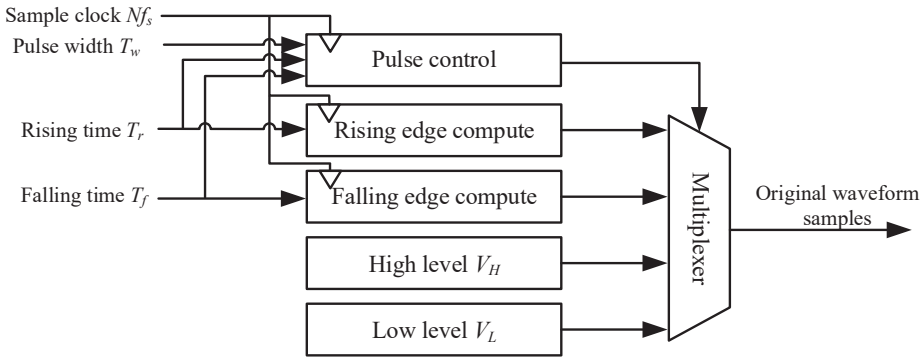

Fig. 3. Block diagram of original waveform sample calculation.

The accumulator threshold in the rising edge calculation equation is expressed in the following inequality:

$$1 \le K \le \frac{T_r}{0.8} \times Nf_s\,. \tag{2}$$

The high-level waveform sample voltage value is V_H.

The accumulator threshold at the high level is displayed in the following inequality:

$$\frac{T_r}{0.8} \times Nf_s \le K < T_w \times Nf_s + \frac{T_r - T_f}{1.6} \times Nf_s\,. \tag{3}$$

The falling edge calculation equation is as follows:

$$V_{\text{sample}} = \frac{0.8}{T_f} \times (V_H - V_L) \times \left(T_w + \frac{T_r + T_f}{1.6} - \frac{K}{Nf_s}\right). \tag{4}$$

The accumulator threshold in the rising edge calculation equation is expressed as follows:

$$T_w \times Nf_s + \frac{T_r - T_f}{1.6} \times Nf_s \le K < T_w \times Nf_s + \frac{T_r + T_f}{1.6} \times Nf_s\,. \tag{5}$$

The low-level waveform sample voltage value is V_L.

The accumulator threshold in the low level is expressed in the following inequality:

$$T_w \times Nf_s + \frac{T_r + T_f}{1.6} \times Nf_s \le K < \frac{Nf_s}{f}\,. \tag{6}$$

According to the equations above, K is accumulated at each sampling clock and next it is used to calculate original pulse waveform samples, as displayed in Fig. 4.

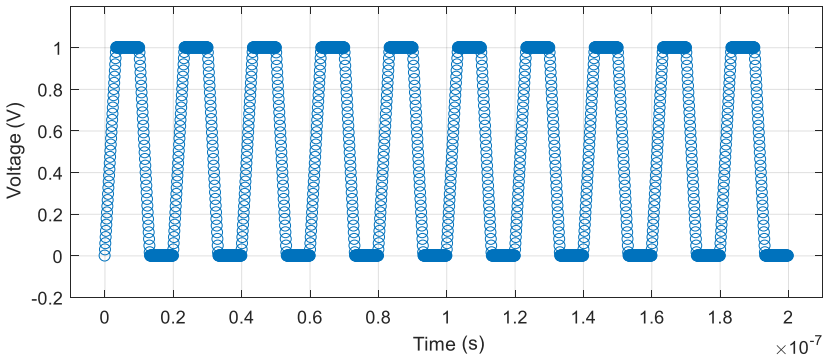

Fig. 4. Original waveform samples.

3.2. Designing the digital filter

In this simulation, the virtual sampling rate was set to 10 GSPS, and the DAC sampling rate was 1.25 GSPS. A decimation filter incorporates an LPF which is used to eliminate high-frequency components in the spectrum. If these components are not filtered out, aliasing may occur on reduction of the sampling rate [25]. The bandwidth of the digital filter should match that of the DAC. The DAC39J82 DAC sampling rate in the hardware test platform selected in this study was 1.25 GSPS. To verify the simulation in the hardware circuit, the DAC sampling rate in this simulation was identical to the sampling rate of the actual hardware platform *i.e.*, 1.25 GSPS. The DAC39J82 bandwidth is 0.4×1.25 GSPS $= 500$ MHz [26]. Therefore, the passband frequency of the digital filter should be designed to be 500 MHz. To reduce the overshoot after filtering, a Butterworth digital filter was selected among other digital filters. The sampling frequency of the digital filter should be 10 GSPS, which is the same as the virtual sampling rate. Following the requirements above, the Filter Designer in MATLAB was used to design a digital filter, and the magnitude response of the designed filter is displayed in Fig. 5. As illustrated in

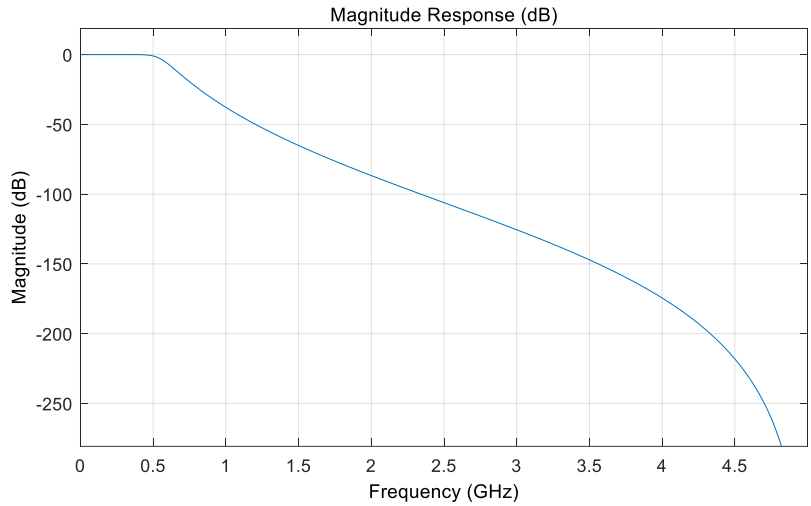

Fig. 5. Magnitude response of the digital filter.

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Fig. 6, the original waveform samples passed through the digital filter to obtain bandwidth-limited pulse waveform samples.

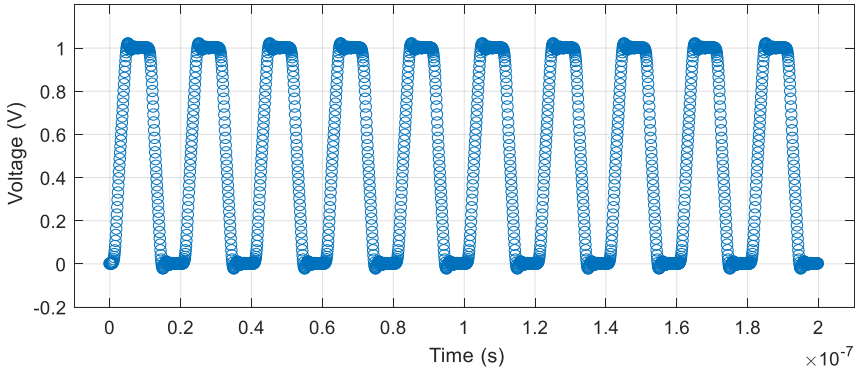

Fig. 6. Digital filtered data samples.

3.3. Decimation and interpolation

The bandwidth of the waveform samples after digital filtering was less than the maximum bandwidth of the DAC. After the bandwidth was limited, the waveform sampling rate remained higher than that of the DAC. Therefore, the waveform sampling rate should align the DAC. In this simulation, the DAC sampling rate was set to 1.25 GSPS, the virtual sampling rate was 10 GSPS, and the filtered waveform samples should be set to decimate by eight. As displayed in Fig. 7, the waveform sampling rate was decimated by eight times. To accurately measure the pulse width, rising time, falling time and other parameters of the pulse waveform, an interpolation algorithm was used to achieve a smooth waveform to simulate the pulse after the signal passed through the DAC and the analogue LPF in the hardware. As displayed in Fig. 8, a smooth transition of discrete waveform samples was achieved by a *piecewise cubic Hermite interpolating polynomial* (PCHIP) applied 1000 times.

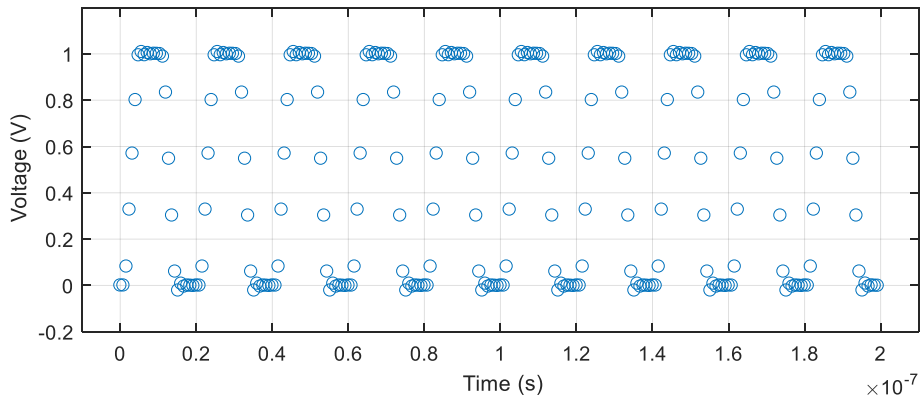

Fig. 7. Resampled data samples.

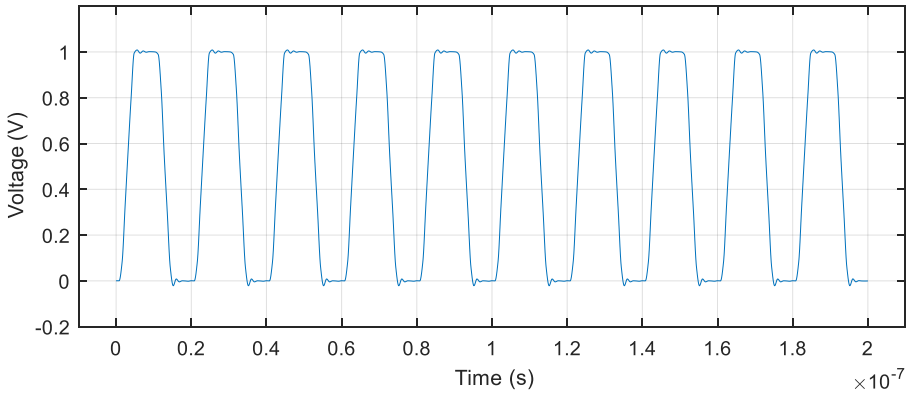

Fig. 8. Data samples after interpolation.

3.4. Validation

The 100 ps timing resolution of the waveform samples was verified by the built-in oscilloscope tool in MATLAB. A continuous pulse waveform was produced by the PCHIP on waveform samples and measured using the oscilloscope tool. As displayed in Fig. 9, the upper left pulse had a rising time, falling time and width of 2.5, 2.5 and 10 ns, respectively. The resultant pulse had a rising time, falling time and pulse width of 2.5, 2.47 and 9.972 ns, respectively. The lower left pulse had a rising time, falling time and pulse width of 2.6, 2.6 and 10.1 ns, respectively. The resultant pulse had a rising time, falling time and pulse width of 2.572, 2.586 and pulse width of 10.067 ns. The upper right pulse had a rising time, falling time and pulse width of 2.7,

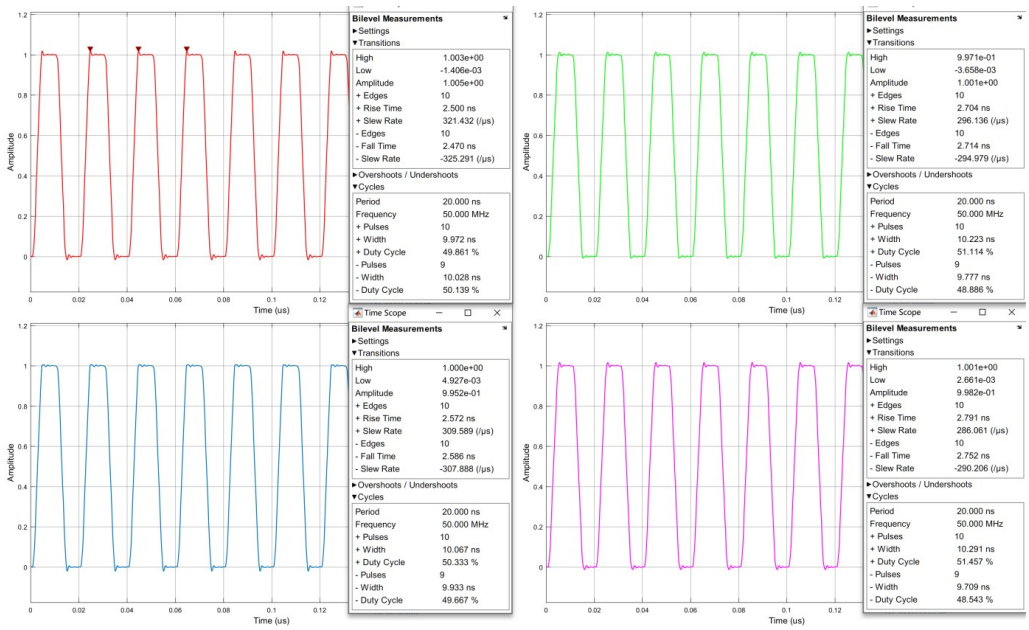

Fig. 9. Pulse waveform measured with the oscilloscope tool.

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2.7 and 10.2 ns. The test resultant pulse had a rising time, falling time and pulse width of 2.704, 2.714 and 10.223 ns. The lower right pulse had a rising time, falling time and pulse width of 2.8, 2.8 and 10.3 ns. The resultant pulse had a rising time, falling time and pulse width of 2.791, 2.752 and 10.291 ns. All pulse frequencies were 50 MHz. The oscilloscope simulation revealed that the rising time, falling time and pulse width of the pulse waveform all increased in 100-ps steps. The simulation verified that the pulse waveform achieved the rising edge, falling edge and pulse width of 100 ps resolution at the 1.25 GSPS sampling rate. The method was verified on the hardware test platform as described below.

4. Pulse measurement results

The pulse waveform synthesis method was verified on the hardware test platform. The hardware test platform used included the following components: a waveform synthesis module including an XCKU085FFVA1516-2I (FPGA), a DAC39J82 digital-to-analogue converter [26], an ADVANTECH MIO-3260 control module [27] and a LeCroy WaveMaster 813Zi-A digital oscilloscope. The control module was connected to the waveform synthesis module with an PCIe connector to transmit waveform samples, control commands and clock signals. The sampling rate of the waveform synthesis module was 1.25 GSPS, and the 2.5 GSPS sampling rate was achieved by 2× interpolation. The sampling rate of the digital oscilloscope was up to 40 GSPS and the bandwidth was 13 GHz.

The test platform was set up as displayed in Fig. 10. The sampling clock was generated by ADF4351 *phase-locked loop* frequency synthesisers [28] and distributed to the DAC and the FPGA using an LMK04828 high-performance clock conditioner [29]. The clock used to drive the DAC was set to 2.5 GHz, and the clock output to FPGA was set to 156.25 MHz The FPGA outputs 1.25 GSPS samples by running in parallel with eight channels driven by a 156.25 MHz clock. The FPGA was used to generate waveform samples and control the DAC. The DAC worked in the interpolation 2x mode and the output sample rate was 2.5 GSPS. Waveform samples were generated at 10 GSPS virtual sampling rate and decimated by eight to 1.25 GSPS sampling rate. The waveform samples calculated in the control module were transmitted to the FPGA through a PCI Express bus. The DAC analogue outputs were DC coupled through a THS3202 amplifier [30]. The analogue pulse waveforms were then output to the digital oscilloscope which

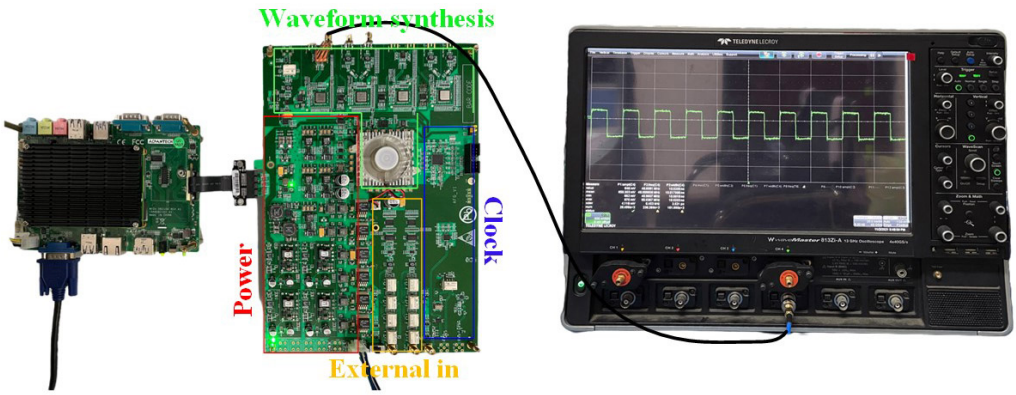

Fig. 10. Experimental test platform.

measured the pulse waveform to obtain the rising time resolution, falling time resolution, pulse width resolution and other parameters. As displayed in Fig. 11, the test results revealed that when the pulse frequency was 50 MHz, the rising time was 2.50 and 2.63 ns, the falling time was 2.45 and 2.61 ns, and the pulse width was 10.03 ns and 10.14 ns. As displayed in Fig. 12, the pulse frequency was 100 MHz, the rising times were 2.48 and 2.58 ns, the falling times were 2.47 and 2.64 ns, and the pulse widths were 5.06 and 5.16 ns. It can be seen that the timing resolution could reach 100 ps. Fig. 13 displays the pulse waveform with a 4.25-ns pulse width at 50 MHz. Figs. 14 and 15 reveal that the rising time and falling times changed from 2.5 to 10.5 ns with a step of 2 ns. Fig. 16 illustrates that the pulse width changed from 4.0 to 4.9 ns with a step of 100 ps. The output spectra from the pulse signal with a 50% duty cycle at 50 and 100 MHz are displayed in Fig. 17. When the output frequency was 50 MHz, the *signal-to-noise ratio* (SNR) was higher than 14

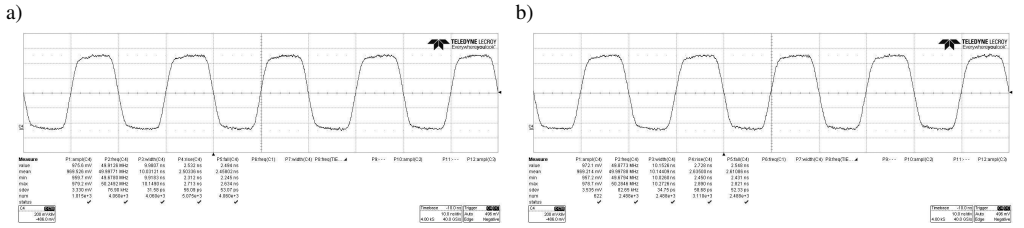

Fig. 11. Pulse waveform at 50 MHz. a) The pulse width is 10.03 ns, the rising time is 2.50 ns and the falling time is 2.45 ns. b) The pulse width is 10.14 ns, the rising time is 2.63 ns and the falling time is 2.61 ns.

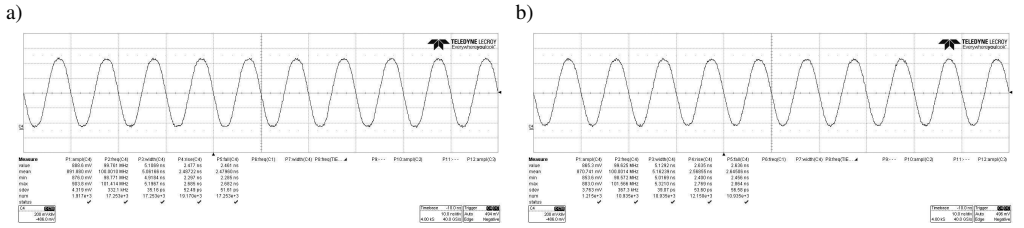

Fig. 12. Pulse waveform at 100 MHz. a) The pulse width is 5.06 ns, the rising time is 2.48 ns and the falling time is 2.47 ns. b) The pulse width is 5.16 ns, the rising time is 2.58 ns and the falling time is 2.64 ns.

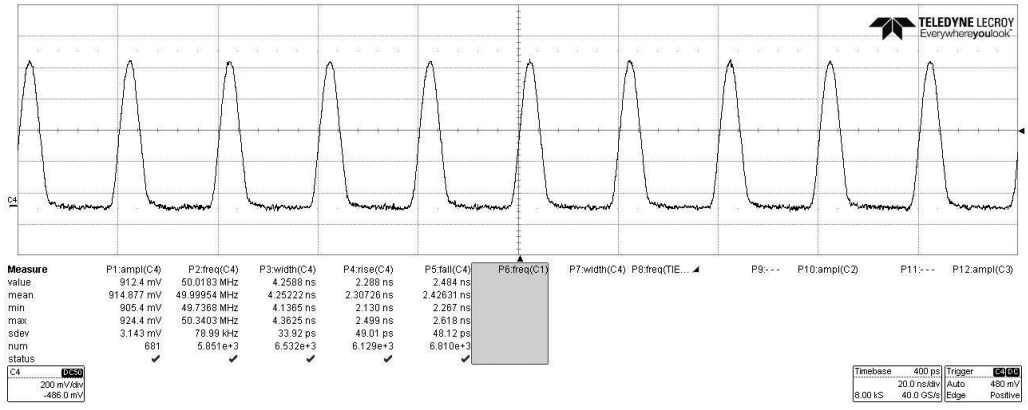

Fig. 13. Pulse waveform with a pulse width of 4.25 ns at 50 MHz.

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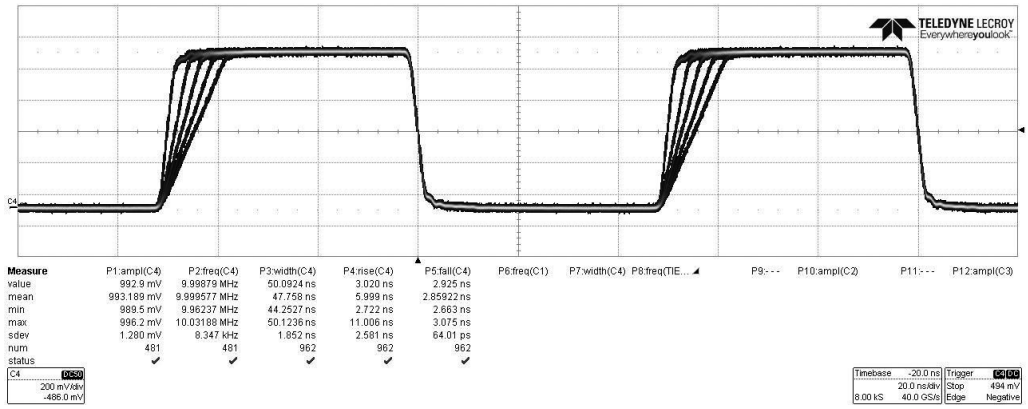

Fig. 14. Rising time changed from 2.5 to 10.5 ns.

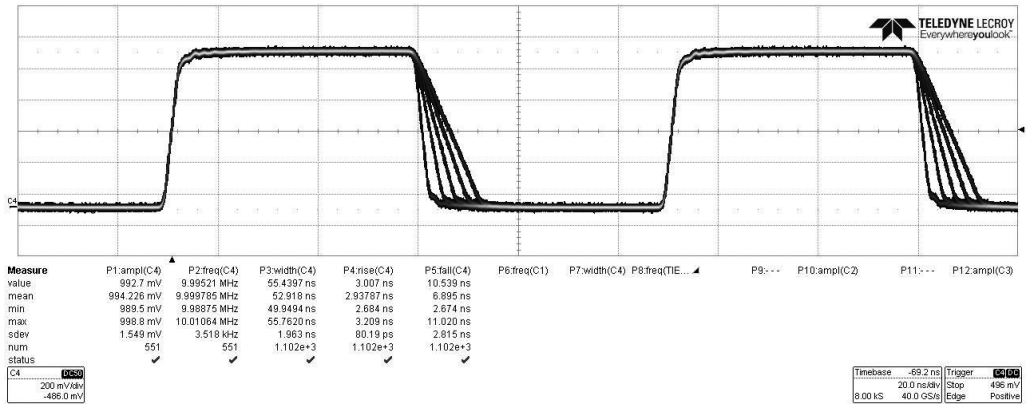

Fig. 15. Falling time changed from 2.5 to 10.5 ns.

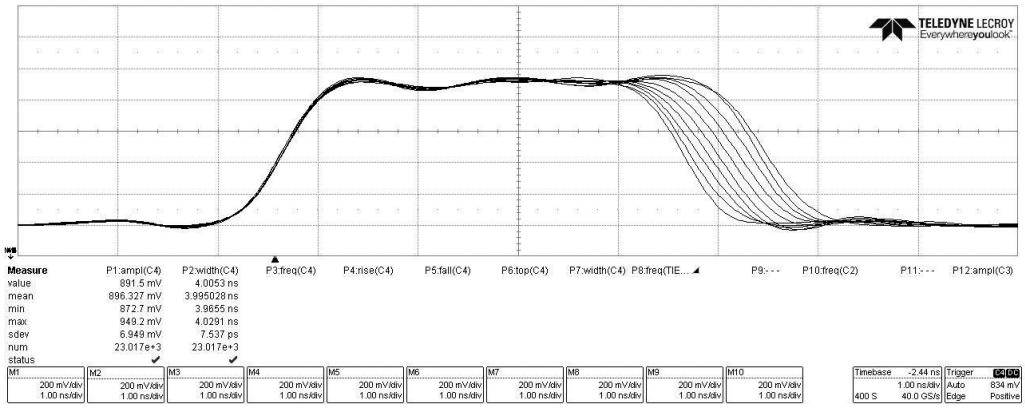

Fig. 16. Pulse width changed from 4.0 to 4.9 ns.

dB according to the minimum harmonic. When the output frequency was 100 MHz, the SNR was higher than 25 dB. The eye diagram and histograms of 50 and 100 MHz pulse waveforms are displayed in Figs. 18 and 19, where the random jitter was 24.31 and 20.89 ps, respectively.

a) b)

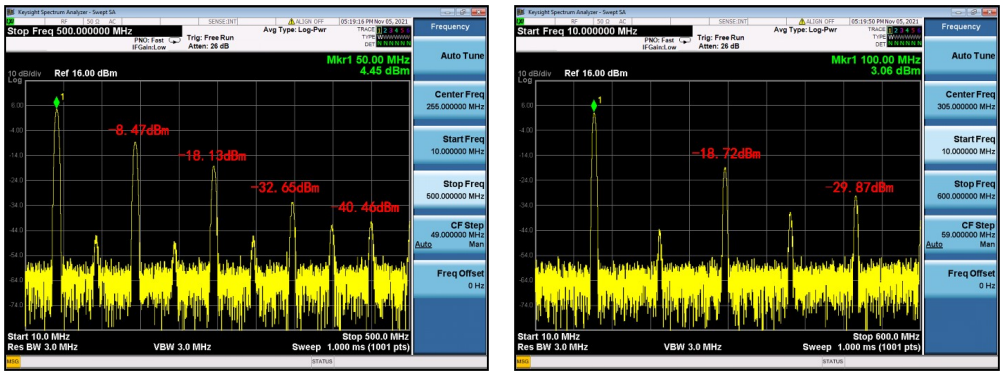

Fig. 17. Pulse waveform spectrum. (a) Spectrum at a frequency of 50 MHz. (b) Spectrum at a frequency of 100 MHz.

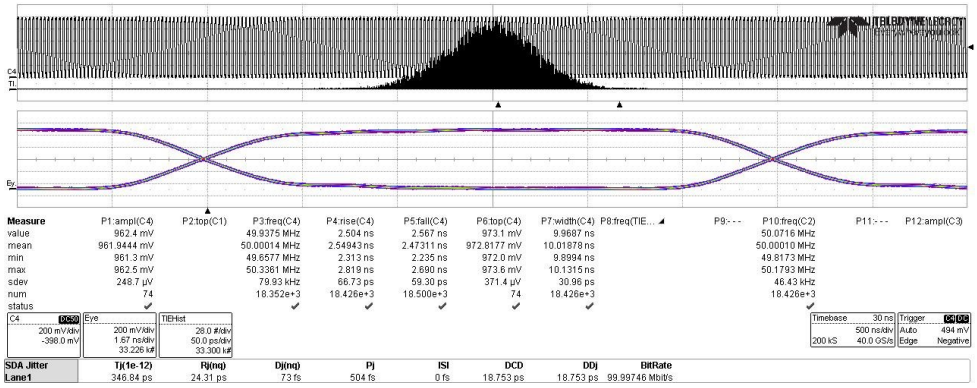

Fig. 18. Eye diagram, histogram of 50 MHz pulse waveform.

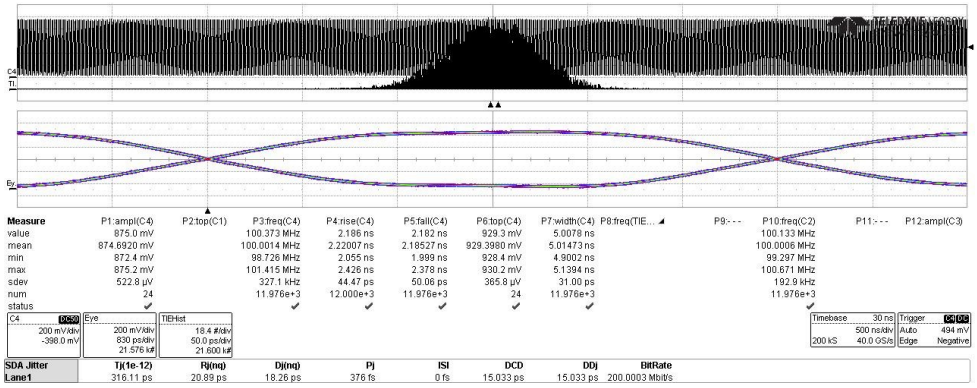

Fig. 19. Eye diagram, histogram of 100 MHz pulse waveform.

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Fig. 20 demonstrates the relationship between minimum pulse width and frequency. Fig. 21 demonstrates the relationship between minimum rising time and frequency. The implementation is presented in Table 1. Table 2 summarizes the errors between the set values and the measured ones. Compared to the other pulse generator, the proposed design provides a timing resolution of less than 100 ps with the setting of all pulse parameters, including rising and falling times, which is not possible in a pulsed output DDS design such as [31], and still provides less than 25 ps of rms jitter. Compared to counter-based pulse generator designs such as [32] and [33], the one described in this this paper provides a significant improvement in timing resolution which is limited only by

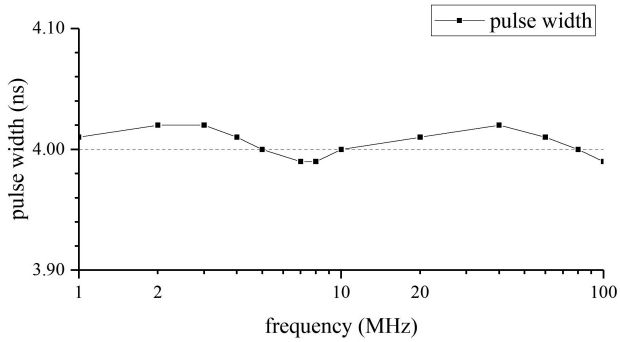

Fig. 20. Relationship between minimum pulse width and frequency.

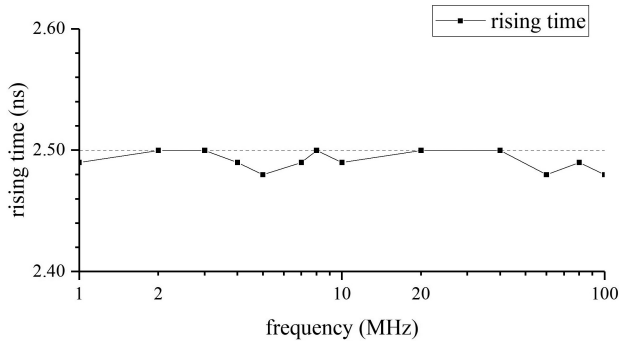

Fig. 21. Relationship between minimum rising time and frequency.

Table 1. FPGA resource occupation summary.

Resource	Utilization	Available	Utilization %
LUT	5204	497520	0.01
LUTRAM	253	267840	0.09
FF	6804	995040	0.68
BRAM	4	1620	0.25
IO	62	624	9.93
GT	9	48	18.75
BUFG	5	1128	0.44

clock cycles of typically a few nanoseconds. Finally, in contrast to the analogue pulse generator design [34], the period accuracy in this paper is only affected by the clock accuracy. In DDS-based pulse generator designs, the period accuracy is limited by the number of phase accumulator bits and the length of the rounding FTW. In antilog designs and designs of pulse edge shaping circuits with analogue conditioning, the rising and falling times can generally only be set to a maximum of several hundred milliseconds with a maximum rising and falling time ratio limitation. The design presented in this paper overcomes all these drawbacks.

Table 2. Measured rising time, falling time and pulse width of pulse waveform.

	Rising time (ns)				**Falling time (ns)**				**Pulse width (ns)**			
	50 MHz		100 MHz		50 MHz		100 MHz		50 MHz		100 MHz	
Set values	2.50	2.60	2.50	2.60	2.50	2.60	2.50	2.60	10.00	10.10	5.00	5.10
Measured values	2.50	2.63	2.48	2.58	2.45	2.61	2.47	2.64	10.03	10.14	5.06	5.16
Error values	0.00	0.03	–0.02	–0.05	–0.05	0.01	–0.03	0.04	0.03	0.04	0.06	0.06

5. Conclusions

This study proposed a novel high time resolution pulse signal generation method based on virtual sampling. The principles, simulation design, simulation verification and hardware verification were detailed. This method can be easily embedded as a module in a test and measurement equipment with a versatile waveform. The method proposed in this study can be used to generate waveforms with high timing resolution in which bandwidth is greater than its frequency, such as triangle waveforms and ramp waveforms. In this study, a DAC with a sampling rate of 1.25 GSa/s was used and the pulse width resolution of the 50 MHz pulse signal was 0.1 ns. The design is not only simple and low-cost but also exhibits excellent performance.

In the future, we will aim at improving the resolution of the pulse signal through the method proposed in this study. The timing resolution can be improved to 10 ps and even 1 ps by increasing the frequency of the virtual sampling clock. The current waveform samples are calculated and processed by the control module. In the next step, we are going to generate waveform samples with high timing resolution through real-time calculations. The generation process of waveform samples will involve migration from the control module to the FPGA for real-time calculation, and PWM will be realised by changing the pulse width value during the calculation.

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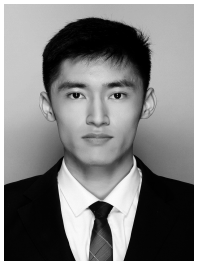

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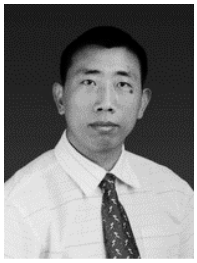

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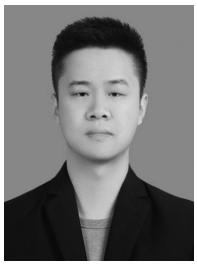

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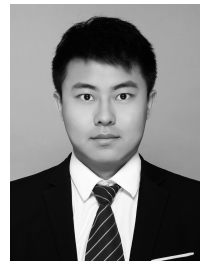

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