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SPAD timing jitter modeling using Fourier series

KAVEH EYVAZI, MOHAMMAD AZIM KARAMI*

School of Electrical Engineering, Iran University of Science and Technology, Tehran, Iran

*Corresponding author: karami@iust.ac.ir

In this paper, a simple analytical model for the Gaussian's peak response part of the timing jitter of single photon avalanche diodes (SPADs) is proposed using Fourier series in the multiplication time calculation. The multiplication time characterizes avalanche multiplication process speed in which low multiplication time suggests a swifter response time and a higher avalanche speed. This paper presents an analytical solution which results in a more accurate multiplication time. The model is verified for SPADs implemented in 0.15 and 0.18 μm standard CMOS process, and the accuracy of the proposed analytical method in full-width at half-maximum (FWHM) calculation is improved by 25% and 5% with respect to the numerical model, respectively.

Keywords: analytical model, Fourier series, multiplication time, timing jitter.

1. Introduction

Single photon avalanche diode (SPAD) detectors are promising replacements to photomultiplier tubes due to excellent timing resolution, low dark noise and simple integration in large arrays [1–5]. Due to sub-nanosecond timing resolution and high quantum efficiency, SPADs are suitable for a variety of applications such as fluorescence lifetime imaging, positron emission tomography and time-resolved near-infrared spectroscopy [6–8].

The amount of uncertainty in the time accuracy of photon detection is termed as timing resolution or timing jitter [9]. An experimental setup is described in [9,10] to study timing jitter properties, in which the time delay between the optical signal emission which is calibrated by the laser output trigger and photon detection is measured. In fact, jitter is calculated by full-width at half-maximum (FWHM) measurement of the time difference histogram [11]. The timing jitter characteristic itself is composed of two different parts: Gaussian's peak and the tail parts [12]. It should be noted that, temporal response of the absorbed photon in the depletion region of SPAD exhibits a Gaussian's shape peak for timing jitter characteristic [12].

Several studies could potentially model the avalanche breakdown process using Monte Carlo's based models in which two main carrier scattering mechanisms, includ-

ing intervalley phonon scattering and impact ionization are used for describing the carrier transport processes [13, 14]. However, using Monte Carlo's based model for timing jitter modeling is time consuming and complex due to considering an effective parabolic valley for both electrons and holes band structures [15]. To overcome these problems, a number of analytical studies are performed to directly calculate the timing jitter characteristic by solving the two-dimensional avalanche current equation [12, 16]. However, in these models, the multiplication time is numerically calculated [12, 16]. As a result, this approach was unable to accurately describe the multiplication time.

In this paper, a simple analytical model is proposed for Gaussian's peak response part of timing jitter in which the multiplication time is calculated using Fourier series. The proposed approach is an analytical solution as compared to previous model presented in [12] which calculates the multiplication time using numerical integration.

This paper is ordered as follows. In Section 2, the device structure and physical mechanisms involved in the timing jitter modulation are described. Section 3 explains model derivation of the Gaussian's peak response part of timing jitter, using a two-dimensional carrier spreading mechanism. In Section 4, device simulation setup, simulated ionization rates of electrons and holes, electric field and avalanche triggering efficiencies of carriers are described. The validation of the proposed model for timing jitter with measurements result is presented in Section 5, and Section 6 presents a summary of the paper.

2. Device structure and physical mechanism

Figure 1 shows the cross-sectional view of a typical p^+/n-well SPAD [17]. The depletion region of a p^+/n-well junction in x-direction is defined starting from the upper boundary of the depletion region W_1 to bottom boundary of depletion region W_2, as shown in Fig. 1. SPADs operate at an excess bias voltage V_{ex} above the diode breakdown voltage. Under the excess bias condition, when a photogenerated carrier reaches the avalanche multiplication region, the strong electric field causes impact ionization. Also, the generated free carrier can diffuse in y-z plane, finally causing an avalanche by diffusion-assisted avalanche spreading [12]. It should be noted that timing jitter

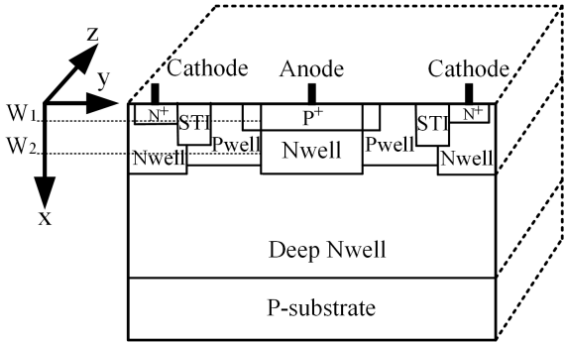

Fig. 1. The cross-sectional view of the p^+/n-well SPAD.

characteristic is composed of the photon detection delays in different regions. The delay of photon detection in the depletion region contributes to a Gaussian's peak of the timing jitter characteristic [9, 12]. In addition, photon absorption can occur in both undepleted top p^+ layer and undepleted bottom n-well layer (named as quasi-neutral regions). The generated minority carriers in the quasi-neutral regions may reach to the depleted region by diffusion mechanism, leading to avalanche breakdown triggering. These carriers determine the exponential tail in the timing jitter characteristic [12, 16].

3. Gaussian peak's modeling

The operation principle of the SPAD relies on the avalanche breakdown triggering, in which electron-hole pairs drift and diffuse in the depletion region in different y-z positions. According to the two-dimensional carrier spreading mechanism, the current continuity equation can be expressed by [12]

$$\frac{\mathrm{d}I}{\mathrm{d}t} = \frac{I}{\tau} + D\nabla^2 I \tag{1}$$

where, τ is the multiplication time, which is responsible for the avalanche multiplication process speed. I is the avalanche current and D is the transverse diffusion coefficient. A simplified first-order expansion for calculating τ is [12]

$$\tau = \frac{\tau_\mathrm{i}}{\frac{n}{F_\mathrm{b}}(F_\mathrm{b} - F_\mathrm{m})} \tag{2}$$

where, F_b is the electric field at the breakdown voltage and F_m is the maximum electric field of the pn junction. The maximum electric field depends on the diode excess bias voltage and depletion layer thickness. n is the device structure dependent fitting parameter, which is between 1 and 4 for a Si-based device [18]. τ_i is the intrinsic response time for carriers drift at saturated velocity. The intrinsic time with respect to a correct quasistatic approximation analysis for avalanche breakdown triggering, is given by [19]

$$\tau_\mathrm{i} = \frac{1}{|v_\mathrm{n}| + |v_\mathrm{p}|} \int_0^{W_2} \exp\left[-\int_x^{W_2} (\alpha - \beta)\mathrm{d}x'\right]\mathrm{d}x \tag{3}$$

Here, v_n and v_p are the electron and hole saturated velocities, α and β are the ionization coefficients for electrons and holes, respectively. In previous models of [12, 16] the ionization coefficients used in Eq. (3) were computed numerically. In contrast, in this section, a new analytical method is proposed to calculate the integrating factor $\exp\left[-\int_x^{W_2} (\alpha - \beta)\mathrm{d}x'\right]$. In this method, Eq. (3) gives the multiplication time by solving the integrating factor using Fourier series. First, the ionization rate difference between electrons and holes as function of depth is extracted from simulation result and it is

assumed that α-β is a periodic function with period of W_2. Then, Fourier series representation converges to α-β function on the interval $0 \le x \le W_2$.

$$\exp\left[-\int_x^{W_2}(\alpha-\beta)\mathrm{d}x'\right] = \exp\left\{-\int_x^{W_2}\left[a_0+\sum_{n=1}^{\infty}a_n\cos\left(\frac{2\pi nx}{T}\right)+b_n\sin\left(\frac{2\pi nx}{T}\right)\right]\mathrm{d}x'\right\}, \quad 0\le x\le W_2 \tag{4}$$

where, a_n and b_n are the Fourier coefficients; n is the number of cycles of the harmonic, which is considered as 3 to compute the Fourier series and T is α-β period.

$$\exp\left[-\int_x^{W_2}(\alpha-\beta)\mathrm{d}x'\right] = \exp\left\{\left[-a_0x-\frac{a_1}{\omega}\sin(\omega x)-\frac{a_2}{2\omega}\sin(2\omega x)-\frac{a_3}{3\omega}\sin(3\omega x)+\frac{b_1}{\omega}\cos(\omega x)+\frac{b_2}{2\omega}\cos(2\omega x)+\frac{b_3}{3\omega}\cos(3\omega x)\right]\Bigg|_x^{W_2}\right\} \tag{5}$$

Here, $\omega = 2\pi/T$. Since, the avalanche current flow is assumed along the electric field direction (x-direction), thereby to solve Eq. (1) the boundary conditions are as follows: $I_y(0) = I_y(L_y) = 0$ and $I_z(0) = I_z(L_z) = 0$. As a result, the avalanche current in different y-z positions is derived [12].

$$I(t) = \sum_{m,\,n=1}^{\infty} I_0\exp\left\{\frac{t}{\tau}-Dt\left[\left(\frac{n\pi}{L_y}\right)^2+\left(\frac{m\pi}{L_z}\right)^2\right]\right\}\sin\left(\frac{n\pi y}{L_y}\right)\sin\left(\frac{m\pi z}{L_z}\right) \tag{6}$$

where, I_0 represents the initial current, L_y is the depletion region width and L_z is the depletion region length. t is the avalanche buildup time which is the time needed for current to reach the threshold value level of 100 μA at different positions on the y-z plane [12]. By extracting the avalanche buildup time from Eq. (6) corresponding to 600 different photon impinging positions, the standard deviation σ and meantime μ used in analytical Gaussian's peak modeling are calculated.

$$\sigma = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(t_i-\mu)^2} \tag{7}$$

Here, N is the number of samples. The next step, for timing jitter histogram derivation is photon detection efficiency (PDE) calculation which is [17]

$$\text{PDE} = \int_0^{W_2} \alpha \exp(-\alpha x) P_{\text{pair}}(x) \mathrm{d}x \tag{8}$$

where, $P_{\text{pair}}(x)$ is the total avalanche triggering efficiency that either an electron or hole causes an avalanche event at different positions on the y-z plane. $\alpha \exp(-\alpha x)$ is the probability of photon's absorption in x-direction, here α is the absorption coefficient, which is wavelength dependent. Finally, the analytical model for Gaussian's peak response is given by [12]

$$G(\mu, \sigma, t) = \text{PDE} \exp\left[\frac{-(t-\mu)^2}{2\sigma^2}\right] \tag{9}$$

4. Device simulation and discussions

The main parameters, such as avalanche triggering efficiencies of electrons and holes, ionization rates of carriers and electric field used in the proposed model are obtained from simulation results using a commercially available device simulator [20]. This simulation is based on 0.15 μm standard CMOS process in which electric field dependent mobility (FLDMOB), Shockley–Read–Hall (SRH) recombination, impact ionization and Geiger mode are considered. Figure 2 shows *I–V* characteristic of introduced device in [17] which is verified with the mentioned simulation setup. The simulated breakdown voltage is about 16 V at room temperature, which is close to the measured result of 16.1 V [21].

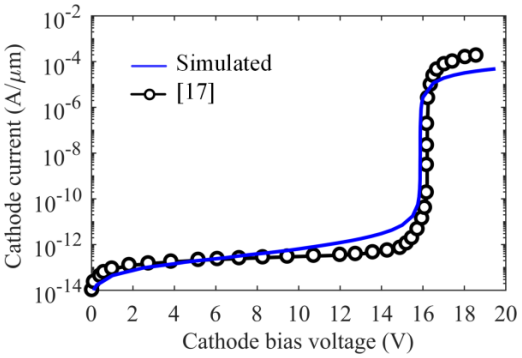

Fig. 2. Simulated *I–V* characteristic of p^+/n-well SPAD implemented in 0.15 μm standard CMOS process.

In Fig. 3 the variations of electric field as a function of depth at different excess bias voltages are shown. Peak value of the electric field is near the upper boundary of depletion region W_1 which is responsible for high ionization rate. In Fig. 4, the electrons and holes ionization rates are shown, in which ionization rates are enhanced with increase in the excess bias voltage. Due to the higher ionization rate of electrons in

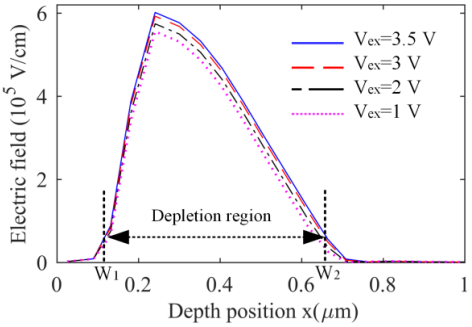

Fig. 3. Simulated electric field at different excess bias voltages.

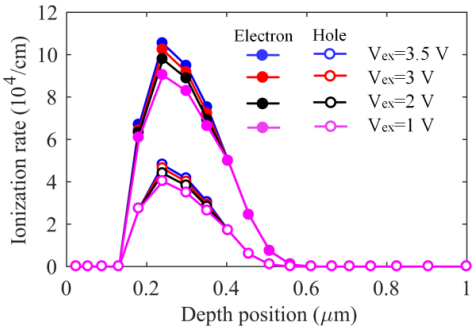

Fig. 4. Electron and hole ionization rates at different excess bias voltages.

comparison with holes ionization rate, electrons are the main carriers causing avalanche current.

The avalanche triggering efficiencies of electrons and holes at different excess bias voltages are shown in Fig. 5. It can be seen that the triggering efficiency for electron reaches to a maximum of 0.67 at the upper boundary of depletion region and decreases

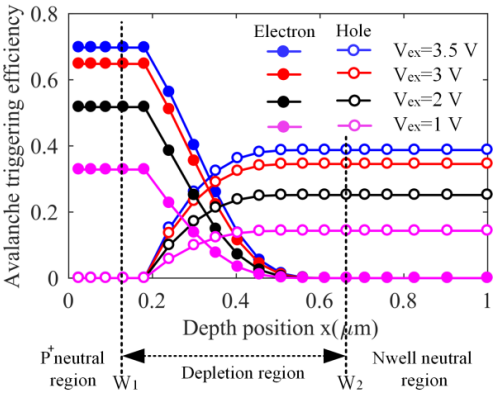

Fig. 5. Simulated avalanche triggering efficiency of carriers at different excess bias voltages.

to zero at the bottom boundary of depletion region. The avalanche triggering efficiencies of electrons and holes remain constant, in the quasi-neutral regions due to the negligible electric field in the mentioned regions [17].

5. Model validation and discussions

Figure 6 shows Fourier series representation of α-β function which has the period of W_2. This figure illustrates, for $n = 3$, the Fourier series converges to α-β on the interval $0 \leq x \leq W_2$ which results in a more accurate multiplication time. Unlike presented models in [19,22], Fourier series result includes the dependence of the ionization coefficients of carriers inside the depletion region depth position.

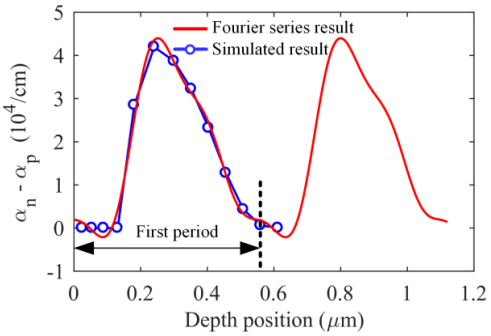

Fig. 6. Fourier series converging to the simulated ionization coefficients of carriers α-β.

To compare both analytical and numerical methods output accuracies, trapezoidal method is used for numerical integration. In Table 1 multiplication time and intrinsic time are calculated using Fourier series and trapezoidal numerical integration for SPAD implemented in 0.15 µm standard CMOS process. The accuracy of the proposed approach to calculate the timing jitter depends on the multiplication time. The difference between the calculated multiplication time from Fourier series and numerical integration produces the deviation in the FWHMs. In comparison with numerical method, the calculated FWHM of 101 ps using the proposed method is close to the measured result of 92 ps from [21] at $V_{ex} = 3.5$ V, as shown in Fig. 7. Hence, the proposed analytical method's accuracy in the FWHM calculation is improved by 25% with respect to the numerical method. It should be noted that, the simulated SPAD in this

T a b l e 1. The calculation results of both methods.

Technology	0.15 µm CMOS (at $V_{ex} = 3.5$ V; $n = 1.8$)
Calculated intrinsic time using Fourier series	1.9 ps
Calculated intrinsic time using numerical method	2.2 ps
Calculated multiplication time using Fourier series	9 ps
Calculated multiplication time using numerical method	13 ps

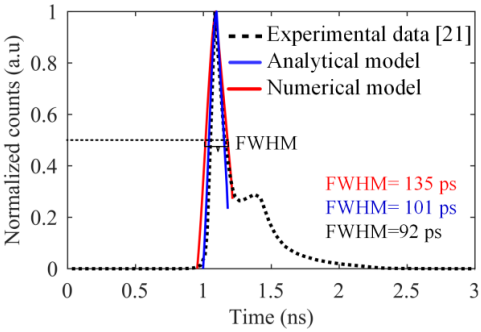

Fig. 7. The timing response of SPAD implemented in 0.15 μm standard CMOS process in [21] at the photon wavelength of 470 nm.

paper and fabricated SPAD in [21] show identical breakdown voltage, indicating similar doping profiles.

Moreover, the proposed model is validated for SPAD based on 0.18 μm standard CMOS process introduced in [12]. For absolute comparison between the proposed method and previous numerical method presented in [12], the main parameters such as avalanche triggering efficiencies of electrons and holes, ionization rates of carriers and electric field used in the proposed model are extracted from [12] at V_{ex} = 0.5 V. Finally, multiplication time and intrinsic time from numerical method and Fourier series are shown in Table 2. Figure 8 shows FWHM of 105 ps using the proposed method

T a b l e 2. The calculation results of both methods.

Technology	0.18 μm CMOS (at V_{ex} = 0.5 V; n = 1.5)
Calculated intrinsic time using Fourier series	1.2 ps
Calculated intrinsic time from [12]	1.32 ps
Calculated multiplication time using Fourier series	30 ps
Calculated multiplication time from [12]	33 ps

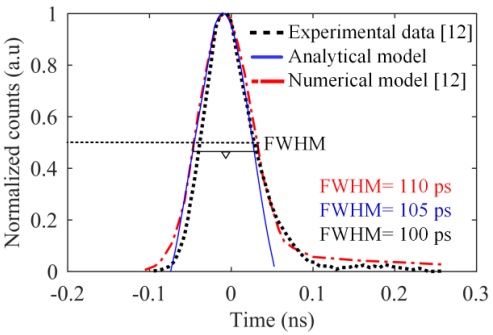

Fig. 8. The timing response of SPAD based on 0.18 μm standard CMOS process in [12] at the photon wavelength of 450 nm.

is close to the measured result of 100 ps. According to this figure, the proposed analytical method FWHM calculation improves the accuracy by 5% with respect to the previous numerical method.

6. Conclusion

A simple analytical model for Gaussian's peak response part of the timing jitter characteristic of SPAD is proposed using Fourier series in the multiplication time calculation. In comparison with previous method, this approach calculates the multiplication time more accurately. Finally, the developed analytical model is validated by the calculated Gaussian's peak response part of timing jitter characteristic and the reported measured results for different SPADs.

References

[1] Xu H., Pancheri L., Dalla Betta G.-F., Stoppa D., *Design and characterization of a p⁺/n-well SPAD array in 150nm CMOS process*, Optics Express **25**(11), 2017: 12765-12778. https://doi.org/10.1364/OE.25.012765

[2] Karami M.A., Amiri-Sani A., Ghormishi M.H., *Tunneling in submicron CMOS single-photon avalanche diodes*, Chinese Optics Letters **12**(1), 2014: 012501.

[3] Richardson J.A., Webster E.A.G., Grant L.A., Henderson R.K., *Scaleable single-photon avalanche diode structures in nanometer CMOS technology*, IEEE Transactions on Electron Devices **58**(7), 2011: 2028-2035. https://doi.org/10.1109/TED.2011.2141138

[4] Ratti L., Brogi P., Collazuol G., Dalla Betta G.-F., Ficorella A., Lodola L., Marrocchesi P.S., Mattiazzo S., Morsani F., Musacci M., Pancheri L., Vacchi C., *Dark count rate degradation in CMOS SPADs exposed to X-rays and neutrons*, IEEE Transactions on Nuclear Science **66**(2), 2019: 567-574. https://doi.org/10.1109/TNS.2019.2893233

[5] Ke S., Lin S., Huang W., Wang J., Cheng B., Liang K., Li C., Chen S., *Geiger mode theoretical study of a wafer-bonded Ge on Si single-photon avalanche photodiode*, Journal of Physics D: Applied Physics **50**(5), 2017: 055106. https://doi.org/10.1088/1361-6463/aa52b9

[6] Li H., Ren X., Ying L., Balasubramanian S., Klenerman D., *Measuring single-molecule nucleic acid dynamics in solution by two-color filtered ratiometric fluorescence correlation spectroscopy*, Proceedings of the National Academy of Sciences **101**(40), 2004: 14425-14430. https://doi.org/10.1073/pnas.0404295101

[7] Daube-Witherspoon M.E., Matej S., Werner M.E., Surti S., Karp J.S., *Comparison of list-mode and DIRECT approaches for time-of-flight PET reconstruction*, IEEE Transactions on Medical Imaging **31**(7), 2012: 1461-1471. https://doi.org/10.1109/TMI.2012.2190088

[8] Bronzi D., Villa F., Tisa S., Tosi A., Zappa F., *SPAD figures of merit for photon- counting, photon-timing, and imaging applications: a review*, IEEE Sensors Journal **16**(1), 2016: 3-12. https://doi.org/10.1109/JSEN.2015.2483565

[9] Spinelli A., Lacaita A.L., *Physics and numerical simulation of single photon avalanche diodes*, IEEE Transactions on Electron Devices **44**(11), 1997: 1931-1943. https://doi.org/10.1109/16.641363

[10] Acerbi F., Ferri A., Gola A., Cazzanelli M., Pavesi L., Zorzi N., Piemonte C., *Characterization of single-photon time resolution: from single SPAD to silicon photomultiplier*, IEEE Transactions on Nuclear Science **61**(5), 2014: 2678-2686. https://doi.org/10.1109/TNS.2014.2347131

[11] Karami M.A., Gersbach M., Yoon H.J., Charbon E., *A new single-photon avalanche diode in 90nm standard CMOS technology*, Optics Express **18**(21), 2010: 22158-22166. https://doi.org/10.1364/OE.18.022158

[12] SUN F., XU Y., WU Z., ZHANG J., *A simple analytic modeling method for SPAD timing jitter prediction*, IEEE Journal of the Electron Devices Society **7**, 2019: 261-267. https://doi.org/10.1109/JEDS.2019.2895151

[13] ZHOU X., NG J.S., TAN C.H., *A simple Monte Carlo model for prediction of avalanche multiplication process in silicon*, Journal of Instrumentation **7**(08), 2012: P08006. https://doi.org/10.1088/1748-0221/7/08/P08006

[14] PLIMMER S.A., DAVID J.P.R., ONG D.S., LI K.F., *A simple model for avalanche multiplication including deadspace effects*, IEEE Transactions on Electron Devices **46**(4), 1999: 769-775. https://doi.org/10.1109/16.753712

[15] PETTICREW J.D., DIMLER S.J., ZHOU X., MORRISON A.P., TAN C.H., NG, J.S., *Avalanche breakdown timing statistics for silicon single photon avalanche diodes*, IEEE Journal of Selected Topics in Quantum Electronics **24**(2), 2018: 3801506. https://doi.org/10.1109/JSTQE.2017.2779834

[16] SHOJAEE F., HADDADIFAM T., KARAMI M.A., *Jitter modulation by photon wavelength variation in single-photon avalanche diodes (SPADs)*, Optical and Quantum Electronics **53**(7), 2021: 397. https://doi.org/10.1007/s11082-021-02991-z

[17] XU Y., XIANG P., XIE X., HUANG Y., *A new modeling and simulation method for important statistical performance prediction of single photon avalanche diode detectors*, Semiconductor Science and Technology **31**(6), 2016: 065024. https://doi.org/10.1088/0268-1242/31/6/065024

[18] LAFORCE F., *Low noise optical receiver using Si APD*, Proceedings of the SPIE, Vol. 7212, Optical Components and Materials VI, 2009: 721210. https://doi.org/10.1117/12.809071

[19] KUVÅS R., LEE C.A., *Quasistatic approximation for semiconductor avalanches*, Journal of Applied Physics **41**(4), 1970: 1743-1755. https://doi.org/10.1063/1.1659100

[20] *Silvaco ATLAS Device Simulation Software User's Manual*, 2018.

[21] PANCHERI L., STOPPA D., *Low-noise single photon avalanche diodes in 0.15 μm CMOS technology*, [In] *2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, IEEE, 2011: 179-182. https://doi.org/10.1109/ESSDERC.2011.6044205

[22] HOLWAY L.H., *Electron-hole avalanches with constant ionization coefficients*, IEEE Transactions on Electron Devices **26**(6), 1979: 991-993. https://doi.org/10.1109/T-ED.1979.19532

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