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SIMULATION OF HIGH-EFFICIENCY INTERLEAVED STEP-UP DC-DC CONVERTER WITH COUPLED INDUCTORS TO USE IN RENEWABLE ENERGY SYSTEM

The majority of renewable energy sources deliver relatively low output voltage. In renewable energy systems high-efficiency high voltage gain step-up DC-DC converters are required as the interface between low voltage sources and the load. Therefore overall performance of the renewable energy system is strongly affected by the efficiency of step-up DC-DC converter itself. This paper presents high-efficiency interleaved step-up DC-DC converter with coupled inductors. Interleaved approach minimizes the current stress of the switches as well as the a sizes of the inductors but also allows reducing input current ripples. The other advantage of interleaving structure is the flexibility of number of phases extension. The number of working phases can be determined depending on the power requirements of the load. High efficiency is achieved by recycling the energy from leakage inductance present in practical coupled inductors. In order to re-use leakage energy voltage clamp circuit is applied. It allows to minimize voltage stress across the switches further improving the efficiency of interleaved DC-DC converter. The simulation carried out will present parametric and performance characteristics of the converter. Most efficient configuration and the number of phases will be discussed in this paper.

1. INTRODUCTION

The majority of renewable energy sources commonly used deliver electric power at the voltage of 20 V_{DC} to 70 V_{DC} (V_i). Therefore to adjust it to the electric grid standards that voltage should be stepped-up by the DC-DC converter to the system DC Bus voltage (V_o) of around 200 V_{DC} or 400 V_{DC} depending on the grid standards. DC-AC inverter produces the AC voltage that can be adjusted to use in the grid requirements. Simplified renewable energy system is depicted in Fig. 1. In this paper the performance of multi-phase selected topology of interleaved step-up DC-DC converter with coupled inductors will be characterized basing on PC computer simulations.

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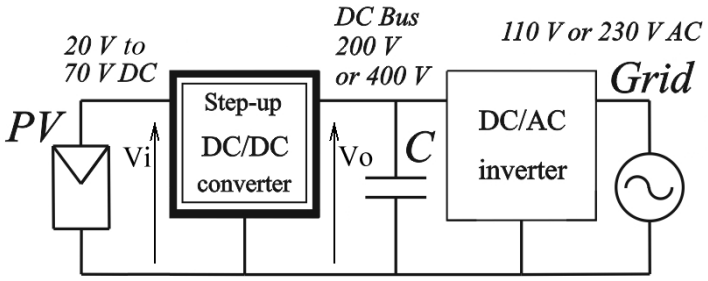

Fig. 1. Simplified renewable (photovoltaic) energy system diagram

2. INTERLEAVED STEP-UP DC-DC CONVERTER WITH COUPLED INDUCTORS TOPOLOGY

Input current delivered from renewable energy source is shared between a number of phases allowing reduction of inductor and semiconductor peak currents which leads to overall power loss reduction [1]. The other advantage of an interleaved topology is possibility to use smaller and cheaper components, flexibility of power transistor driving strategy as well as efficient input/output current ripple rejection [2].

2.1. Electrical Scheme

The interleaved step-up DC-DC converter is shown in Fig. 2. It is derived from single-phase flyback converter which is the simplest and hence the cheapest topology. It consists of *n* phases connected in parallel.

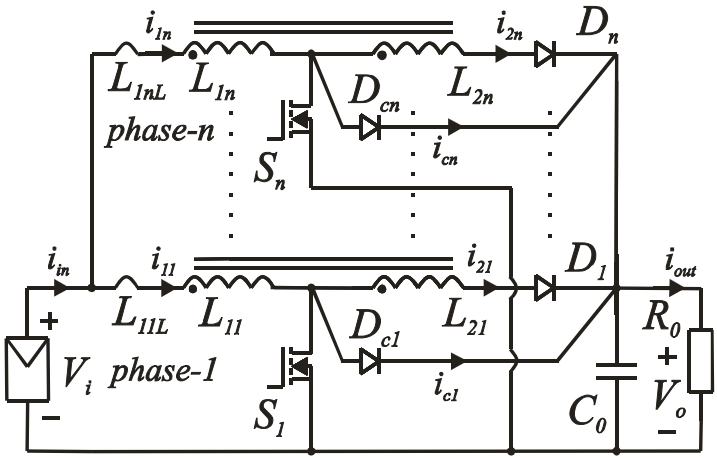

Fig. 2. Interleaved step-up DC-DC converter

In contrary to the legacy flyback topology [3] the windings of both primary L_{1k} and secondary L_{2k} inductors are connected together (k = 1,2, ..., n). That allows the input inductor leakage L_{1kL} energy to be efficiently recycled directly to the output through D_k diode. D_k acts as clamping diode preventing transistor drain voltage to excess the level of V_o at transistor turn off transient.

2.2. Principle of operation

Assuming continuous conduction mode there are three modes of operation in one switching cycle (T) of interleaved step-up DC-DC converter. Fig. 3 describes the work of n = 3-phase converter. The gate driving signals of transistors S_1, S_2 and S_3 are phase shifted by $2\pi/3$ electrical angle and switched at duty cycle D = 0,66 (Fig. 3a, 3b and 3c). At the example of k-th phase (k = 1,2, ..., n) with assumption of ideal coupling between L_{1k} and L_{2k} (K = 1) in mode-1 when transistor S_k is switched on the energy is transferred from input to the primary inductance L_{1k} and leakage inductance L_{1kL}. In this mode L_{1k} current (i_{1k}) can be describe as:

$$\frac{di_{1k}}{dt} = \frac{v_i}{L_{1k} + L_{1kL}}, \qquad t = [t_0, t_1] \tag{1}$$

The energy stored in leakage inductance is discharged to output capacitor C_0 through forward biased diode D_{Ck} in mode-2.

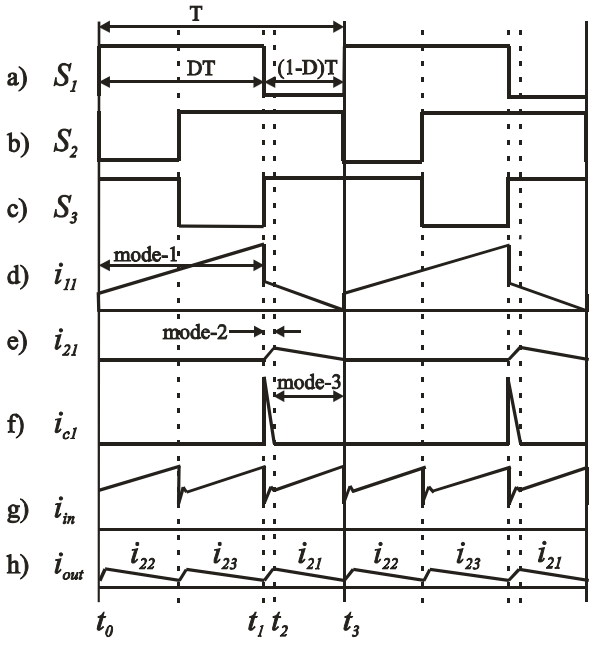

Fig. 3. Key waveforms of interleaved step-up DC-DC converter during operation modes 1 to 3

$$\frac{di_{1kL}}{dt} = \frac{v_i - v_0}{L_{1kL}} \cdot \frac{N}{N+1}, \qquad t = [t_1, t_2] \tag{2}$$

where N is turns ratio of coupled inductors L_{2k} and L_{1k}.

In mode-3 when the leakage inductance current value is zero and transistor S1 is turned off and the output diode D_1 is on, the primary inductance current is:

$$\frac{di_{1k}}{dt} = \frac{v_i - v_0}{L_{1k}} \cdot \frac{1}{N+1}, \qquad t = [t_2, t_3] \tag{3}$$

Thus output voltage level regulation is accomplished by varying the duty cycle of the switches.

The voltage gain of the converter can be derived from:

$$\frac{V_0}{V_i} = 1 + \frac{D(1+N)}{1-D} \tag{4}$$

Aggregate output current (i_0) is composed of each individual phase currents (Fig. 3h - with C_0 disconnected) and is further filtered by C_0. Output voltage (V_0) regulation (4) can be achieved by adjusting the duty cycle of the switches [4].

3. PSPICE SIMULATION MODEL OF INTERLEAVED STEP-UP DC-DC CONVERTER WITH COUPLED INDUCTORS

Fig. 4 presents PSpice model of n = 2-phase interleaved step-up DC-DC converter. Fast power MOSFET transistors (IRFP27N60K, R_{DSon_typ} = 180mΩ) are driven by phase shifted square waves generated by V_{gk} voltage sources. Gate driving circuit comprises C_{gk} (10nF), D_{gk} and R_{gk} (10Ω) chosen to optimize turn off time of the transistors. For all the tests switching frequency f_S is 20kHz.

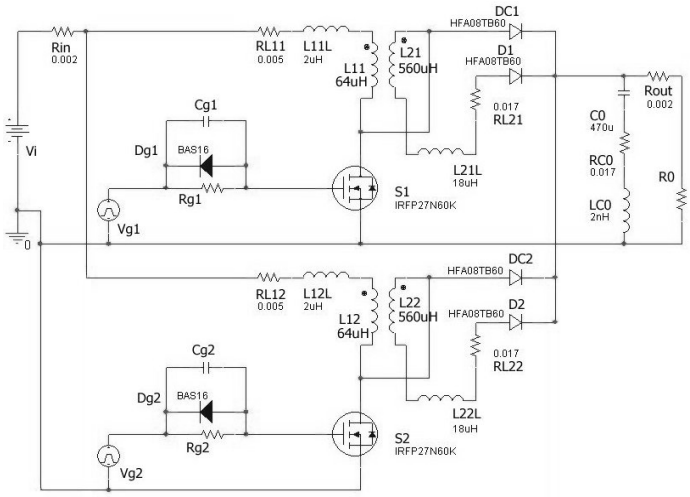

Fig. 4. PSpice model of 2-phase interleaved step-up DC-DC converter

The output diodes D_k and clamp diodes D_{ck} are fast recovery HFA08TB60. The power semiconductors the transistors and the diodes are 600V rated.

R_{in} and R_{out} represent input and output lead resistances while R_{C0} and L_{C0} describe real capacitor parasitic resistance and inductance respectively.

L_{1k} together with L_{2k} are primary and secondary windings of coupled inductor. Input leakage inductance L_{1kL} is 2µH. L_{2kL} is the output leakage inductance [5] which together with R_{L1k} and R_{L2k} which are primary and secondary winding resistances formulate a model of the coupled inductors with turns ratio $N = 3$ and inductance coupling coefficient $K = 0.97$. All the values of parameters listed above were confirmed with MT4090 RLC meter measurements.

4. TRANSIENT CHARACTERISTICS

Fig. 5 presents simulation waveforms of 3-phase interleaved step-up DC-DC converter. The output voltage V_0 for given conditions is 270V. Fig. 5a shows transistors S_1 drain to source voltage which is effectively clamped not exceeding V_0. Reverse recovery current of D_1 causes negative voltage overshoot which shows V_{D1} plot. The peak current of D_{C1} is equal to the peak current of transistor S_1 current at the end of conduction (Fig. 5c). The value of output current I_0 is 3.17A.

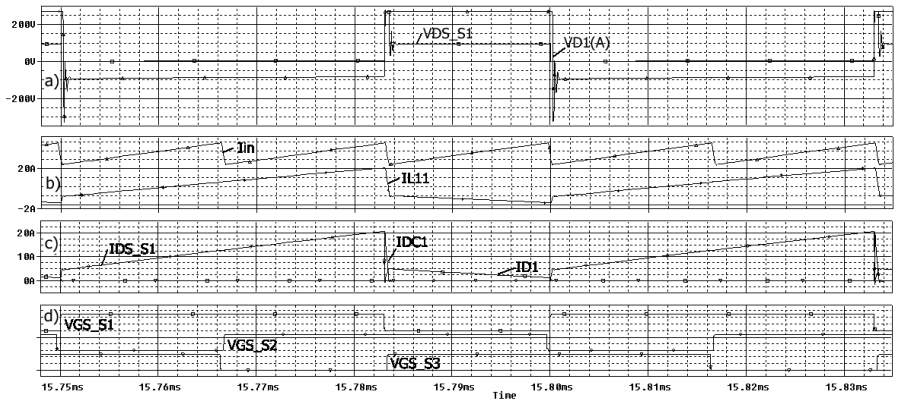

Fig. 5. Transient waveforms of a) drain to source voltage V_{DS} of S_1 and output diode voltage at anode side V_{D1}, b) input current I_{in} and primary inductor I_{L11} (phase 1), c) transistor S_1 current I_{DS_S1}, clamping diode current I_{DC1} and output diode current I_{D1}, d) gate to source transistor driving voltages at f_S = 20kHz, V_{in} = 35V and $D = 0.66$

5. PARAMETRIC CHARACTERISTICS

Parametric characteristics present the dependency of interleaved step-up DC-DC converter on the number of phases. They cover 3-phase (3ph) to 7-phase (7ph) topologies. Simulation was carried out at following conditions: input voltage

V_i = 35V, average input current I_i = 42A, switching frequency f_S = 20kHz, load resistance R_0 = 85Ω, output voltage V_0 = 350V and output power P_0 of 1.5kW.

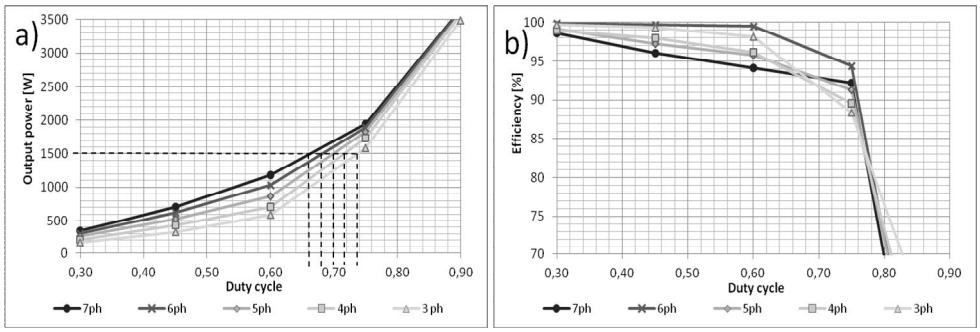

Fig. 6. Parametric characteristics of a) output power P_0 , and b) efficiency η vs. duty cycle

Fig. 6a shows that to achieve 1.5kW of output power the range of duty cycle is 0.66 to 0.74 depending on the number of phases. For 5- or more phase topologies the efficiency over 92% can be obtained within above duty cycle range (Fig. 6b).

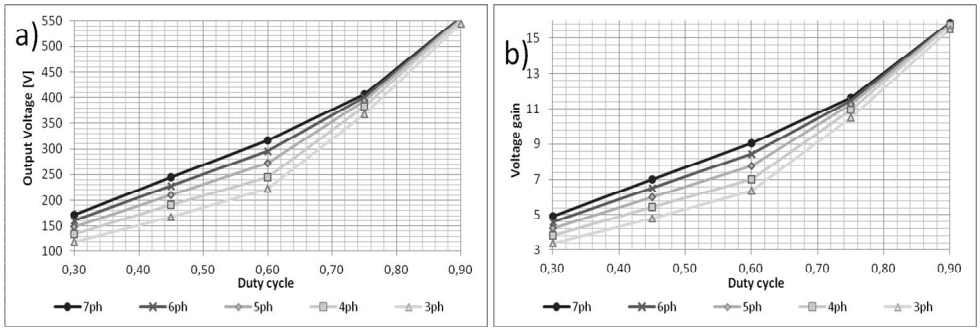

Fig. 7. Parametric characteristics of a) output voltage V_0, and b) voltage gain D vs. duty cycle

The output voltage can be held at the level of 350V at the duty cycle within the range of 0.66 to 0.74 for different number of phases in use (Fig. 7a) or depending on the load it can be easily adjusted by varying the duty cycle. The more phases are in use the same value of voltage gain can be achieved at lower duty cycle (Fig. 7b).

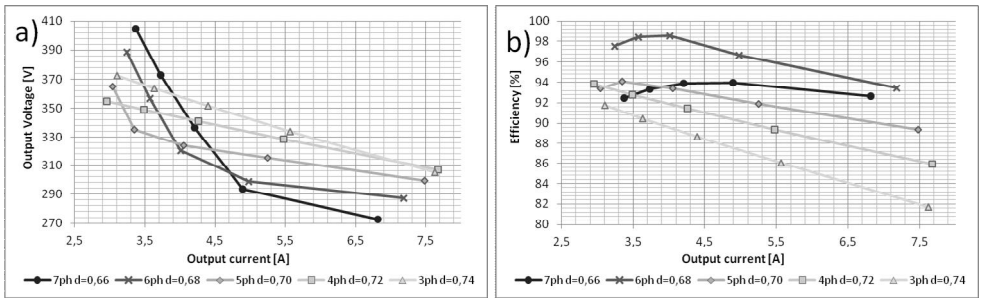

Fig. 8. Load regulation characteristic a), and efficiency η vs. output current I_0 plot b)

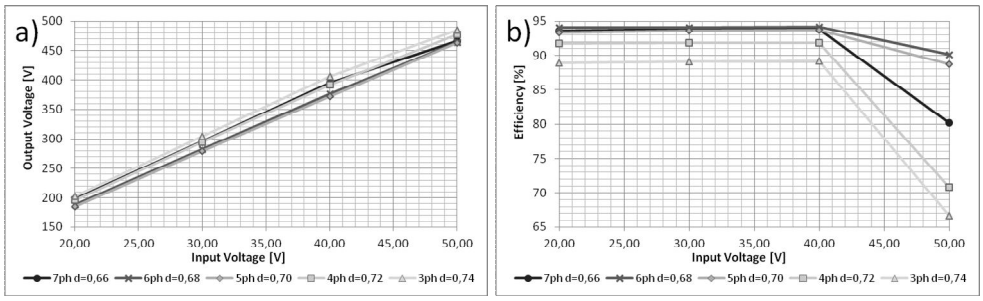

Fig. 9. Line regulation characteristic a), and efficiency η vs. input voltage Vi plot b)

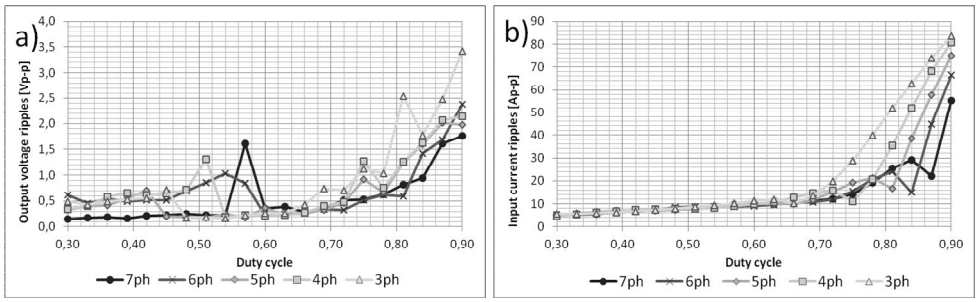

Fig. 10. Output voltage ripples a), and input current ripples b) vs. duty cycle D

Line regulation of converter is nearly linear across input voltage range tested (Fig. 9a) but load regulation is linear only for 3- and 4-phases. In both cases the efficiency reported in Fig. 8b and in Fig. 9b is higher than 92% for 5- or more phases at up to 40V of input voltage. The output voltage ripples are at relatively small level (lower than 4V peak-to-peak) but there is the range of duty cycle (0.60 to 0.72) where the ripples are even smaller not exceeding 0.7 V peak-to-peak (Fig. 10a). However input current ripples are high enough they remain at the lowest levels for the duty cycle up to 0.70 for 3-phase topology and up to 0.75 for 7-phases (Fig 10b).

6. CONCLUSION

PC computer based simulation tests confirmed high efficiency of 1.5kW interleaved step-up DC-DC converter with coupled inductors. Five or more interleaved phases can be used to achieve the best performance. Proposed topology can be effectively utilized in low-voltage renewable energy systems. However simulation results look consistent real laboratory measurement results may vary because of component model inaccuracies.

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