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Neural Network-Based Optimisation of Sinusoidal PWM Controller for VSI-Driven BLDC Motor

Special issue paper

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Abstract: Although increasing the number of switches increases the switch losses, most designed controllers focus on controlling an inverter circuit with more than six switches. The paper aims to address this issue that arises in implementation of the voltage source inverter (VSI) for brushless DC (BLDC) motors. It optimises the sinusoidal pulse width modulation (PWM) controller, minimising total harmonic distortion (THD) while keeping the VSI's circuit at six switches to avoid increased switching losses. This was achieved by applying an artificial neural network (ANN) to generate a signal, which combines with the already existing reference and carrier signals. The addition of the new signal to the existing signals contributed to generating more pulses compared with the conventional sinusoidal PWM. Simulink was used to design the system and analyse its performance with the conventional and neutral point clamped (NPC) VSI systems. Results indicated that the proposed system performs better when controlled with an LCC filter. Compared with the control experiments, its output waveform has the lowest THD value, which is 6.04%. The switching losses of all the systems were also computed. Results from the computation indicated that the proposed system is capable of reducing the switching losses by 0.6 kW compared with the NPC VSI brushless DC motor (BLDCM) system. BLDCM speed was tested across various conditions; the results are reported in Section 5.

Keywords: *artificial neural network • harmonics • sinusoidal PWM • inverter • MATLAB/simulink*

1. Introduction

Three-phase voltage source inverters (VSIs) are frequently applied in brushless DC motor (BLDCM) drives for various industrial and automotive applications. Nevertheless, optimising the performance of VSI-based BLDCMs presents several challenges that require engineering solutions. One of the key issues is the need to balance the switching losses and the harmonic content of the output waveform. Many researchers propose increasing the number of switches to reduce the harmonic content (Haw et al., 2021; Sagvand et al., 2023; Shahir and Babaei, 2016; Vahedi and Trabelsi ., 2019; Ye et al., 2019). Thus, recent designed controllers are used in controlling inverters with more than six semiconductor switches. Nonetheless, it has been reported that a higher number of semiconductor devices and capacitors lead to increased losses and costs, and reduced efficiency (Sagvand et al., 2023). The study proposes a VSI-driven system for BLDCM. It aims to minimise switching loss compared with the neutral point clamped (NPC) VSI. The proposed system utilises fewer switches to minimize the total harmonic distortion (THD) in the output waveform. Furthermore, the system incorporates an LCC low pass filter to enhance the output voltage waveform, surpassing both the conventional VSI-driven BLDCM and NPC VSI-driven BLDCM systems.

To circumvent the need for more capacitors and semiconductor devices, enhancing the VSI controller is preferred. This study aims to optimise the conventional sinusoidal pulse width modulation (PWM) by integrating an artificial neural network (ANN) generated signal with the existing reference and carrier signals. Thus, by incorporating an ANN signal to the conventional sinusoidal PWM, the system succeeded in reducing the THD of the output waveform

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Parameter	Value
Stator phase resistance (Rs)	0.2 Ω
Stator phase inductance (Ls)	0.5 mH
Flux linkage	0.175
Back EMF flat area	120°
Inertia	0.12 kg/m^2
Viscous damping	0.005 Nms
Pole pair	4

Table 1. Parameters of the BLDCM used in testing the proposed controller.

with fewer switches. The use of fewer switches contributed to the reduction of switching losses compared with the NPC VSI-driven BLDCM system. The proposed controller was tested on VSI-driven BLDCM to assess its harmonics efficiency. Table 1 presents the parameters of the BLDCM used in the test.

To validate the proposed system, a conventional-based VSI system and an NPC VSI-based system were designed for comparison. The conventional-based VSI circuit comprises 6 semiconductor switches, with 2 pairs at each leg of the inverter, while the NPC VSI consists of 12 semiconductor switches, with 4 pairs at each leg. The switch losses, along with the THD present in the output waveform of the system, were compared for analysis. The rotor speed of the BLDCM was also compared under different torque conditions. Results from the comparison demonstrate that the proposed system performs better in minimising the switching losses compared with the NPC VSI-driven system. Moreover, the system produces the best voltage output waveform when connected to the suggested LCC filter. Finally, the suggested system has a low starting speed compared with the conventional and NPC VSI-driven systems.

2. Theoretical Framework

2.1. Related works

Odeh et al. (2021) conducted a study on a single-carrier-based sinusoidal PWM topology for a cascaded H-Bridge (CHB) multilevel inverter. The objective of the work was to propose a seven-level inverter that would reduce the THD in the output voltage waveform. To achieve this, the researchers developed a single-carrier-based sinusoidal PWM technique to control the semiconductor switches of the CHB inverter. The findings of the research proved that the proposed system has the ability to reduce the THD content. However, the use of 24 semiconductor switches in the inverter contributed to increased switch losses and higher cost.

Shilpa (2021) proposed a cascaded multilevel inverter with a reduced switch count. The primary objective of the study was to develop an H-bridge inverter that has fewer switches while improving on the output voltage waveform. To achieve this, the researchers developed a multicarrier-based sinusoidal PWM controller for the inverter circuit, which utilised 10 semiconductor switches. Although the researchers demonstrated that the proposed system produces a superior output waveform, the utilisation of an inverter circuit with more than six semiconductor switches increases the cost and switching losses.

Antar et al. (2020) developed a 27-level CHB VSI for sensorless control of induction motors. The main objective of the research was to find an inverter circuit that would minimise the THD of the output waveform. To achieve this, a modified asymmetric sinusoidal PWM technique was proposed to control the 36 available semiconductor switches in the circuit. Although the researchers successfully reduced the THD in the output waveform, the use of 36 semiconductor switches in the development of the inverter circuit leads to an increase in the switching losses and system cost.

Palanisamy et al. (2020) designed a novel multilevel inverter with a reduced number of semiconductor switches. The main objective of the study was to develop a 15-level inverter that would balance both switching losses and the THD of the output voltage waveform. To achieve this, the researchers developed a multicarrier sinusoidal PWM controller to control the switches in the proposed inverter. The findings demonstrated a reduced THD in the output voltage waveform. However, the use of 10 semiconductor switches in the inverter circuit contributes to an increase in cost and switching losses.

Mahmud et al. (2019) conducted an analysis on the application of sinusoidal PWM topology on a five-level H-bridge/neutral point clamped (H-NPC) inverter. The study focused on minimising the THD in the inverter circuit. To achieve this, an H-NPC inverter circuit was constructed using eight semiconductor switches. The circuit was controlled using a multicarrier-based sinusoidal PWM technique to reduce the harmonic content of the output waveform. The results of the study demonstrated that the proposed system effectively reduced the harmonic content. However, the inclusion of additional semiconductor switches would result in increased switching losses and higher system costs.

Current researchers focus on improving the output waveform of an inverter by developing an advanced controller to control an inverter circuit with more than six semiconductor switches. However, in addition to the switching frequency, which contributes to switching losses, the inclusion of more semiconductor switches will increase the cost and switching losses of the system. Therefore, there is a need to maintain the standard six semiconductor switches of a three-phase inverter while advancing the controller of the inverter circuit.

To achieve this objective, a modified ANN-based sinusoidal controller was proposed, along with the design of an LCC filter. The performance of the proposed inverter system was compared with that of a traditional three-phase inverter and an NPC inverter to demonstrate its ability to balance the switching losses and reduce the THD present in the output waveform of a VSI-driven BLDCM system.

2.2. Artificial neural network

An ANN was implemented using a supervised feedforward network architecture. Thus, the model was trained with a target output (Johnson, 2023). The network consists of three layers: an input layer with five neurons, a hidden layer with five neurons and an output layer with three neurons. The input layer receives data from three reference signals and two carrier signals, while the output layer produces three control signals generated by combining the reference and carrier signals. Figure 1 illustrates the image of the proposed ANN.

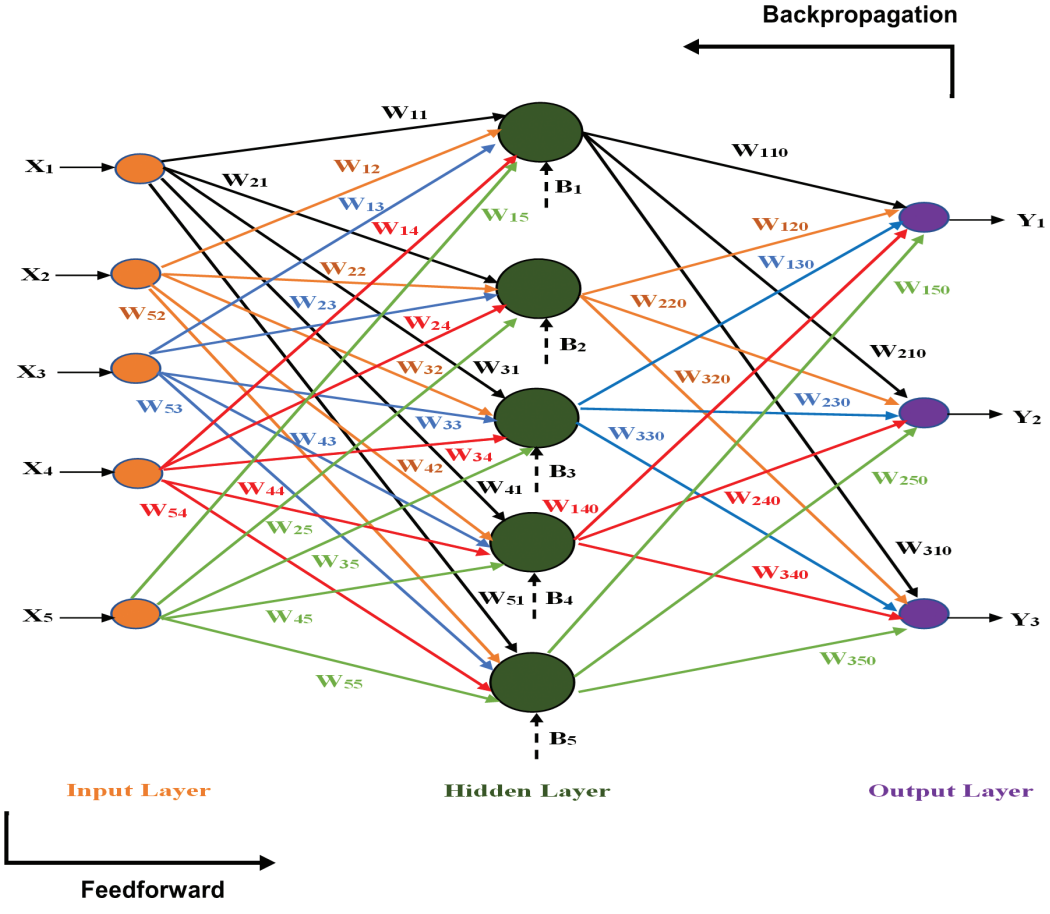

Fig. 1. Structure of proposed ANN.

The arrows labelled 'W' with a peculiar subscript in Figure 1 represent the weight between the nodes. These weights play a role in modifying the input data within the hidden layer. Random values ranging from 0 to 1 are assigned to the weights. In addition to weights, bias, labelled as B1, B2, B3, B4 and B5, contribute to storing information at the node. The bias is also needed to shift the activation function either towards the left or right side of the plane. The input, weights and bias combine to form the weight sum at a particular node. For instance, considering the first node, the weighted sum can be expressed mathematically as:

$$V = (W_{11} \times X_1) + (W_{12} \times X_2) + (W_{13} \times X_3) + (W_{14} \times X_4) + (W_{15} \times X_5) + B_1 \tag{1}$$

The activation functions are fundamental mathematical operations utilised to evaluate the significance of an input within a network's neuron (GeeksforGeeks, 2018). The tansig, the logsig and the purelin activation functions were applied to the input, hidden and output layers, respectively, to regulate data across the network's nodes. Eqs (2)–(4) present the mathematical expressions corresponding to each activation function:

$$tansig(n) = \frac{2}{1+e^{-2n}} - 1 \tag{2}$$

$$logsig(n) = \frac{1}{1+e^{-n}} \tag{3}$$

$$purelin(n) = n \tag{4}$$

where n represents the number of iterations.

The network was trained using the trainlm function, which utilises the Levenberg–Marquardt optimisation (LMO) algorithm to update the weight and bias values. This numerical optimisation technique has several advantages over other algorithms (Xiao et al., 2014; Yan et al., 2021), with the primary benefit being its ability to achieve accurate results with less training data. The LMO technique provides an estimation of Hessian (H) matrices, $H = J^T J$, in the following Newton-like updates:

$$X_{k+1} = X_k - \left[J^T + \mu I\right]^{-1} J^T e \tag{5}$$

In order to achieve the Hessian matrices approximation in the Newton's method, the scalar value, μ, was set to 0.

Throughout the computation process, increasing the value of μ enabled calculation of the gradient value with a smaller step size. Conversely, decreasing the performance function and subsequently reducing the value of μ, led to a larger successive step. The performance function was estimated with the Hessian matrices, that is $H = J^T J$. Whereas the gradient was computed mathematically as:

$$g = J^T e \tag{6}$$

where e and J represent the error and Jacobian matrices, respectively.

The error criterion that was considered for training the network is the mean square error (MSE). It can be mathematically expressed as:

$$MSE = \frac{1}{n}\sum_{i=1}^{n}\left(y - \tilde{y}\right)^2 \tag{7}$$

where n = the number of iterations and $y - \tilde{y}$ = the difference between the actual and predicted value.

To update the weight of the network and minimise the MSE, the error back propagation (BP) learning algorithm was utilised. This weight updating process is expressed mathematically as follows:

$$w(k+1) = w(k) - \eta g(k) \tag{8}$$

where η and $g(k)$ represent the learning rate and gradient vector, respectively.

By utilising the chain rule base, the gradient vector value was computed in the backward mode. Table 2 shows the parameters of the ANN data used in training the proposed network.

To train the system, 70% of the gathered data was utilised, while the remaining 30% was reserved for validation. The test results demonstrated the proposed ANN's capacity to reduce harmonic distortion in the proposed controller. The outcome of the network training can be observed in Figures 2 and 3.

Parameter	Value
Type of network	Feedforward/backpropagation
Learning algorithm	Trainlm
Epoch	1,000
Convergence limit	1.0×10^{-12}
Number of input layers	5
Number of hidden layers	5
Number of output layers	3
Activation function for input layer	tansig
Activation function for output layer	purelin
Activation function for hidden layer	logsig

Table 2. Parameters of proposed ANN.

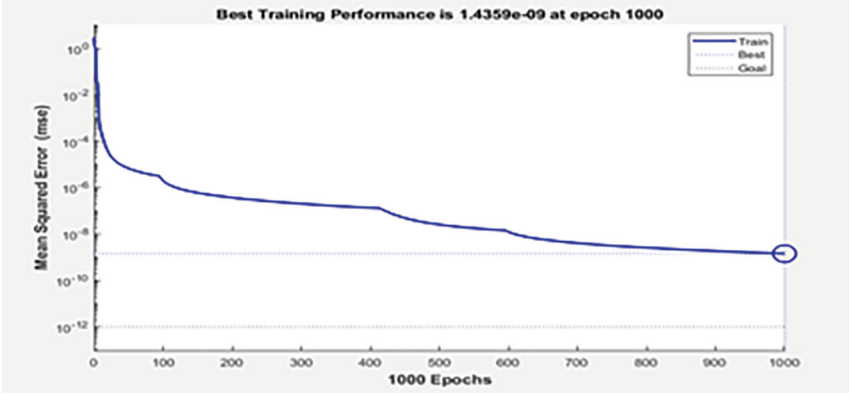

Fig. 2. Mean square error output chat after the training.

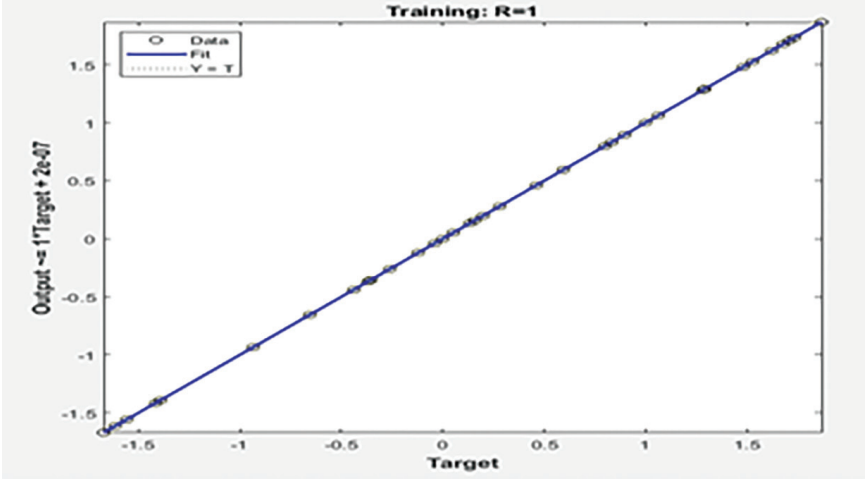

Fig. 3. Output of regression curve after the training.

2.3. Proposed signals for pulses generation

It has been documented multiple times that sinusoidal PWM is a distinctive method employed in managing the switches of an inverter (Addo-Yeboa and Owusu, 2022; Awate and Wagh, 2016). This technique for inverter control employs a sinusoidal reference signal and a sawtooth carrier signal to produce asymmetrical pulses for altering the switching states of the inverter.

The proposed switching approach utilised a modified sinusoidal PWM technique. To begin with, two triangular wave signals were produced by implementing Eqs (9) and (10):

$$C_1(x) = -1 + 2\left|round(f_s x) - f_s x\right| \tag{9}$$

$$C_2(x) = 2\left|round(f_s x) - f_s x\right| \tag{10}$$

where $C_1(x)$ = output of the first triangular signal, $C_2(x)$ = output of second triangular signal and f_s = switching frequency = 500 Hz x = period of signal

Three sinusoidal signals with a phase shift of 120° were also generated by applying Eqs (11)–(13):

$$R_1(x) = sin(100\pi x) \tag{11}$$

$$R_2(x) = sin\left(100\pi x + \frac{2\pi}{3}\right) \tag{12}$$

$$R_3(x) = sin\left(100\pi x - \frac{2\pi}{3}\right) \tag{13}$$

Subsequently, the five output signals, $C_1(x), C_2(x)$, $R_1(x)$, $R_2(x)$ and $R_3(x)$, served as an input of the proposed ANN algorithm.

In order to obtain a target for the proposed supervised learning ANN algorithm, a target output was obtained from the five signal outputs. Mathematically, the target outputs, $y_1(x), y_2(x)$ and $y_3(x)$ were expressed as:

$$y_1(x) = R_1(x) - \left[C_1(x) + C_2(x)\right] \tag{14}$$

$$y_2(x) = R_2(x) - \left[C_1(x) + C_2(x)\right] \tag{15}$$

$$y_3(x) = R_3(x) - \left[C_1(x) + C_2(x)\right] \tag{16}$$

To increase the number of asymmetrical pulses for controlling the gates of the inverter switches, the output signal of the ANN was replaced with the sinusoidal waveform in a conventional sinusoidal PWM controlling technique.

2.4. LCC low pass filter

Low pass filters are comprised of passive components that are connected in a circuit to weaken high-frequency signals (Tomáš Zedníček, 2018). An LCC filter was installed between the output of the inverter and the BLDCM to decrease the inverter's harmonic content more effectively. The LCC filter's single line diagram is displayed in Figure 4.

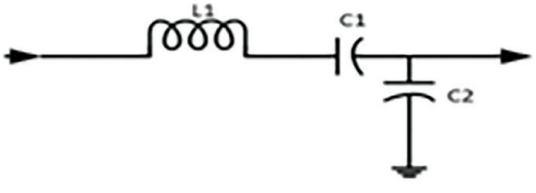

Fig. 4. Single line diagram of proposed low pass filter.

The values of the C_1 and L_1 were selected by applying Eqs (17) and (18), which is given as:

$$L_1 = \frac{V_{dc}}{4 \times \triangle I_{LMAX} f_s} \tag{17}$$

$$C_1 = \left(\frac{10}{2\pi f_s}\right)^2 \left(\frac{1}{L_1}\right) \tag{18}$$

where V_{dc} = input voltage of the inverter, $\triangle I_{LMAX}$ = 20% of the load's rated current and f_s = switching frequency.

A fixed capacitor (C_2) with a value of 50 μF was selected to attenuate the low-frequency signal of the series connection of C_1 and L_1. The proposed LCC filter was connected between the BLDCM and all the VSI-based circuits under discussion in order to observe its impact on the systems. The findings of the VSI systems after connecting the LCC filter has been discussed in Section 4 of this paper.

2.5. Switching losses

Switching losses in semiconductor switches are generated during transitions between the blocking and conducting states. In the context of an inverter circuit, two primary factors contribute to switching losses: the switching frequency and the number of semiconductor switches employed in the circuit design. Increasing the switching frequency of the controller results in higher switching losses (Maniktala, 2012). Similarly, a greater number of semiconductor switches in the system lead to increased switching losses (Sagvand et al., 2023).

When a metal-oxide semiconductor field-effect transistor (MOSFET) or any other three-terminal semiconductor switch is incorporated into a circuit as shown in Figure 5, it generates a switching current (I_{sw}) and a switching voltage (V_{sw}) to regulate the load (L). The waveforms of I_{sw} and V_{sw} can be illustrated as depicted in Figure 6.

Based on the output waveforms of I_{sw} and V_{sw}, the rising time (t_{on}), falling time (t_{off}), maximum switching voltage (v_m) and maximum switching current (i_m) can be measured. These parameters are then used to calculate the switching losses, as expressed in the mathematical formula (Rohm.com, 2018):

$$P_{sw} = \frac{v_m i_m (t_{on} + t_{off}) f_s}{2} \tag{19}$$

where P_{sw} = switching loss, v_m = maximum switching voltage, i_m = maximum switching current, t_{on} = rising time of switching current, t_{off} = falling time of switching current and f_s = switching frequency.

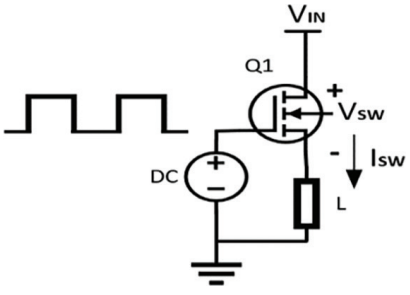

Fig. 5. Current switching with MOSFET.

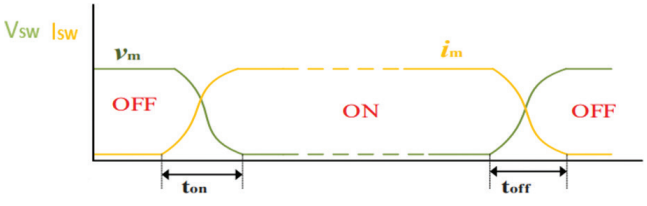

Fig. 6. Output waveform of switching current and voltage.

3. Methodology

3.1. Block diagram of proposed system

Figure 7 illustrates the block diagram of the proposed system.

Referring to Figure 7, a pair of triangular signals and three sinusoidal signals were created utilising Eqs (2)–(6). These signals were utilised as input to the ANN. The resulting signals from the ANN were combined with the triangular and sinusoidal signals to generate pulses for controlling the inverter switches. An LCC filter was then employed to link the output of the inverter to the BLDCM, producing a pure sinewave signal. The pure sinewave signal was then employed for controlling the BLDCM.

3.2. Design of conventional sinusoidal PWM

Prior to the design of the proposed system, a single-carrier sinusoidal PWM was designed to serve as a control experiment for the proposed system. The internal structure of the designed traditional controller is shown in Figure 8.

In Figure 8, a combination of sinusoidal waveform and sawtooth waveform was utilised to generate pulses for the switches at one leg of the inverter. Specifically, the 'A' sinusoidal wave was combined with the sawtooth wave to

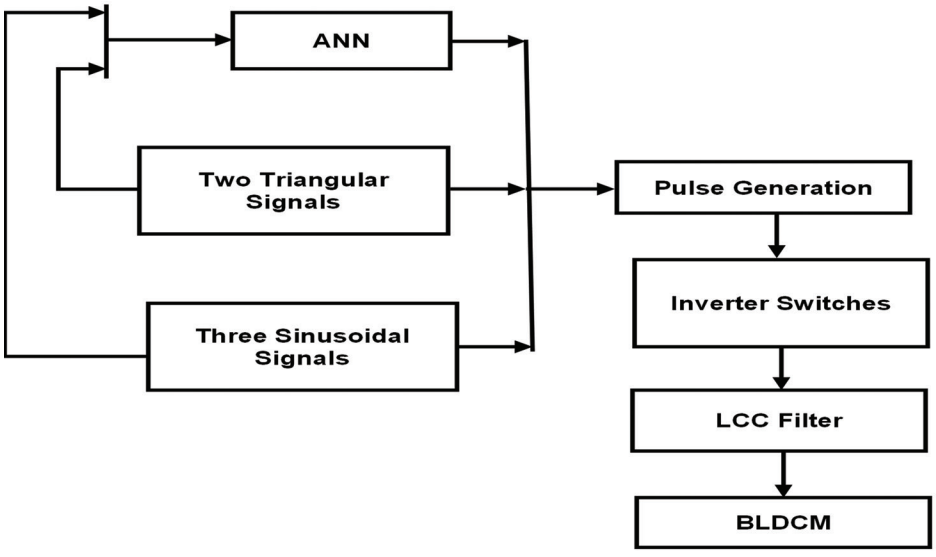

Fig. 7. Block diagram of proposed system.

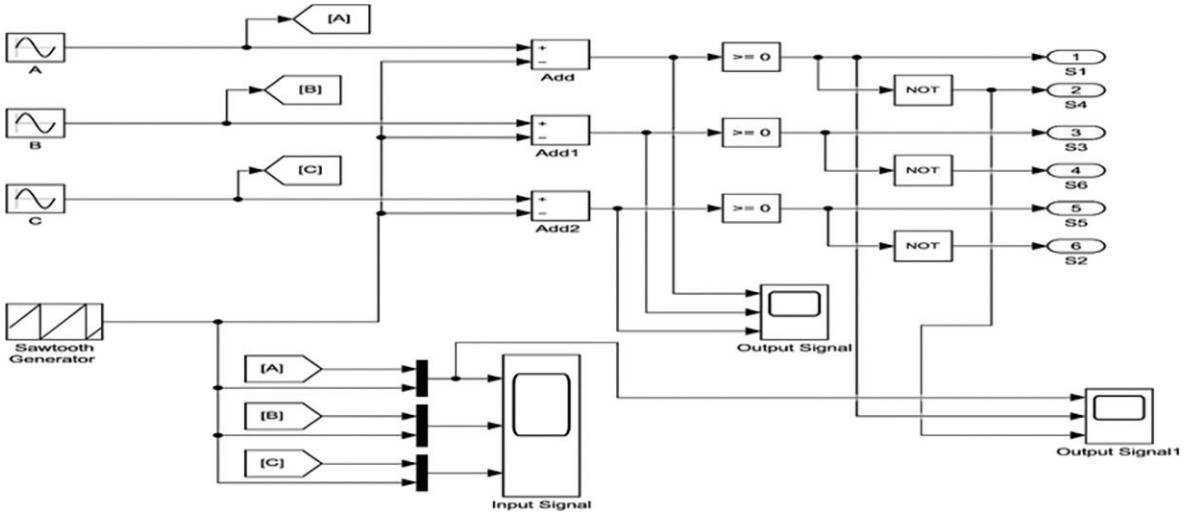

Fig. 8. Design of conventional sinusoidal PWM controller.

produce pulses at the S1 and S4 terminals. The resulting output of the pulses generated at one leg of the inverter is shown in Figure 9.

The conventional sinusoidal PWM controller was employed to regulate a three-phase VSI-driven BLDCM system, as shown in Figure 10.

Figures 11 and 12 display the voltage waveform obtained from the conventional VSI-driven system both before and after implementing the proposed LCC Filter, designed according to Eqs (17) and (18).

The analysis of the output waveform's harmonic content was conducted to arrive at a conclusion. The findings of this analysis are included in Section 4 of this paper.

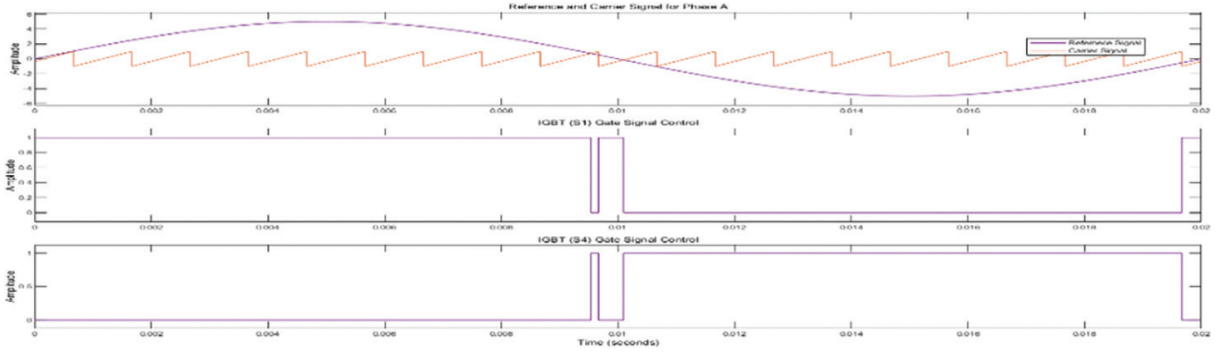

Fig. 9. Pulse generation by the conventional sinusoidal PWM for one leg of the VSI at a cycle.

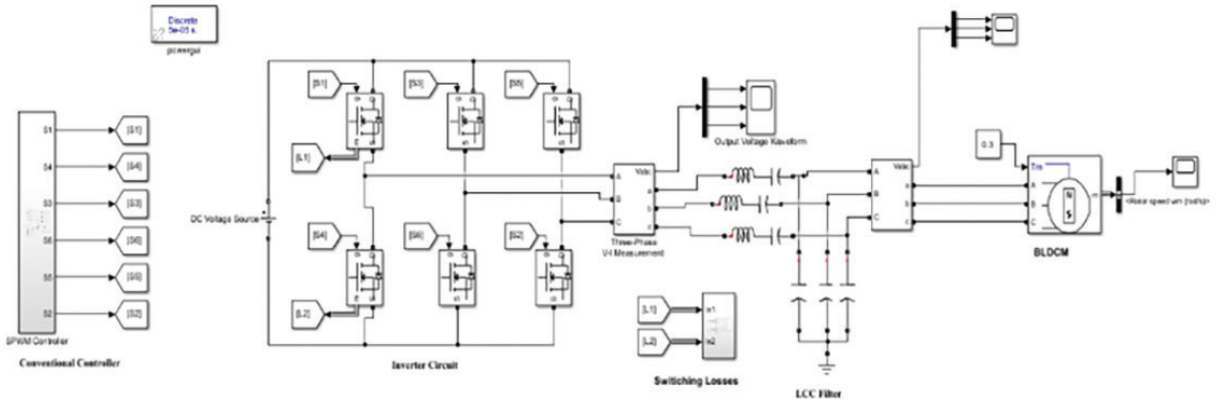

Fig. 10. Conventional VSI-driven system for BLDCM control.

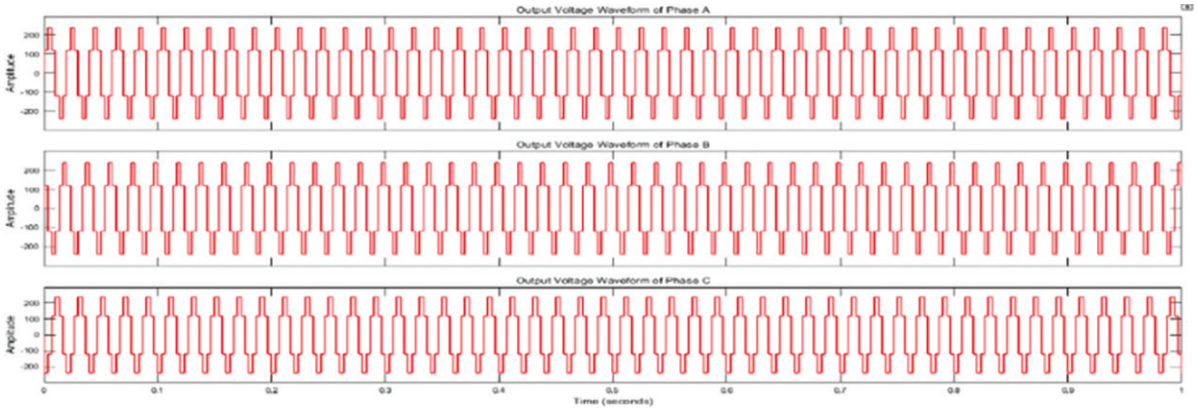

Fig. 11. Output voltage waveform of a conventional VSI-driven system before connecting the LCC filter.

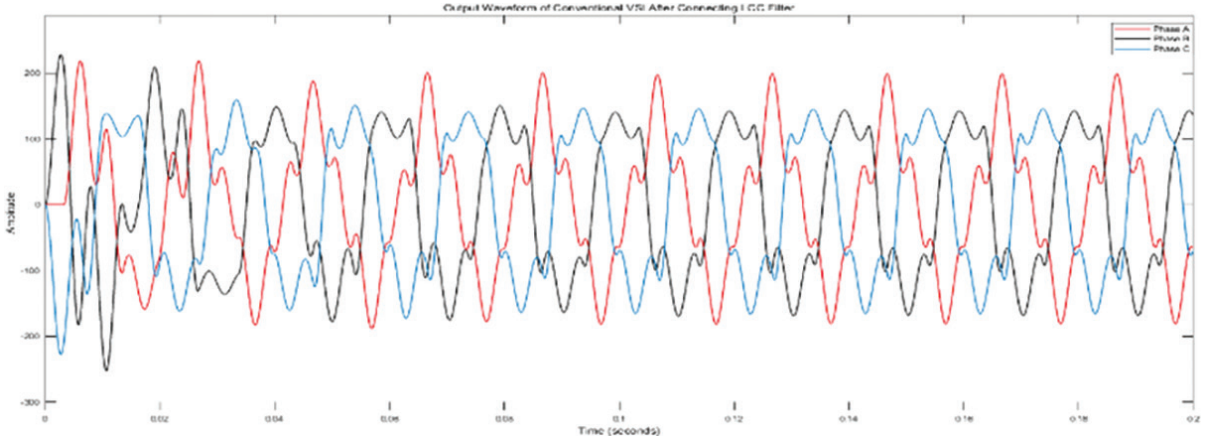

Fig. 12. Output voltage waveform of a conventional VSI-driven system after connecting the LCC filter.

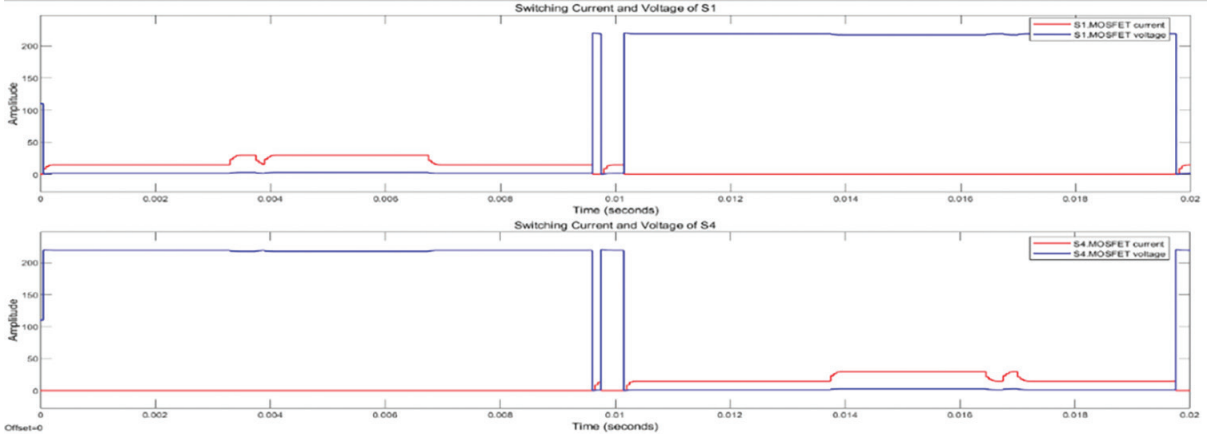

Fig. 13. The switching voltage and current of the MOSFETS located at the first leg of the conventional three-phase VSI circuit.

Parameter	Value	
v_m	220 V	
i_m	29.69 A	
f_s	500 Hz	
	S1 (µs)	S4 (µs)
t_{on}	291.465	97.155
t_{off}	97.155	291.465

Table 3. Parameters for computing the switching losses in the conventional three-phase VSI circuit.

Subsequently, the switching voltage and current of the MOSFETS located at the first leg of the conventional VSI circuit, S1 and S4, were observed for analysis. Figure 13 shows the outcome of the switching voltage and current.

The key parameters observed in the chart depicted in Figure 13 were v_m, i_m, t_{on} and t_{off}. The results of the observation are presented in Table 3.

3.3. Design of proposed sinusoidal PWM controller

The VSI, which was previously managed by the conventional controller, was also subjected to the proposed controller. Figure 14 illustrates the design of the proposed controller.

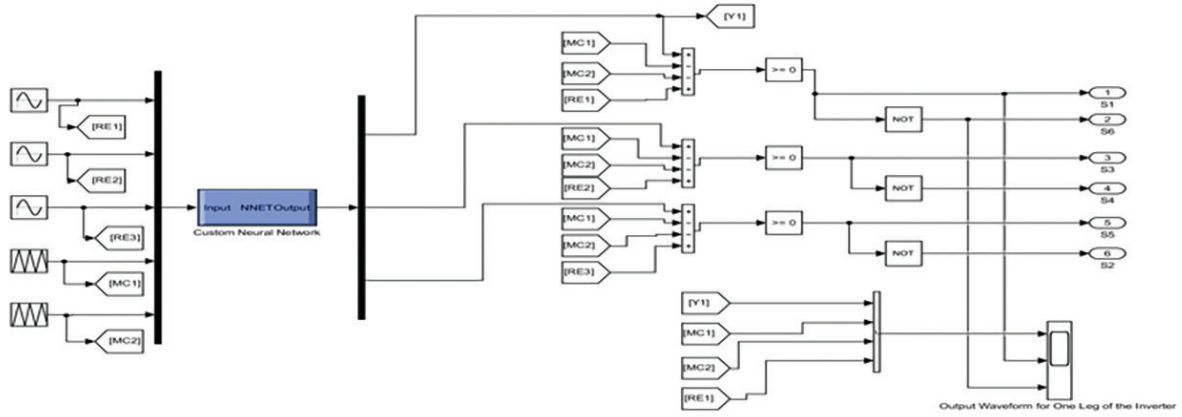

Fig. 14. Design of proposed sinusoidal PWM controller for VSI-driven BLDCM.

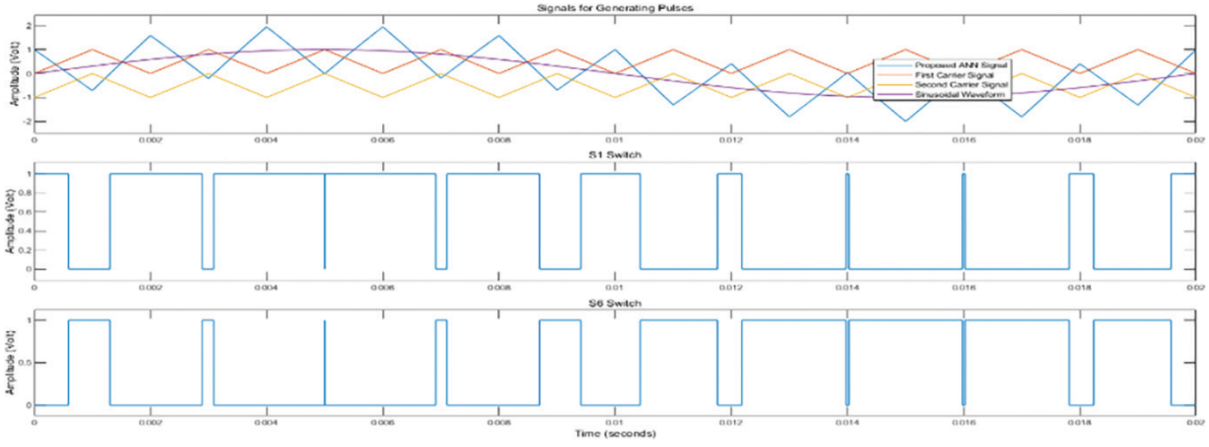

Fig. 15. Pulse generation by the proposed sinusoidal PWM for one leg of the VSI at a cycle.

In Figure 14, the signals utilised for producing pulses underwent initial training via ANN, utilising the theory expounded upon in Sections 2.1 and 2.2. Following this training, the resultant signals were combined with both sinusoidal and triangular signals to generate pulses for the VSI. The controller's output for one leg of the VSI is depicted in Figure15.

A comparison between the proposed and conventional controllers for a single cycle (as depicted in Figures 11 and 15, respectively) reveals that the proposed controller generates more asymmetric pulses. This, in turn, leads to a decrease in the THD present in the VSI's output voltage waveform. Figure 16 showcases the output voltage, following the control of the VSI's switches with the proposed controller. The harmonic output of the voltage waveform has been expounded upon in Section 4 of this paper.

To further decrease the harmonic content in the VSI output waveform, a connection was established between the BLDCM and the VSI output via an LCC filter. Figure 17 illustrates the operational set-up for a three-phase VSI-driven BLDCM system based on the proposed controller.

Upon establishment of the LCC filter, the output voltage waveform of the VSI was analysed. The resulting output waveforms can be seen in Figure 18.

An analysis of the harmonic content present in Figures 16 and 18 was conducted, alongside an examination of the motor's performance. The conclusions drawn from these observations are documented in Section 4 of this paper.

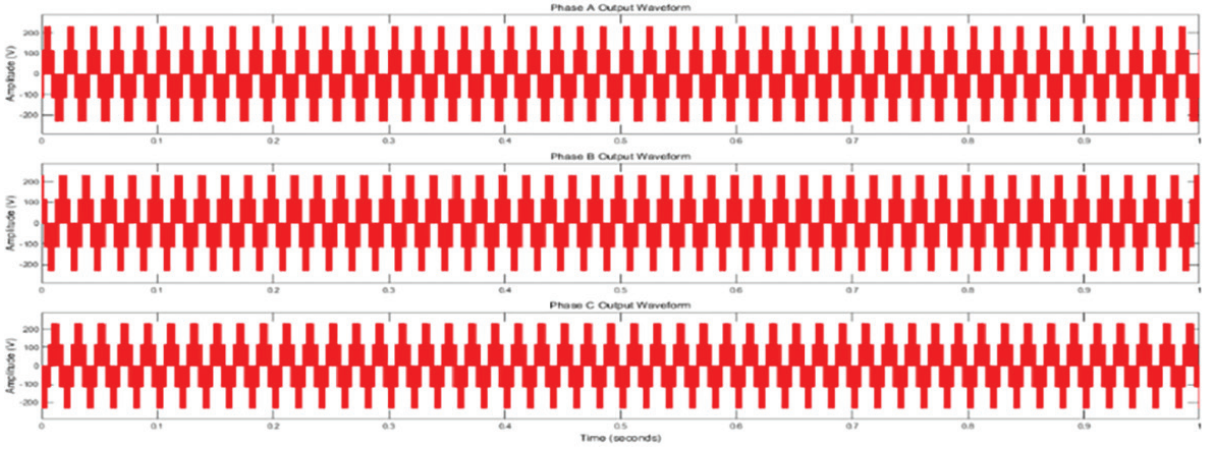

Fig. 16. Output voltage waveform of a VSI controlled by proposed sinusoidal PWM controller before connecting the LCC filter.

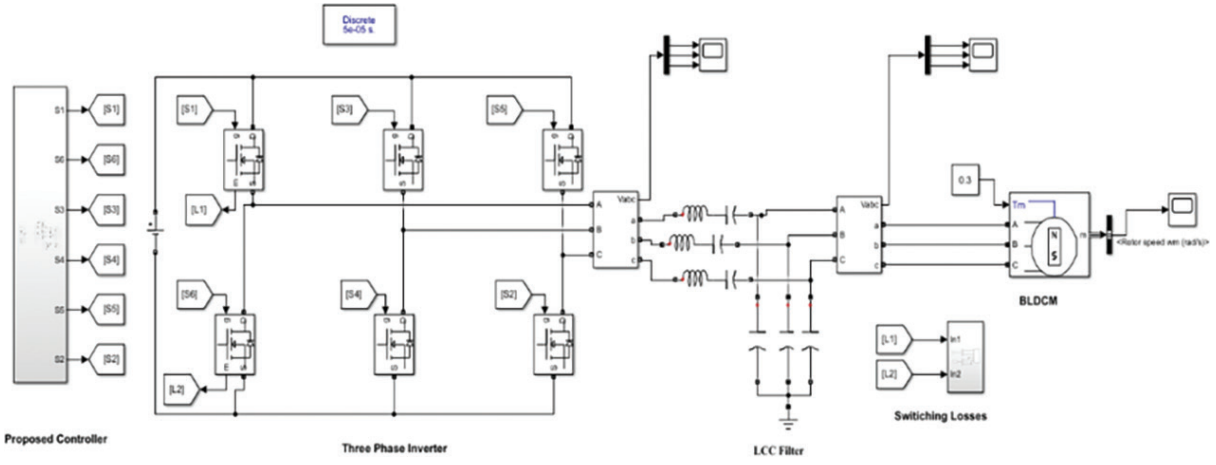

Fig. 17. Proposed VSI-driven system for BLDCM control.

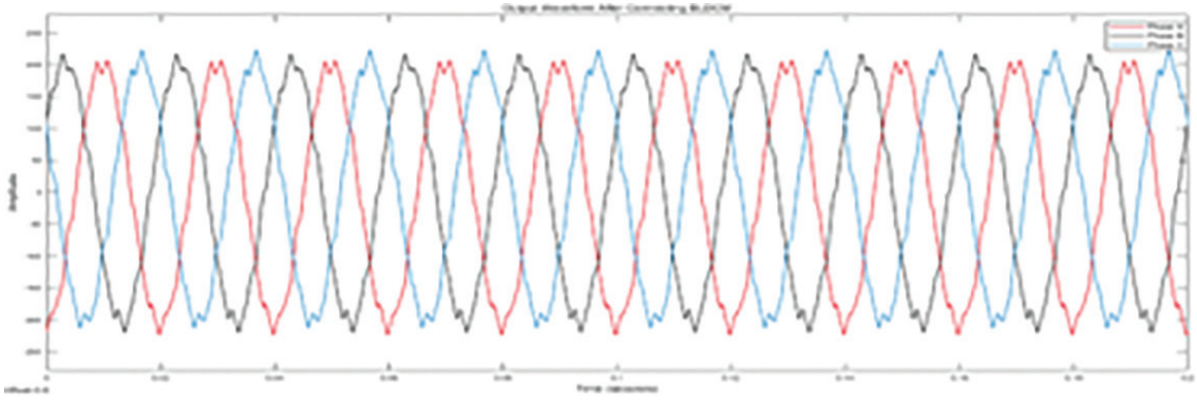

Fig. 18. Output voltage waveform of the proposed ANN based VSI-driven system after connecting the LCC filter.

The switching current and voltage for one leg of the proposed VSI system were subsequently observed for analysis. Figure 19 illustrates the chart displaying the switching voltage and current generated by the S1 and S4 MOSFET switches.

Similarly to the conventional VSI controlled system, the v_m, the i_m, the t_{on} and they t_{off} were recorded and are presented in Table 4.

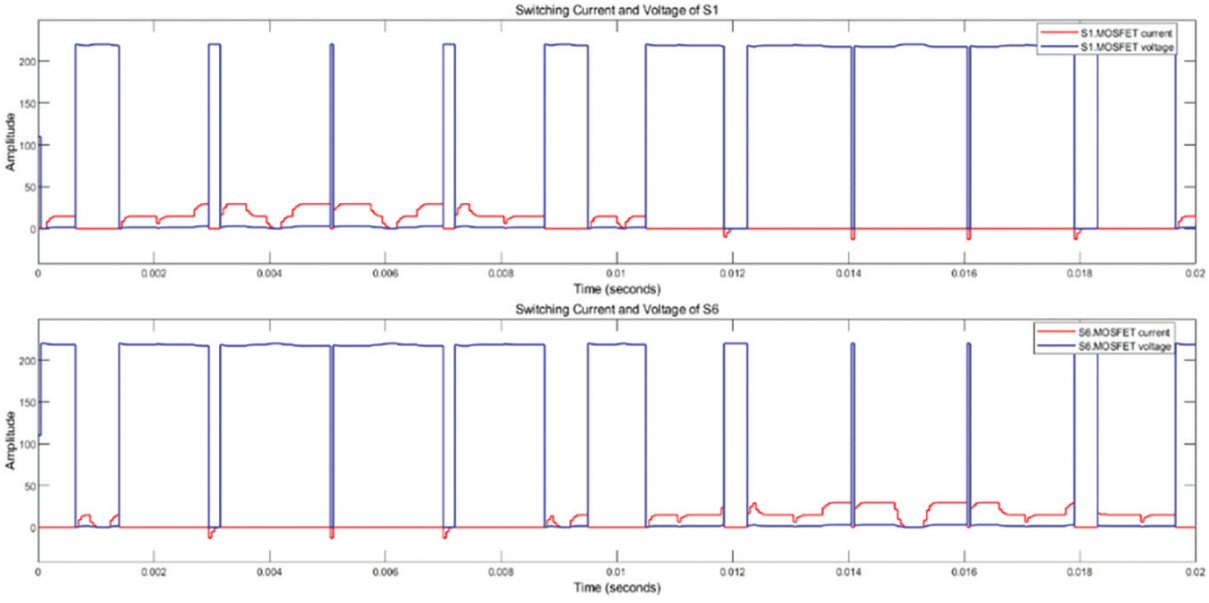

Fig. 19. The switching voltage and current of the MOSFETS located at the first leg of the proposed three-phase VSI circuit.

Parameter	Value	
v_m	220 V	
i_m	29.69 A	
i_m	500 Hz	
	S1 (μs)	S4 (μs)
t_{on}	413.261	238.03
t_{off}	238.03	413.261

Table 4. Parameters for computing the switching losses in the proposed three-phase VSI circuit system.

3.4. Design of NPC VSI-driven BLDCM system

An NPC VSI controller was also designed to compare its output with the proposed system. Figure 20 displays the output of the design.

Referring to Figure 20, it becomes evident that both a sinusoidal and a triangular waveform were employed to generate pulses for controlling the 12 semiconductor switches. Consequently, each leg of the inverter consists of four switches. Figure 21 illustrates the modulating signals and the corresponding pulses for one leg of the NPC VSI system.

The NPC VSI system was utilised to power the BLDCM through the proposed LCC filter, as shown in Figure 22. The output waveform of the proposed system, both before and after implementation of the filter, is illustrated in Figures 23 and 24, respectively.

Considering Figure 23, it is evident that prior to the application of filters, the system generated a seven-level output waveform, which performed better compared with the proposed system. However, after connecting the system to the LCC low pass filter, as shown in Figure 24, it produced a waveform resembling a sine wave with some ripple. The THD content of each output waveform was analysed and presented in Section 4 of this paper.

The v_m, i_m, t_{on} and t_{off} were of the NPC VSI system and are also recorded from Figure 25 and presented in Table 5.

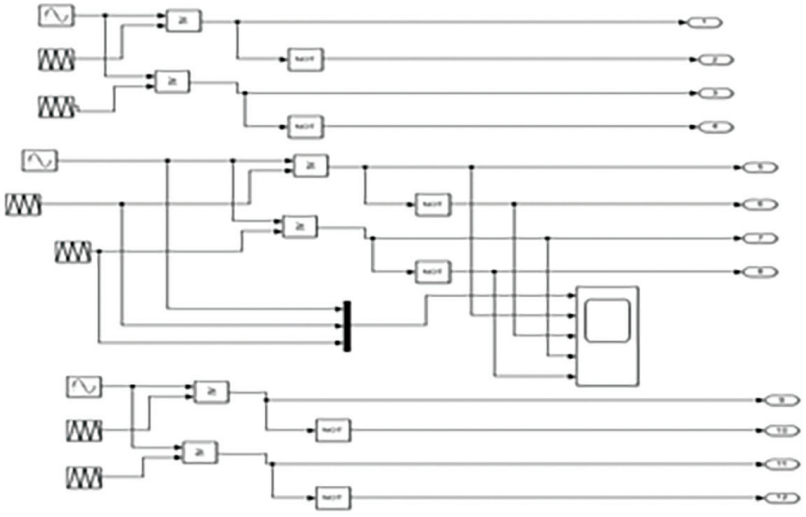

Fig. 20. Design of the NPC VSI sinusoidal PWM based controller.

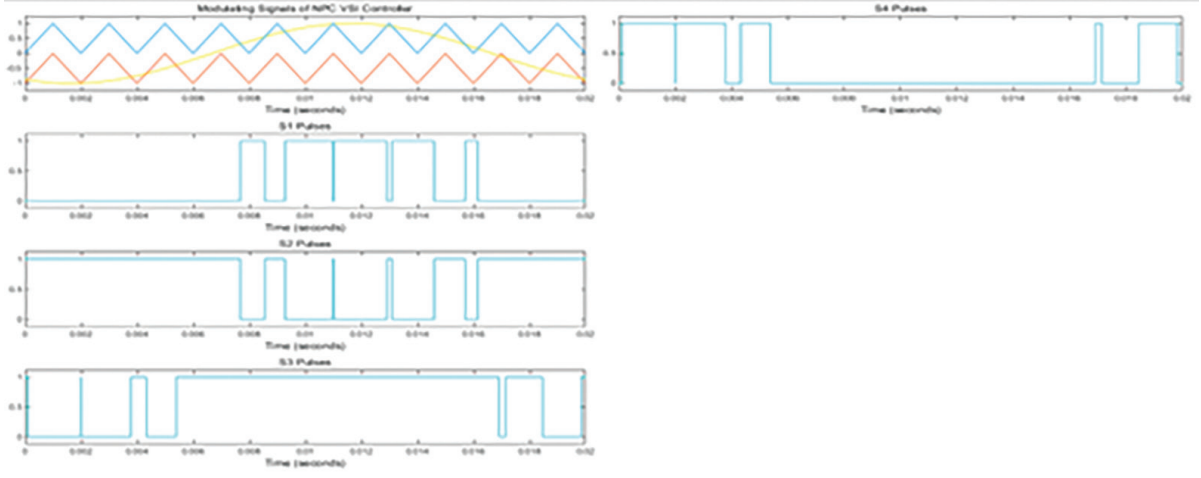

Fig. 21. Pulse generation by the NPC VSI sinusoidal PWM based controller for one leg of the VSI in a cycle.

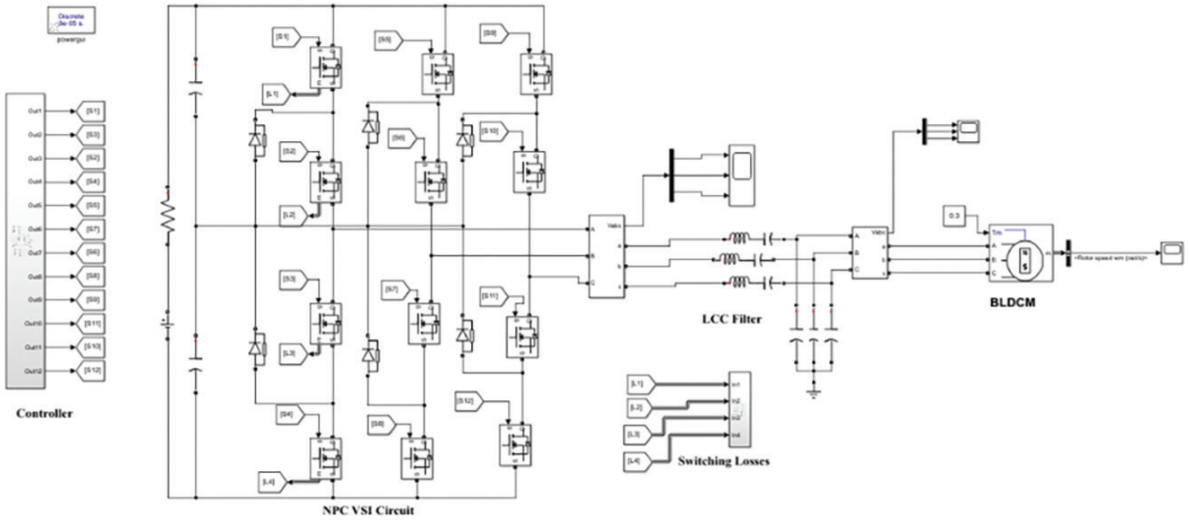

Fig. 22. NPC VSI-driven system for BLDCM control.

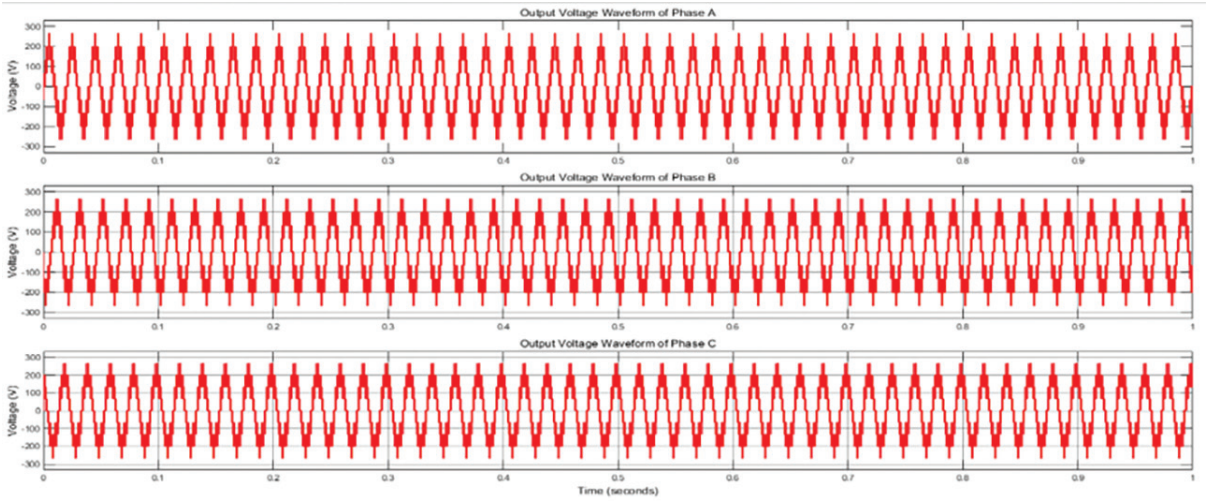

Fig. 23. Output voltage waveform of the NPC VSI system before connecting the LCC filter.

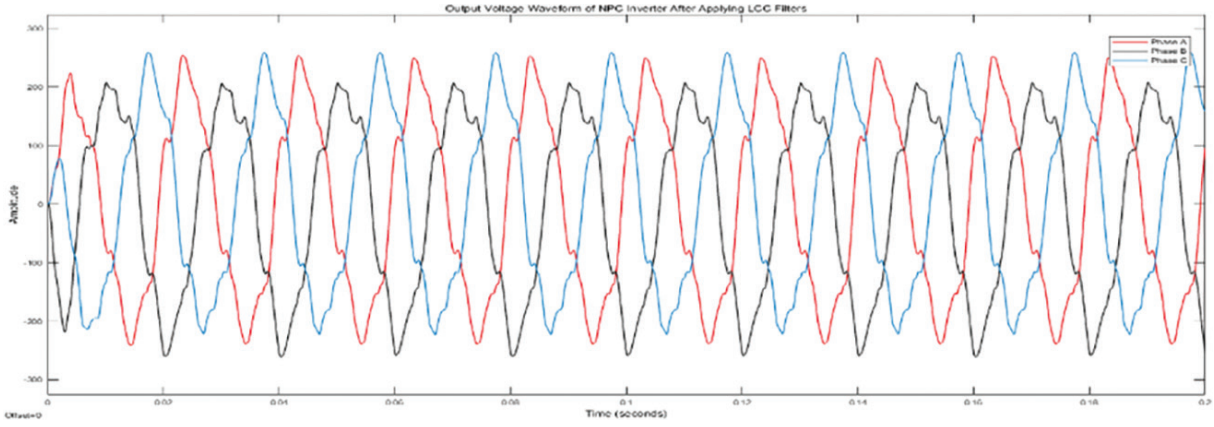

Fig. 24. Output voltage waveform of the NPC VSI system after connecting the LCC filter.

4. Results and Discussion

4.1. Simulation results

The THD in the output voltage waveform of the various systems under discussion was observed under different conditions. One condition involved observing the waveform without the LCC filter, while the other condition involved observing it after connecting the proposed LCC filter.

Figures 26–28 present the THD values of the conventional, proposed and NPC VSI-driven BLDCM systems, respectively, without the influence of the suggested LCC filter.

Figures 29–31 present the THD values of the conventional, proposed and NPC VSI-driven BLDCM systems, respectively, after connecting the suggested LCC filter.

The rotor speed of the BLDCM in the various systems under discussion was also observed under different torque conditions. The torque conditions considered were 0.3 Nm, 0.6 Nm, and 0.9 Nm. Figures 32–34 depict the rotor speed for the conventional, proposed and NPC VSI-driven systems, respectively.

From Figures 32–34, it is apparent that the rotor speed remains constant under all torque conditions. However, it is noticeable that the rotor speed initially started at 8.716 rad/s in the conventional VSI-driven system and

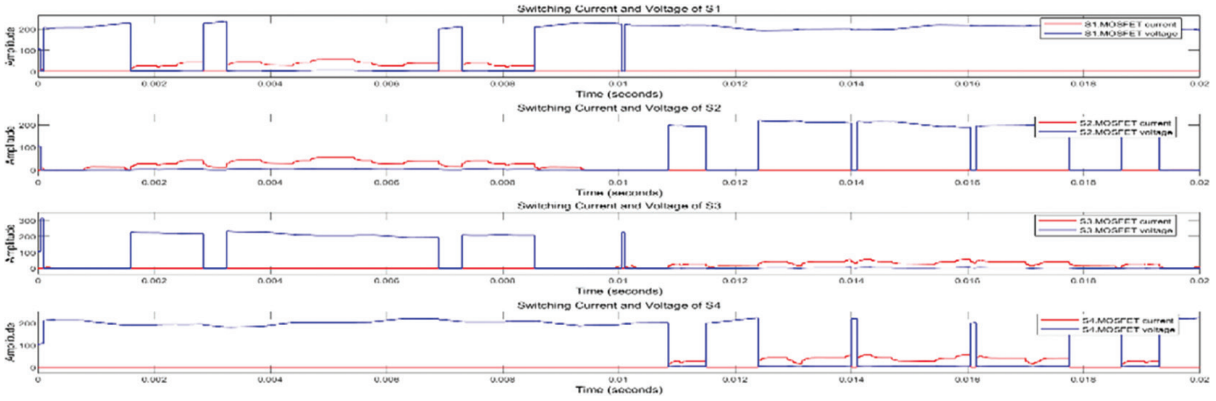

Fig. 25. The switching voltage and current of the MOSFETS located at the first leg of the NPC VSI circuit.

Parameter	Value			
v_m	220 V			
i_m	29.69 A			
f_s	500 Hz			
	S1 (μs)	S2 (μs)	S3 (μs)	S4 (μs)
t_{on}	212.575	219.703	141.744	141.744
t_{off}	141.744	141.744	212.575	219.703

Table 5. Parameters for computing the switching losses in the NPC VSI circuit system.

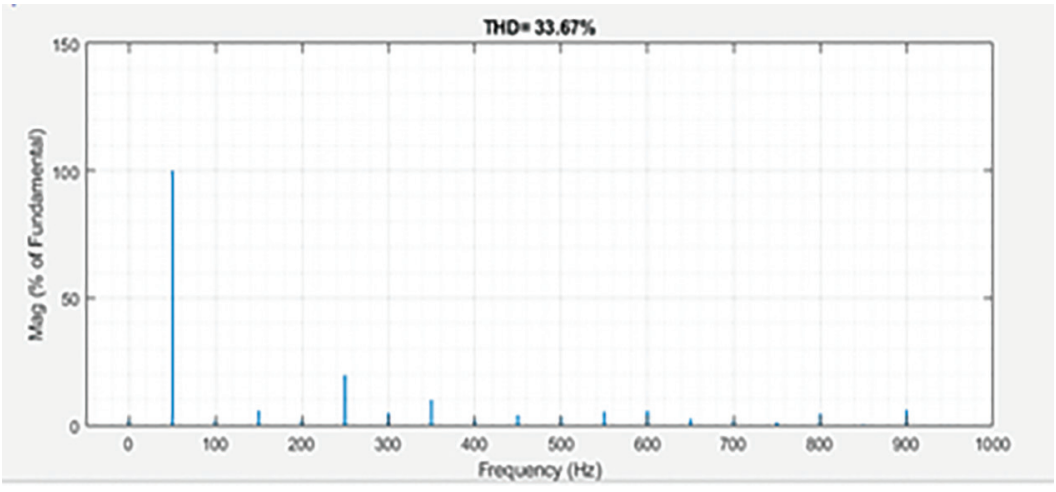

Fig. 26. THD content of VSI's voltage output waveform under conventional sinusoidal PWM controller without LCC filter.

reached the range of −1 to 1 rad/s after 0.376 s. In the proposed ANN-based VSI-driven system, the rotor speed began at 5.383 rad/s and took 0.7 s to reach the range of −1 to 1 rad/s. Lastly, when the BLDCM was connected to the NPC VSI-driven system, the rotor speed commenced at 7.590 rad/s and took 1.1 s to fall within the range of −1 to 1 rad/s.

The performance of the motor was then analysed at variable speed, 0 rad/s, 60 rad/s and 100 rad/s, under the same torque conditions. Figures 35–37 display the variation of the speed for the various system under consideration.

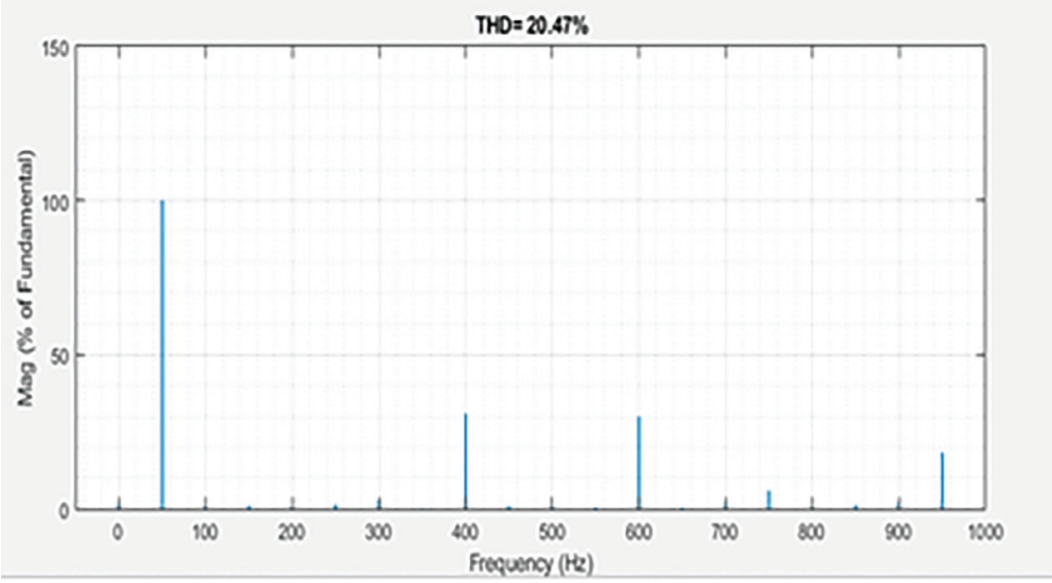

Fig. 27. THD content of VSI's voltage output waveform under proposed sinusoidal PWM controller without LCC filter.

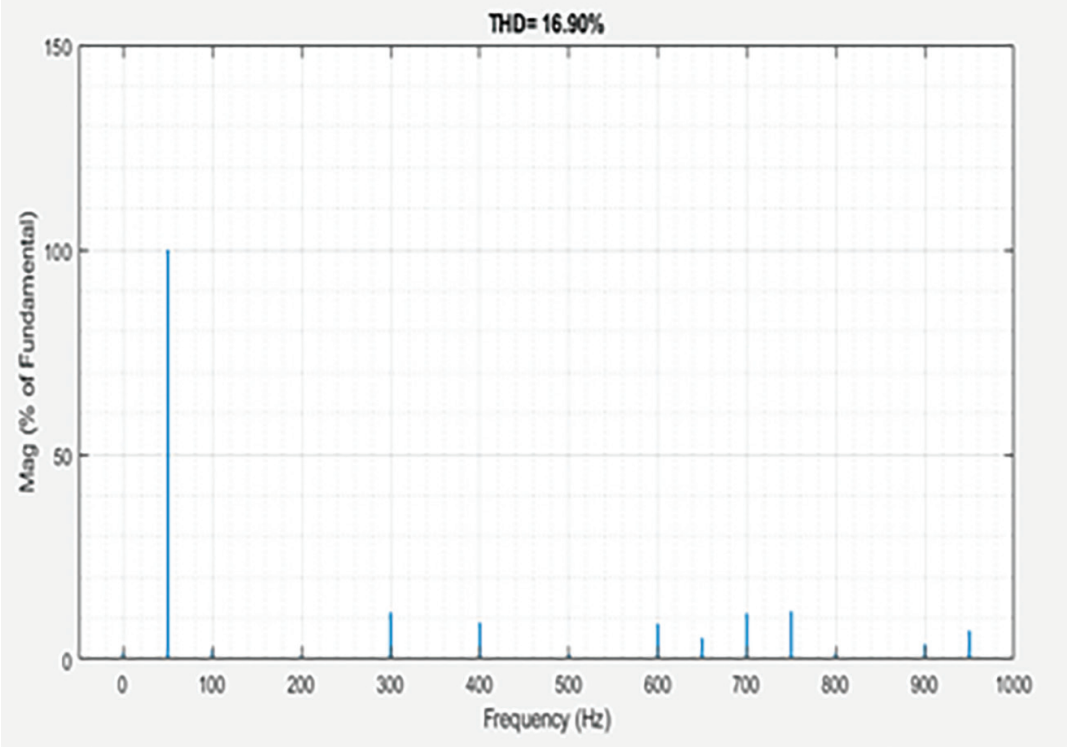

Fig. 28. THD content of VSI's voltage output waveform under NPC sinusoidal PWM controller without LCC filter.

Based on Figures 35–37, one can observe a smooth transition in the speed of the individual systems from the lowest set speed (0 rad/s) to the maximum set speed (100 rad/s) under all three torque conditions.

4.2. Computation of the switching losses of the various system

Below are the computations for the switching losses.

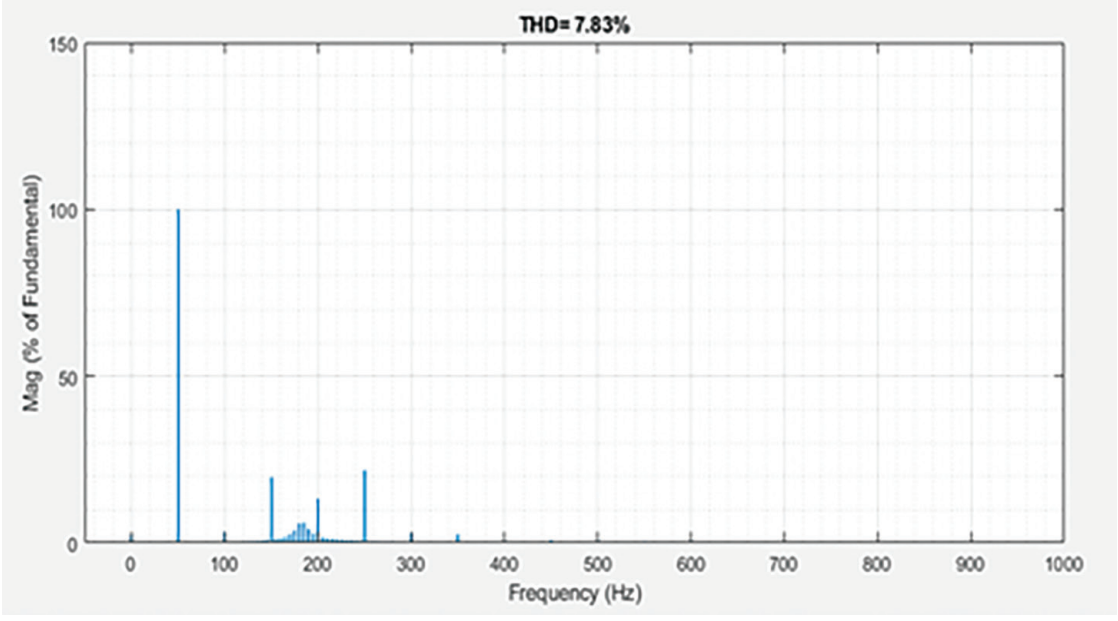

Fig. 29. THD content of the conventional VSI system after connecting the LCC filter.

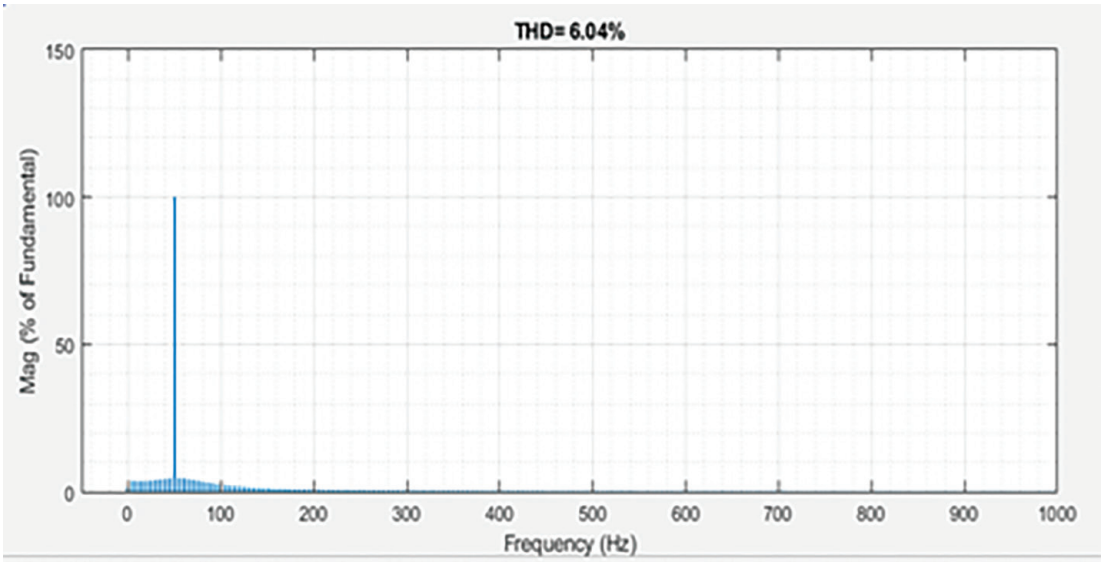

Fig. 30. THD content of the proposed system after connecting the LCC filter.

Switching Losses Computation for Conventional VSI System

The calculation of switching losses was performed utilising Table 3 in Section 3.2 and Eq. (19). The computation of switching losses for the S1 and S2 switches in the traditional system can be determined as follows:

$$P_{S1} = \frac{220 \times 29.69 \times (291.465 + 97.155) \times 10^{-6} \times 500}{2} = 634.6W$$

$$P_{S2} = \frac{220 \times 29.69 \times (97.155 + 291.465) \times 10^{-6} \times 500}{2} = 634.6W$$

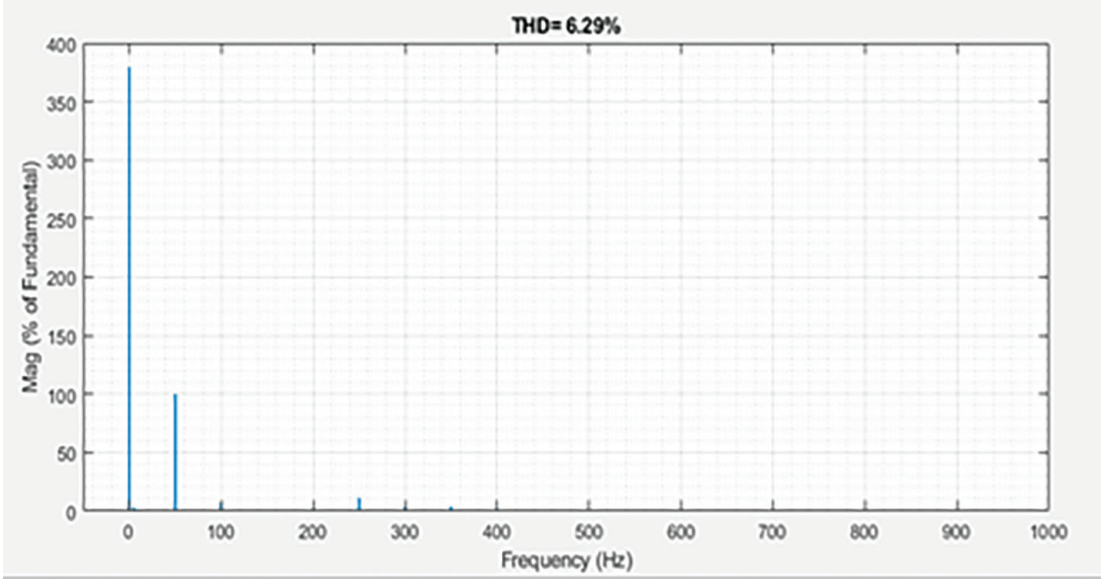

Fig. 31. THD content of the NPC VSI system after connecting the LCC filter.

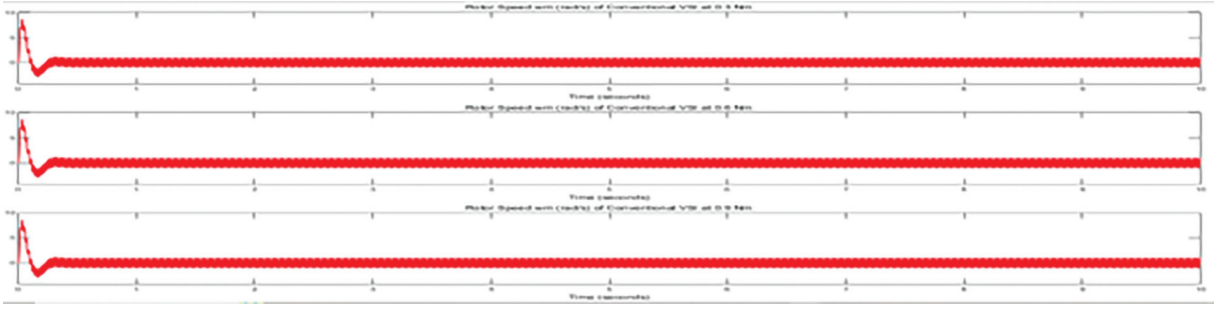

Fig. 32. Performance of the BLDCM connected to the conventional VSI system under 0.3 Nm, 0.6 Nm and 0.9 Nm torque conditions.

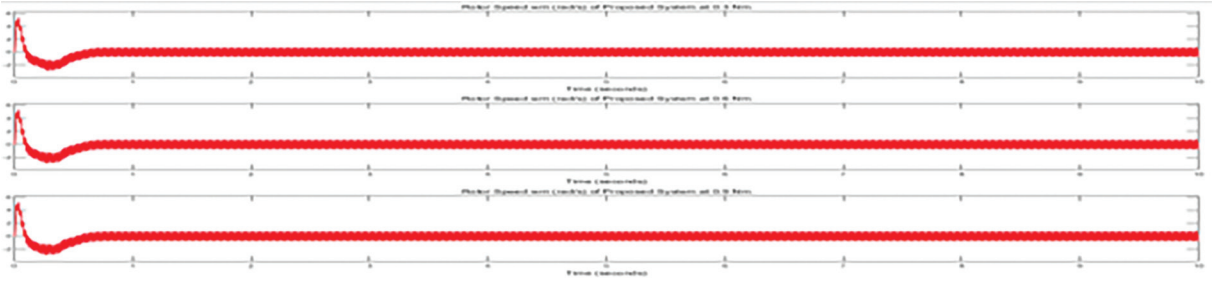

Fig. 33. Performance of the BLDCM connected to the proposed VSI system under 0.3 Nm, 0.6 Nm and 0.9 Nm torque conditions.

Therefore, the calculation of the overall switching losses for one leg of the inverter, denoted as P_{S12}, can be determined as:

$$P_{S12} = P_{S1} + P_{S2} = 634.6 + 634.6 = 1269.2W$$

The total switching losses of the conventional VSI, denoted as P_{SWC}, can be calculated as:

$$P_{SWC} = 3P_{S12} = 3(1269.2) = 3807.6W = 3.8kW$$

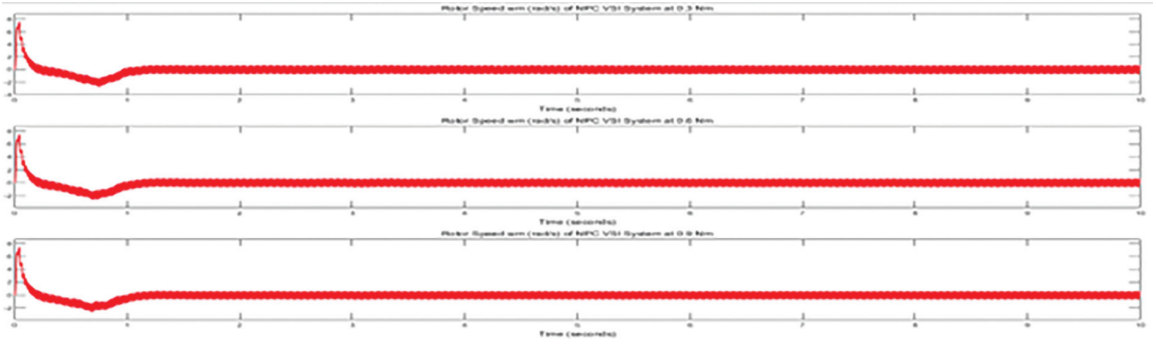

Fig. 34. Performance of the BLDCM Connected to the NPC VSI system under 0.3 Nm, 0.6 Nm and 0.9 Nm torque conditions.

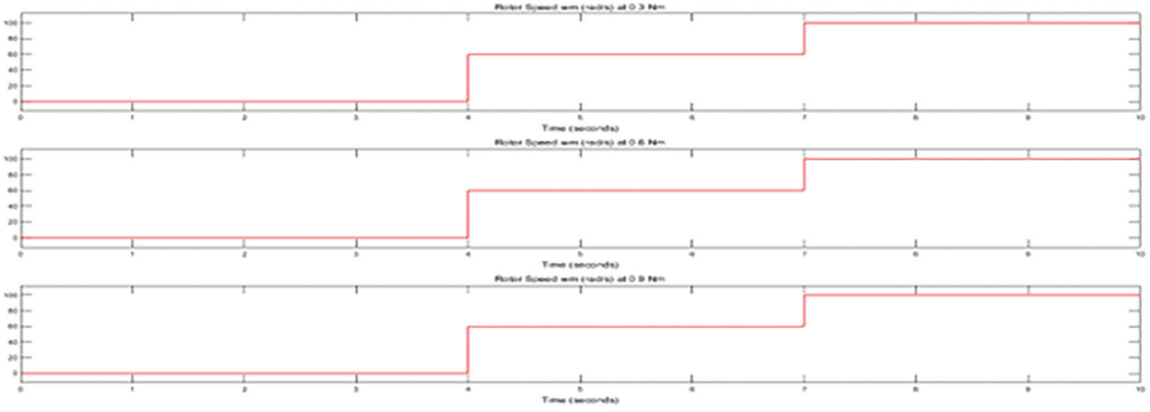

Fig. 35. Variation of the motor speed at 0 rad/s, 60 rad/s and 100 rad/s for conventional drive system.

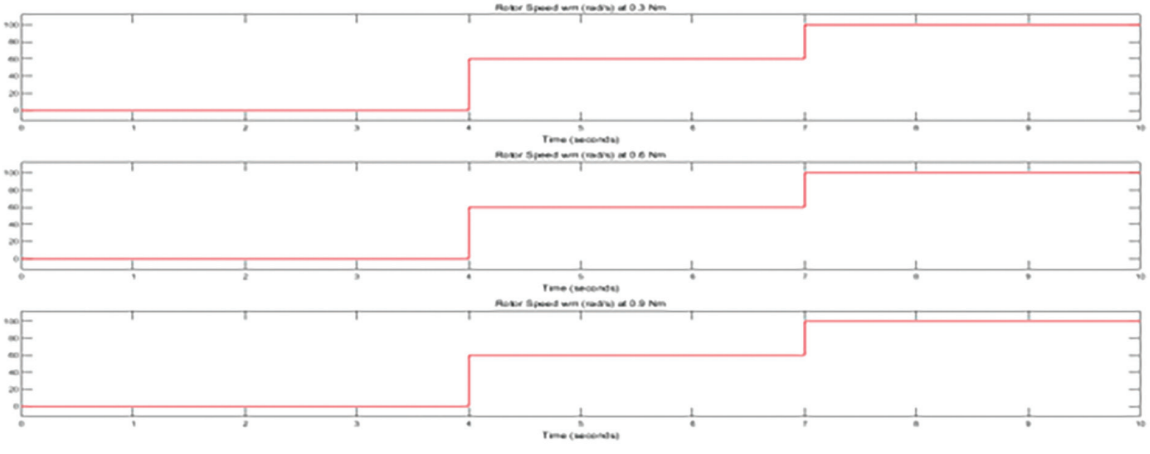

Fig. 36. Variation of the motor speed at 0 rad/s, 60 rad/s and 100 rad/s for proposed drive system.

Switching Losses Computation for the Proposed VSI System

Likewise, the analysis of switching losses for the proposed VSI system can be conducted using Table 4 in Section 3.3 and Eq. (19). Mathematically, the computation of switching losses can be performed as:

$$P_{S1} = \frac{220 \times 29.69 \times (413.261 + 238.03) \times 10^{-6} \times 500}{2} = 1063.53W$$

$$P_{S4} = \frac{220 \times 29.69 \times (238.03 + 413.261) \times 10^{-6} \times 500}{2} = 1063.53W$$

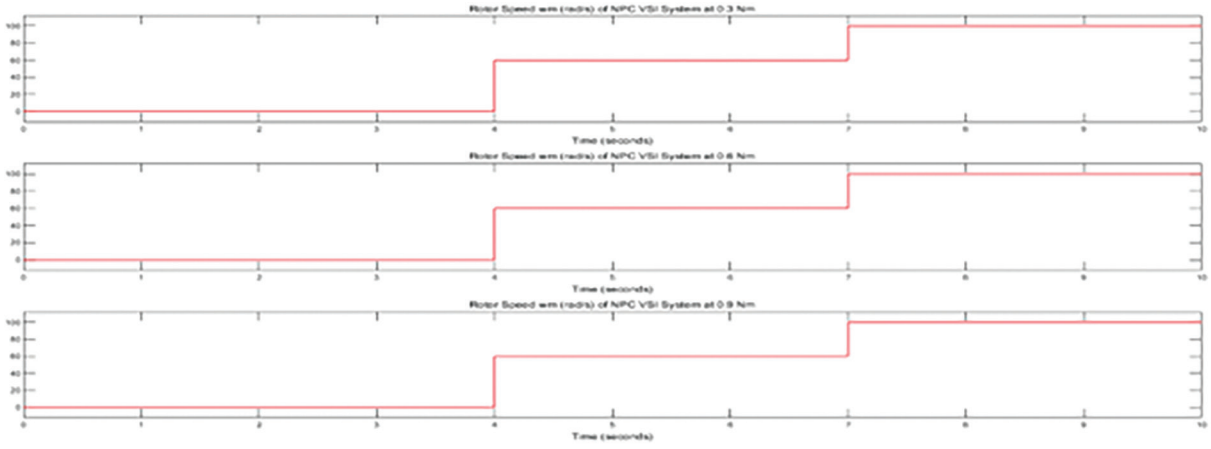

Fig. 37. Variation of the motor speed at 0 rad/s, 60 rad/s and 100 rad/s for NPC-based drive system.

Hence, the calculation of the overall switching losses for one leg of the inverter, labelled as P_{S14}, can be determined as:

$$P_{S14} = P_{S1} + P_{S4} = 1063.53 + 1063.53 = 2127.06W$$

The overall switching losses of the proposed VSI system, represented as P_{SWP}, can be calculated as:

$$P_{SWP} = 3P_{S14} = 3(2127.06) = 6381.18W = 6.4kW$$

Switching Losses Computation for the NPC VSI System

Similarly, the computation of switching losses for the NPC VSI system can be performed using Table 5 in Section 3.4 and Eq. (19). Mathematically, the switching losses can be calculated as:

$$P_{S1} = \frac{220 \times 29.69 \times (212.575 + 141.744) \times 10^{-6} \times 500}{2} = 578.56W$$

$$P_{S2} = \frac{220 \times 29.69 \times (219.703 + 141.744) \times 10^{-6} \times 500}{2} = 590.22W$$

$$P_{S3} = \frac{220 \times 29.69 \times (141.744 + 212.575) \times 10^{-6} \times 500}{2} = 578.56W$$

$$P_{S4} = \frac{220 \times 29.69 \times (41.744 + 219.703) \times 10^{-6} \times 500}{2} = 590.22W$$

Therefore, the calculation of the overall switching losses for one leg of the NPC VSI circuit, designated as P_{S1234}, can be determined as:

$$P_{S1234} = P_{S1} + P_{S2} + P_{S3} + P_{S4} = 578.56 + 590.22 + 578.56 + 590.22 = 2337.56W$$

The total switching losses for the NPC VSI system, denoted as P_{SWN}, can be calculated as:

$$P_{SWN} = 3P_{S14} = 3(2337.56) = 7012.68W = 7.0kW$$

Type of system	THD value (%) before connecting the LCC filter	THD value (%) after connecting the LCC filter
Conventional VSI-driven BLDCM system	33.67	7.83
Proposed VSI-driven BLDCM system	20.47	6.04
NPC VSI-driven BLDCM system	16.90	6.29

Table 6. Summary of THD results.

Type of system	Total switching losses (kW)
Conventional VSI-driven BLDCM system	3.8
Proposed VSI-driven BLDCM system	6.4
NPC VSI-driven BLDCM system	7.0

Table 7. Summary of total switching losses.

4.3. Discussion of result

The summary of the THD content of the output voltage waveform of the VSI under all conditions is displayed in Table 6.

In addition, result of the total switching losses for all three systems under discussion is presented in Table 7.

Based on the information presented in Tables 6 and 7, it can be deduced that the LCC filter exhibits superior performance in the proposed ANN-based VSI-driven BLDCM system compared with the other systems being examined. Furthermore, its capability to handle switching losses falls between that of the conventional VSI-driven BLDCM and NPC VSI-driven systems. Therefore, the trend of increasing the number of switches in a VSI circuit to enhance its output waveform should be re-evaluated. This would aid in achieving a balance between system performance in terms of switching losses and the harmonic content of the output waveform.

Moreover, upon reviewing Figures 31–33, it becomes evident that the proposed system has the lowest initial speed in comparison to the conventional and NPC VSI-driven BLDCM systems.

5. Conclusion

This paper discusses a new controller for a BLDCM. The proposed technique modifies the common sinusoidal PWM controller used in inverter switch control. This modification involves training the sinusoidal and triangular wave signals to generate a new signal, which is combined with the reference wave and two triangular waves to produce pulses at the switching terminals of the controller. The proposed system, along with the conventional and NPC VSI circuits utilising 6 and 12 switches, respectively, was designed with MATLAB/Simulink. Subsequently, the three systems were examined and compared after being connected to a BLDCM via an LCC filter. The results revealed that while the NPC VSI system demonstrated superior performance in minimising THD in the output waveform, the proposed system achieved the lowest THD value (6.04%) after the connection of the LCC filter. Furthermore, due to the retention of six switches during the design of the proposed system, which are known for having the lowest switching losses, a reduction of 0.6 kW in overall switching losses was achieved with the proposed system compared with the NPC VSI-based system. During the examination of rotor speed at 0 rad/s, it was observed that the initial speed rose to 5.383 rad/s. However, in the case of the conventional and NPC VSI-based systems, the increase in starting speed surpassed 5.383 rad/s at 0 rad/s. The speed of the various system was also varied under three speed conditions, 0 rad/s, 60 rad/s and 100 rad/s. Results from the variation indicated that all the systems have the ability to control the speed of the BLDCM under different speed condition.

Based on the presented results, it can be concluded that the utilisation of additional switches leads to increased switching losses in a VSI-driven system. Therefore, it is recommended to maintain the minimum number of switches while minimising the output waveform of the VSI-driven system. This approach helps optimise the system by simultaneously reducing both switching losses and the THD value in the output voltage waveform.

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