

A METHOD OF REDUCING SWITCH COUNT IN THREE-LEVEL NPC INVERTER – ANALYSIS IN STEADY STATES

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Abstract: The proof of a concept for a new method of modulation has been presented which reduce switch count in a three-level neutral point clamped (3L-NPC) inverter. The method is an implementation of space vector modulation (SVM) by means of a prediction algorithm and sequences of transistors, which are not common in use. Those sequences make active use of clamping diodes of the inverter. The prediction algorithm analyzes possible sequences of transistors' states and choose those which offers smaller switch count. Measurements of steady states were taken on prototype 3L-NPC.

Keywords: *reduction of switch count, three-level NPC inverter, space vector modulation*

1. INTRODUCTION

The neutral-point-clamped PWM inverter was originally developed by Nabae, Takahashi and Akagi in 1981 [1]. Main advantages of this configuration over two level topologies are better efficiency, less harmonic distortion due to more voltage levels and half of voltage rating of switching devices requirement [1–3]. Lower voltage changes between levels reduces stress on the motor wiring. Additionally, lower voltage transistors may work faster, which allows usage of higher switching frequency. Increased voltage levels and higher switching frequency decrease inverter output harmonics [4]. Main disadvantages of NPC configuration compared with two-level inverters are more complex topology with more power switches, more clamping diodes and difficulty to do real power flow control for the individual inverter [5].

The paper presents a proof of concept for reduction of the number of individual state changes in power transistors (switch count) with modified space vector modulation (SVM) method in a three-level neutral point clamped (3L-NPC) inverter. The method is presented in detail in [6]. It is realized by utilizing a prediction algorithm and sequences of transistors which are not common in use. Those sequences make active use

of clamping diodes of the inverter. The prediction algorithm analyzes possible sequences of transistors' states and chooses those which offer smaller switch count. Finding ways to make switch count as low as possible is necessary to avoid switching losses.

The method of modulation was tested on a prototype 3L-NPC converter made especially for testing novel modulation methods. Designing of industrial converter using the modulation method presented in this paper needs further research.

3L-NPC converter used for the tests is described in section 2. The SVM modulation and prediction algorithm are presented in section 3. Section 4 contains tests results of the converter work in steady states. Section 5 is the conclusion.

2. DESCRIPTION OF THE PROTOTYPE CONVERTER

A working prototype converter was made at the Institute of Drive Systems and Robotics, Opole University of Technology for testing of a new concept of modulation for 3L-NPC inverters. The converter allows easy access to measure points of its circuit. The converter is shown in Fig. 1 and its main circuit is shown in Fig. 2.

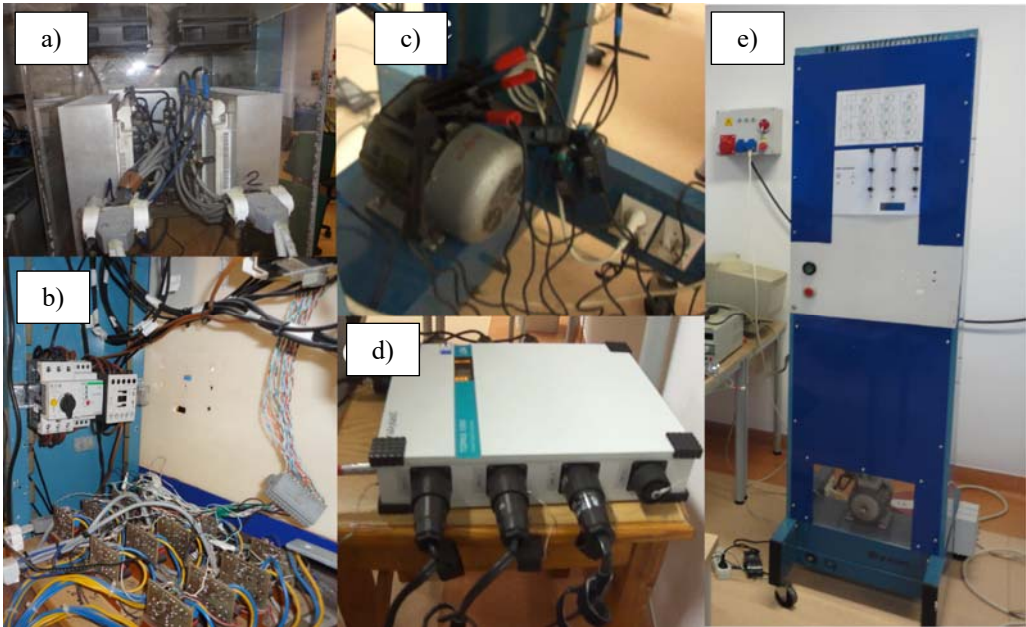


Fig. 1. A prototype converter: a) IGBT modules with heatsinks, b) twelve IGBT driver modules, c) Elektrim Sa71-4A induction motor with power analyzer connections, d) power quality analyzer TOPAS 1000, e) front side of the converter with an induction motor at the bottom, at the top are LED indicators for every power transistor

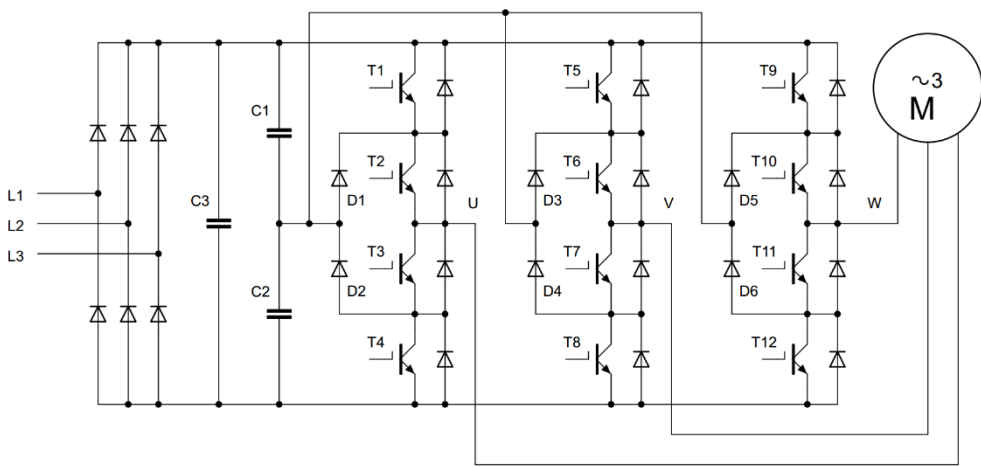


Fig. 2. Main circuit of the converter

2.1. MAIN COMPONENTS

- Insulated gate bipolar transistors (IGBT) are used as inverter power switches (T1–T12 in Fig. 1). Transistors are in two FS150R12KE3G modules made by Infineon. Each module contains six IGBT transistors ($V_{CE} = 1200$ V, $I_{Cnom} = 150$ A) and six clamping diodes ($V_{RRM} = 1200$ V, $I_F = 150$ A).
- Six-pulse rectifier module VUO34-18NO1 made by Ixys ($V_{RRM} = 1800$ V, $I_{DAV} = 45$ A, $I_{FSM} = 300$ A).
- Four electrolytic filter capacitors ($C = 950$ μ F, $V = 400$ V) made by Epcos, shown in Fig. 1 as C1 and C2 (each one is made of two capacitors in series).

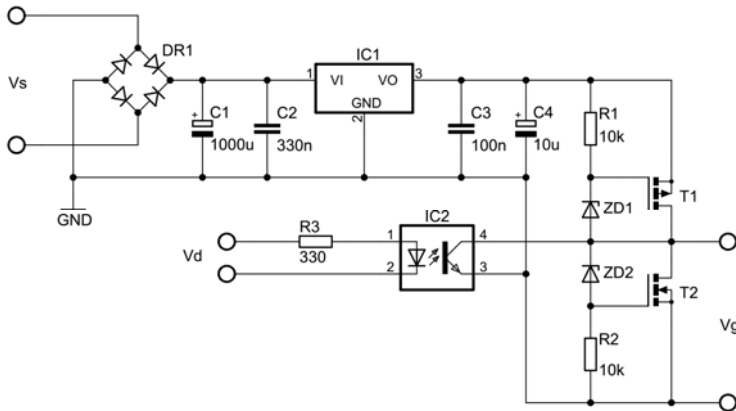


Fig. 3. IGBT gate driver module circuit: V_s – supply input, V_d – driving signal input from the microcontroller, V_g – driving output to the transistor gate

- Twelve modules with opto-isolators as IGBT gate drivers. A circuit of one such a module is shown in Fig. 3. Each module is powered from a separate transformer winding. PC817A photocouplers are used with 5 kV isolation voltage between the input and output. The modules provide isolation between microcontroller outputs and power transistors gates.
- Three-phase induction motor Elektrim Sa71-4 A, 380 V, 50 Hz, 0.84 A (wye connection), 0.68 power factor.

2.2. CONVERTER PROTECTION

Several devices are used for the protection of the converter circuit (a block diagram of the protection devices is shown in Fig. 4):

- Three circuit breakers S161 L25A for over-current protection, rated 25 A.
- Contactor I used as a converter ON/OFF switch.
- Motor protector PKZM0-1 made by Eaton. This protector have thermal over-current protection adjustable in the range of 0.67–1 A, and a short-circuit magnetic protection rated at 14 A. The protector can disconnect surge currents up to 150 kA at 400 V.
- Phase loss monitor CZF-BR made by F&F disconnecting contactor II in the case of phase loss.
- Custom protection module for filter capacitors disconnecting contactor III in the case of overvoltage.
- Metal-oxide varistors (MOV) TMOV20-821 with over temperature cut-off function to protect excessive voltage surges.

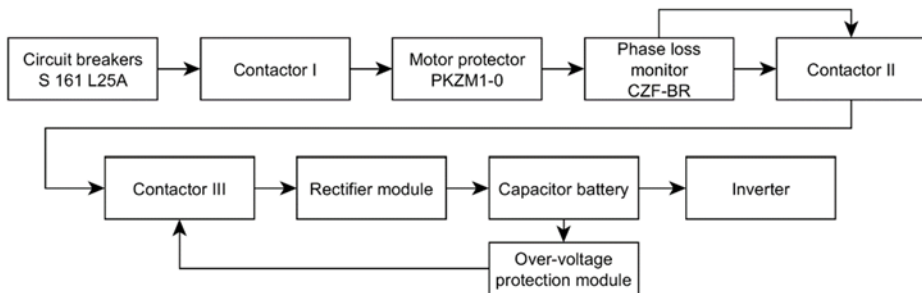


Fig. 4. Block diagram of protection devices.

3. MODULATION METHOD

For the test, a modified space vector modulation (SVM) method was used [6]. The modulation rotating magnetic field is represented as U_0 vector rotating in a complex

plane. Control algorithm is used to calculate the U_0 coordinates according to desired parameters of the inverter in a sample of time.

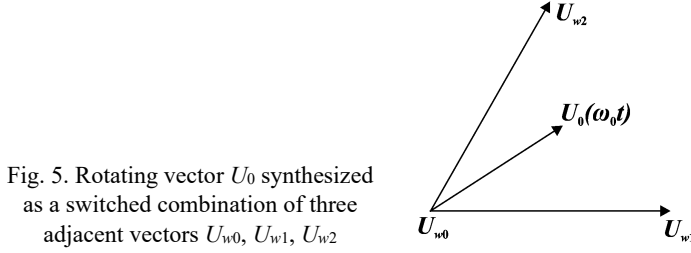


Fig. 5. Rotating vector U_0 synthesized as a switched combination of three adjacent vectors U_{w0} , U_{w1} , U_{w2}

A three-level inverter can give nineteen combinations of voltage values between phases (u_{AB} , u_{BC} , u_{CA}) at its output. Those combinations are represented in a form of nineteen switching vectors. Those vectors form a regular hexagon in the complex plane. If sampling time T_C is constant and sufficiently small, the U_0 vector is considered constant in that time. In a two-level inverter, the U_0 is synthesized as a weighted average combination of the adjacent switching voltage vectors (Fig. 5). There are six non-zero voltage vectors (U_{w1} – U_{w6}) and one zero voltage vector (U_{w0}) in a two-level inverter which divide the complex plane into six sectors that make up the two-level hexagon. The switching time (t_0 , t_1 , t_2) of each vector is calculated from $i = 1$ –6 according to Eqs. (1) and (2), where i stands for the sector number in which U_0 vector is currently located. If $i + 1 = 7$, then we assume that $i = 1$, because when U_0 vector is in the sixth sector then it is synthesized from the sixth and first non-zero voltage vectors (U_{w6} and U_{w1}). Calculated times (t_0 , t_1 , t_2) are used to modulate switching vectors in a sequence: $t_0/4$, $t_1/2$, $t_2/2$, $t_0/2$, $t_2/2$, $t_1/2$, $t_0/4$ or $t_0/4$, $t_2/2$, $t_1/2$, $t_0/2$, $t_1/2$, $t_2/2$, $t_0/4$, where t_0 is for zero vectors, and t_1 , t_2 for non zero vectors.

$$\frac{T_C}{2} U_0 (\omega_0 t) = t_1 U_{wi} + t_2 U_{wi+1} \tag{1}$$

$$t_0 = T_C - t_1 - t_2 \tag{2}$$

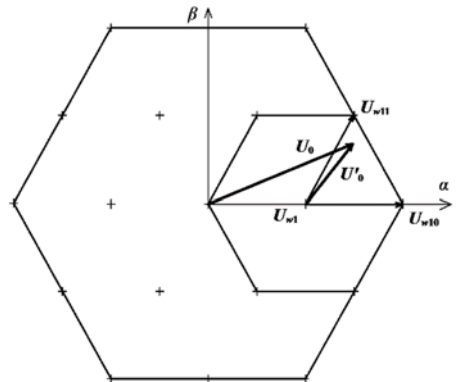


Fig. 6. Transposition of U_0 coordinates from the main hexagon to U'_0 coordinates in a local two-level hexagon. U'_0 is synthesized as a switched combination of three adjacent vectors U_{w1} , U_{w10} , U_{w11}

For a three-level inverter, the method of coordinates transposition is used [7]. It allows the use of the same calculation of switching times as in a two-level inverter. Depending on the θ angle, U_0 coordinates are transposed to U'_0 in one of six smaller hexagons (Fig. 6), which is treated locally in the analogous way as it is in the two-level inverter. The modified SVM algorithm uses 6 look-up tables with switching vectors sequences transposed for 6 outer two-level hexagons and one table without transposition for the inner hexagon.

Each of the nineteen switching vectors of three-level inverter can be obtained by one to four different combinations of twelve transistors' states. For example, a zero voltage vector U_{w0} can be obtained from three possible sets of transistors' states (T_1-T_{12}) 110011001100, 011001100110, 001100110011, where 0 denotes OFF, and 1 denotes ON state. This paper presents an approach in which additional combinations of transistors' states are used. Those combinations make active use of clamping diodes of the inverter.

A prediction algorithm is used in order to make full use of the additional sets and to calculate a sequence of possible sets of transistors' states in a way that offers a smaller switch count. This algorithm calculates switching sequence for two steps ahead. The considered set of transistors' states is compared with the previous one by a XOR logical operation (Fig. 7).

$$\begin{array}{r} \begin{bmatrix} 1100 & 0011 & 1100 \\ 1100 & 0011 & 0100 \\ 1100 & 0011 & 0110 \end{bmatrix} \\ \text{XOR} \\ \begin{bmatrix} 1100 & 0011 & 1100 \\ 1100 & 0011 & 0100 \\ 1100 & 0011 & 0110 \end{bmatrix} \\ \hline \begin{bmatrix} 0000 & 0000 & 1000 \\ 0000 & 0000 & 1010 \end{bmatrix} \end{array}$$

Fig. 7. In this example, the most optimal set after 110000111100 is 110000110100, because only one transistor changes its state

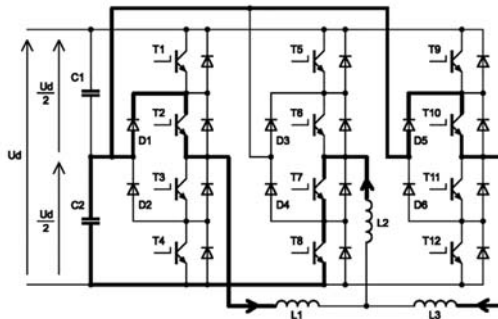


Fig. 8. One of the additional sets of transistors' states that do not require measurement of the inverter output current flow

The tests described in the paper consist only of those sets of transistors' states which did not require measurement of the inverter output current flow (Fig. 8). Further research will require a more advanced circuit to accurately measure the inverter output

current flow at a given time. Then it will be possible to make use of all additional sets of transistors' states, and therefore further improve the efficiency of the prediction algorithm.

The modified SVM algorithm was used at this given parameters:

- voltage frequency $f = 50$ Hz and 33.33 Hz,
- sampling time $T_C = 0.5$ ms,
- temporal resolution $t_r = 10$ μ s,
- transistor dead time $t_d = 20$ μ s.

Time after state change on microcontroller output to voltage change on motor windings is from 2 to 5 μ s. This time was measured at line to line voltage change from 0 V or 11 V to 22 V. If the longest time of the voltage change is equal to 5 μ s, then secure value of transistor's dead time should be 10 μ s. Because of temporal resolution of used microcontroller, the dead time was finally set at 20 μ s.

4. ANALYSIS OF STEADY STATES

The main goal of this measurements was to compare waveforms of voltage and current levels at the output of the inverter for the same voltages, frequencies and voltage vectors PWM sequence, but with different sets of transistors' states. The measurements were taken for several steady states of the converter, from which two were chosen. The first at the voltage frequency $f = 50$ Hz and full modulation index which is equal to one, and the second at $f = 33.33$ Hz and 0.66 modulation index. Both, standard and additional sets of transistors' states were tested.

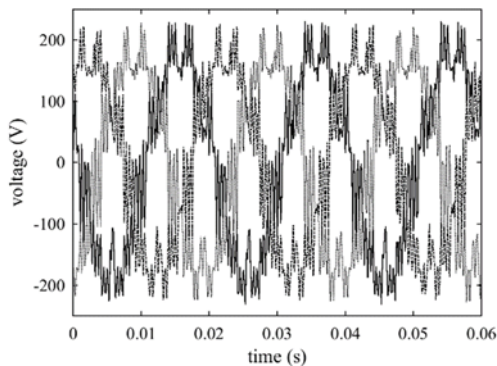


Fig. 9. Line to neutral voltage waveforms for three phases of the induction motor for $f = 50$ Hz for standard conducting states of transistors

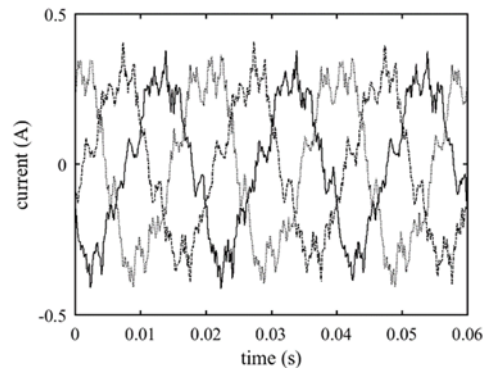


Fig. 10. Current waveforms for three phases of the induction motor for $f = 50$ Hz for standard conducting states of transistors

The measurements were made using the power quality analyzer TOPAS 1000 made by LEM NORMA GmbH. Time interval between sampling for the analyzer is set at

156 μs . The analyzer calculates harmonic spectrum of the voltages and current. Results presented in Figs. 9–16 consist of three independent waveforms shown in every figure. This waveforms depict voltage and current levels for three phases L1, L2, L3 at the output of the inverter and are marked with solid, dashed and dotted lines, respectively.

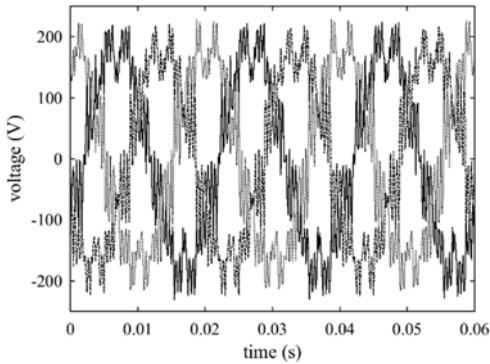


Fig. 11. Line to neutral voltage waveforms for three phases of the induction motor for $f = 50$ Hz for standard and additional conducting states of transistors

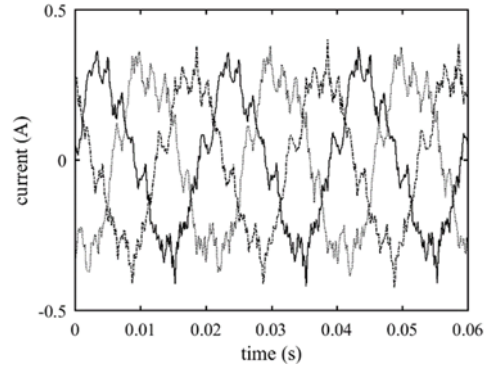


Fig. 12. Current waveforms for three phases of the induction motor for $f = 50$ Hz for standard and additional conducting states of transistors

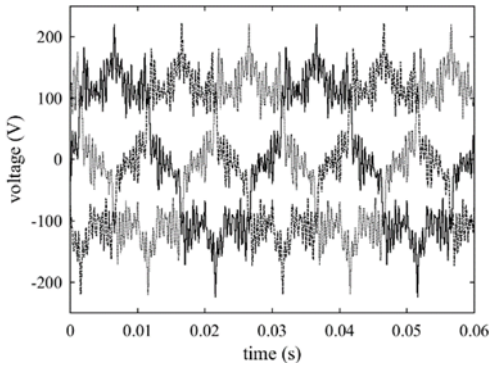


Fig. 13. Line to neutral voltage waveforms for three phases of the induction motor for $f = 33.33$ Hz for standard conducting states of transistors

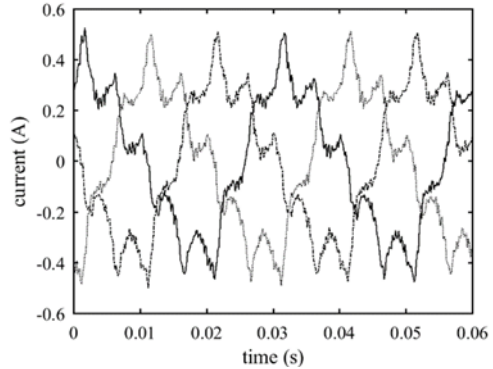


Fig. 14. Current waveforms for three phases of the induction motor for $f = 33.33$ Hz for standard conducting states of transistors

In Figures 9–12, three periods, while in Figs. 13–16 only two periods of waveforms are presented. Measurements were taken without any filters. The absence of filters is visible in Fig. 17 which presents the example harmonic spectrum of motor line to neutral voltages. Algorithm was not optimized for low THD in this tests. THD for standard conducting states of transistors and $f = 50$ Hz: $L_{V1} = 19.91\%$, $L_{V2} = 18.92\%$, $L_{V3} = 18.84\%$, $L_{I1} = 21.73\%$, $L_{I2} = 21.02\%$, $L_{I3} = 23.17\%$. THD for standard and additional conducting

states of transistors and $f=50$ Hz: $L_{V1} = 19.49\%$, $L_{V2} = 18.43\%$, $L_{V3} = 18.51\%$, $L_{I1} = 20.74\%$, $L_{I2} = 19.72\%$, $L_{I3} = 22.06\%$.

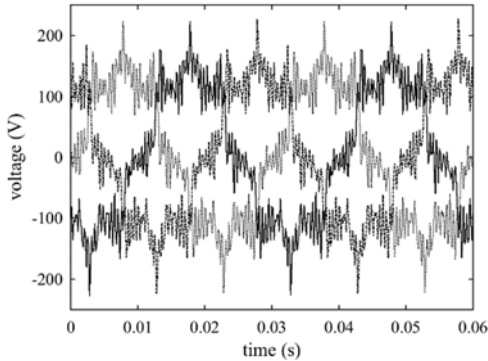


Fig. 15. Line to neutral voltage waveforms for three phases of the induction motor for $f=33.33$ Hz for standard and additional transistors conducting states

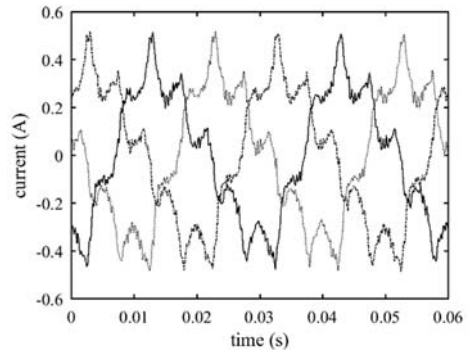


Fig. 16. Current waveforms for three phases of the induction motor for $f=33.33$ Hz for standard and additional transistors conducting states

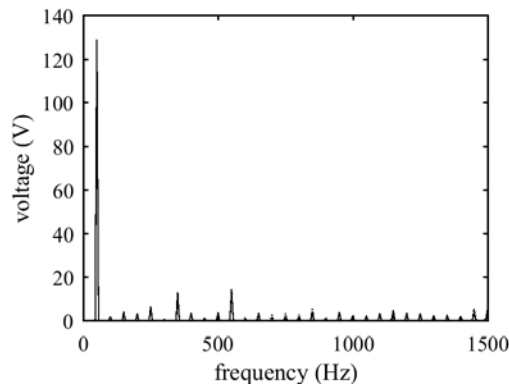


Fig. 17. Harmonic spectrum of motor line to neutral voltages for $f=50$ Hz for standard and additional conducting states of transistors.

The results of measurements presented in Figs. 9–16 show that using additional sets of transistors' states per voltage vector do not introduce significant changes to the output voltage and current waveforms. The THD levels are also consistent.

Thanks to additional sets of transistors' states, a switch count reduction was achieved. The number of individual transistors' state changes for one period is presented in Table 1. Examples with and without additional sets of transistors' states have been compared.

Table 1 shows that a modified SVM algorithm which uses additional sets of transistors' states allows considerable switch count reduction in a 3L-NPC inverter.

Table 1. Sums of individual state changes of every transistor in one period

Frequency [Hz]	Standard sets	Standard and additional sets
25	716	686
33.33	666	635
37.5	622	557
50	268	239

Measurements of dynamic response of the converter will be done after implementation of the algorithm on faster microcontroller which is the subject of ongoing research.

5. CONCLUSION

Thanks to additional sets of transistors' states, and the use of a prediction algorithm, it is possible to reduce considerably the transistors switch count. The authors presented measurements of working prototype converter using modified SVM algorithm, only with sets which did not require measurement of the inverter output current flow. This measurements prove that additional sets of transistors' states can be used in three-level neutral point clamped inverter without introducing significant changes to the output voltage and current waveforms.

Testing of all additional states will be done after major modifications of measurement and driving side of the converter. This may lead to further improvement of the presented algorithm.

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