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Fault-tolerant control for three-phase three-level T-type inverters with a redundant leg

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Abstract: Three-level T-type inverters have lower total harmonic distortion in output voltage, higher power density and lower voltage stress of power switches compared with conventional two-level inverters and have been widely used in applications with a wide-power range. Reliability improvement is particularly important for the T-type inverters because of the increased number of power switches and high system complexity. This paper proposes a fault-tolerant topology, which is constructed by adding a redundant leg including half-bridge switches and neutral-point switches connected between the DC bus capacitors and the DC-link midpoint of the conventional T-type inverter. In addition, an after-fault control strategy is proposed based on the results of a fault diagnosis method using bridge voltage. The fault-tolerant control of the open-circuit fault of the power switches and the phase-leg fault can both be achieved by the proposed method. Experimental results are given to verify that the proposed fault-tolerant three-level T-type inverter can output the full voltage level and power during the fault-tolerant operation based on the proposed control strategy.

Key words: fault diagnosis, fault-tolerant control, open-circuit fault, phase-leg fault, redundant leg, T-type inverter

1. Introduction

T-type inverters have been widely used in many industrial applications, such as renewable energy systems, grid-tie applications, traction inverters, and induction motor control systems [1–4]. T-type inverters are transformed from neutral-point-clamped (NPC) inverters, but have lower conduction losses and higher efficiency compared with the NPC inverters [5–7]. In addition,

there are other advantages that T-type inverters have such as lower total harmonic distortion in output voltage, higher power density and lower voltage stress of power switches compared with the conventional two-level inverters. However, like other multilevel inverters, the probability of failure in T-type inverters is lifted because of the increased number of power switches and high system complexity. Hence, fault diagnosis and fault-tolerant control becomes more important to ensure the reliability of the T-type inverters especially in safety critical applications.

Figure 1 shows the schematic of a three-phase three-level T-type inverter ($3LT^2I$) [6]. The conventional two-level voltage source inverter topology is extended with a bidirectional active switch to the DC-link midpoint "o". In this topology, the half-bridge switches (S_{x1} and S_{x4}, x represents a, b, and c) have to block the full DC-link voltage, the same as a conventional two-level inverter. Differently, the neutral-point switches (S_{x2} and S_{x3}) have to block only half of the DC-link voltage. Therefore, it is possible to adopt the devices with a lower voltage rating. Compared to the three-level NPC topology [5], the $3LT^2I$ uses a single switch to block the full DC-link voltage instead of two switches connected in series to block the full DC-link voltage. Therefore, the conduction losses of the $3LT^2I$ are considerably reduced. The $3LT^2I$ basically combines the advantages of the two-level converters such as low conduction losses and simple operation principles with the advantages of the multilevel converters [6].

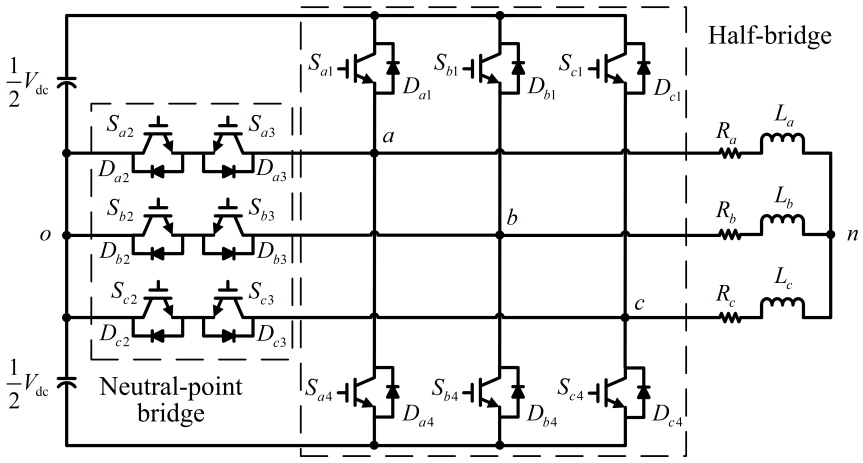


Fig. 1. Schematic of the three-level T-type inverter topology

The reliability of power electronic inverters is very important to any advanced electrical system because it is related to the cost and efficiency of the overall system. Therefore, to improve the reliability of the systems, many efforts have been made on fault diagnosis and fault-tolerant control for many kinds of converters [8–10].

Different effective methods to enhance the fault-tolerant capability of T-type inverters have been proposed in some publications. One popular fault-tolerant method is based on space vector modulation because the multilevel inverters have more switching state combinations compared with two-level inverters [11–15]. In this kind of methods, the topology of T-type inverters remains unchanged and only different control strategies are studied for the fault-tolerant purpose. In [11]

and [12], a fault-tolerant strategy based on replacing the switching state or changing the dwell time of the switching state is proposed by dividing into two cases: the faulty condition of half-bridge switches and neutral-point switches in T-type inverters. The methods proposed in [12] are analyzed and compared in [13], and two different fault-tolerant control methods are proposed, named as improved two-level switching tolerant control and hybrid switching tolerant control. Both methods in [13] are implemented by adding an optimal time-offset to the three-phase turn-on times. In the case of the open-circuit fault in T-type inverters and the large voltage vectors becoming impossible to obtain, a fault-tolerant control strategy based on the possible zero and small voltage vectors is proposed to avoid the distortion of the output voltage [14]. A fault-tolerant PWM control algorithm for a three-level quasi-switched boost T-type inverter is implemented in [15] by selecting appropriate values for the modulation index and duty cycles of two additional switching devices.

Another kind of fault-tolerant method is achieved by adding several redundant power devices and the topology of the inverters is changed such as the circuit topologies detailed in [16–22]. When there is a fault in T-type inverters, some output voltage levels couldn't be obtained. In order to obtain these lost voltage levels again, some new current paths based on the redundant devices should be rebuilt. A four-leg fault-tolerant T-type inverter topology is proposed with additional four insulated gate bipolar transistors (IGBTs) providing a fault-tolerant solution to open-circuit and certain short-circuit faults in the power switches [16, 17]. In this inverter, the overload capability is also increased compared to the conventional T-type inverters. A proposed topology of the fault-tolerant control includes four additional triode AC (TRIAC) semiconductor switches and three IGBTs compared with the classical three-level T-type inverter [18]. Here, when a switch fault occurs in half-bridge switches or neutral-point switches of T-type inverters, one IGBT can be shared in both cases. In [19], a fault-tolerant T-type inverter is proposed and fault-tolerant control strategies are investigated for both half-bridge and neutral-point switches. Under fault-tolerant operation, the redundant fourth-leg of this inverter is also used to balance neutral-point voltage. In [20], a fault-tolerant topology modification for three-level T-type inverters is proposed to achieve the fault-tolerant operation in the case of switch open-circuit or short-circuit failures without degradation of output capacity. A redundant unit that can be shared across phases in a T-type three-level inverter is proposed to manage open-circuit faults [21]. There are two IGBTs and six diodes in the redundant unit, and open-circuit faults in multiple legs of the inverter can be tolerated simultaneously. In [22], a fault-tolerant topology is proposed for an active T-type three-level converter to ensure that the converter can be operated continuously under open-circuit faults. Under fault conditions, the proposed topology can keep its outputs without degradation of the performance.

In this paper, a fault-tolerant three-phase three-level T-type inverter topology with a redundant unit added to a conventional T-type inverter is proposed and evaluated. Based on this topology, an additional current path will be provided and the full output capability can be obtained when there is an open-circuit fault in power switches or a phase-leg fault occurs. The remainder content of this paper is organized as follows. In Section 2, different faults of the inverter are analyzed. A fault diagnosis method based on three-phase bridge voltages and the proposed fault-tolerant topology is represented in Section 3 and Section 4, respectively. To verify the proposed fault-tolerant topology, experimental results are demonstrated in Section 5. Finally, conclusions are given in Section 6.

2. Fault analysis

As shown in Fig. 1, "a", "b", and "c" are three half-bridge midpoints, from where the three-phase load is connected, and "o" is the DC-link midpoint. The voltage v_{xo} (x represents a, b, and c) between the half-bridge midpoint "x" and the DC-link midpoint "o" is named as "bridge voltage'. Three bridge voltages under different switching states and switching command combinations are listed in Table 1. There are three switching states in the 3LT^{2}I: the positive state [P] with the bridge voltage is $+V_{\mathrm{dc}}/2$, the neutral state [O] with the bridge voltage is zero, and the negative state [N] with the bridge voltage is $-V_{\mathrm{dc}}/2$.

Table 1. Switching states, switching command combinations and bridge voltage of 3LT^{2}I

Switching state	S_{x1}	S_{x2}	S_{x3}	S_{x4}	**Bridge voltage**
[P]	on	on	off	off	$+V_{\mathrm{dc}}/2$
[O]	off	on	on	off	0
[N]	off	off	on	on	$-V_{\mathrm{dc}}/2$

The multi-carrier modulation strategy of the three-level T-type inverter is shown in Fig. 2, where G_{s1}, G_{s2}, G_{s3} and G_{s4} are the four drive signals of the power switches S_{x1}, S_{x2}, S_{x3} and S_{x4} (x represents a, b, and c), respectively. In the figure, u_{sx} is the sine modulation wave of the phase-x, u_{c1} and u_{c2} are the two triangular carriers of the inverter, respectively. When $u_{sx} > u_{c1}$, S_{x1} in the T-type inverter is turned on, and when $u_{sx} < u_{c1}$, S_{x1} is turned off. When $u_{sx} > u_{c2}$, S_{x2} in the T-type inverter is turned on, and when $u_{sx} < u_{c2}$, S_{x2} is turned off. The drive signal of S_{x3} is complementary to S_{x1}, and the drive signal of S_{x4} is complementary to S_{x2}.

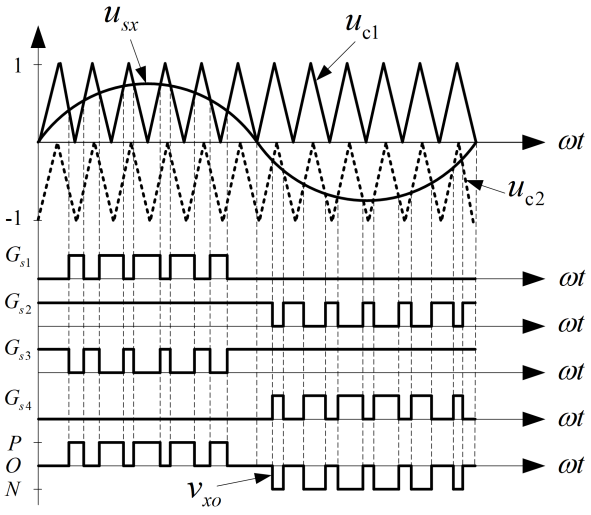


Fig. 2. Multi-carrier modulation strategy of the three-level T-type inverter

Considering the circuit symmetry of the 3LT^{2}I, only three cases of fault modes that could happen and can be tolerated here to represent all possible fault modes will be discussed in this paper. These three cases of fault modes include:

1) open-circuit fault in switch S_{a1};

2) open-circuit fault in switch S_{a2};

3) phase-leg fault in phase-a.

2.1. Case 1: open-circuit fault in switch S_{a1}

If an open-circuit fault occurs in S_{a1}, as can be seen from Table 1, the switching state [P] may be influenced and the bridge voltage will also be affected. According to the direction of the phase current, there are two situations that should be discussed. On the one hand, if the phase current $i_a > 0$ (taking the current direction shown in Fig. 3(a) as reference), Fig. 3(a) shows the change of the phase current path before and after the S_{a1} open-circuit fault. When the open-circuit fault of S_{a1} occurs, the phase current will flow through S_{a2} and D_{a3} instead of S_{a1} as shown in Fig. 3(a). As a result, the switching state will change from [P] to [O]. On the other hand, if the phase current $i_a < 0$, the phase current could flow through D_{a1} in the switching state [P], so the phase current path and the switching state will not change after the S_{a1} open-circuit fault. Figure 3(b) shows the bridge voltage under the S_{a1} open-circuit fault. It is shown that the bridge voltage v_{ao} maintains zero in the fault period after the S_{a1} open-circuit fault occurs, where the fault period starts with occurring of the time S_{a1} open-circuit, and ends at the half phase point of the bridge voltage.

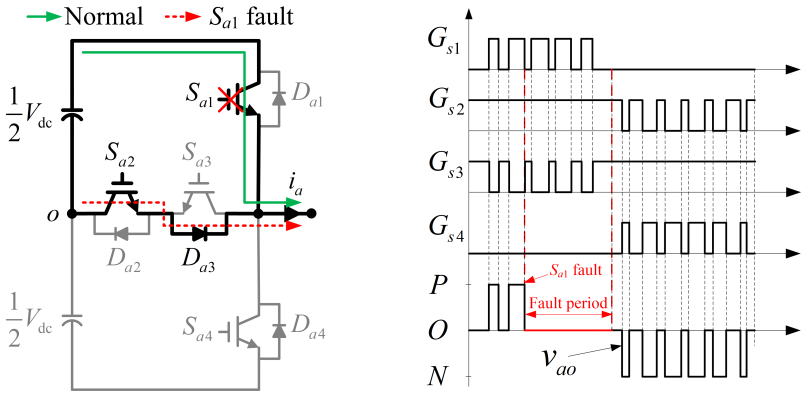


Fig. 3. Phase current and bridge voltage under S_{a1} open-circuit fault: current path (a); gate drive signals and bridge voltage (b)

2.2. Case 2: open-circuit fault in switch S_{a2}

If an open-circuit fault occurs in S_{a2}, it is more complicated since both the switching states [P] and [O] may be influenced as shown in Table 1.

Switching state [P]: The phase current flows through D_{a1} if the phase current $i_a < 0$, and the phase current flows through S_{a1} if the phase current $i_a > 0$. Hence, the phase current path and the bridge voltage will not be influenced under the S_{a2} open-circuit fault at this switching state.

Switching state [O]: If the phase current $i_a > 0$, Fig. 4(a) shows the difference in the phase current path before and after the S_{a2} open-circuit fault. When the open-circuit fault of S_{a2} occurs, the phase current will flow through D_{a4} as shown in Fig. 4(a). As a result, the switching state will change from [O] to [N]. If the phase current $i_a < 0$, the phase current could flow through S_{a3} and D_{a2} in the switching state [O], so the phase current path and the switching state will not change before and after the S_{a2} open-circuit fault. Figure 4(b) shows the bridge voltage under the S_{a2} open-circuit fault. It is shown that the bridge voltage is alternating between $+V_{\mathrm{dc}}/2$ and $-V_{\mathrm{dc}}/2$ in the fault period after the S_{a2} open-circuit fault occurs.

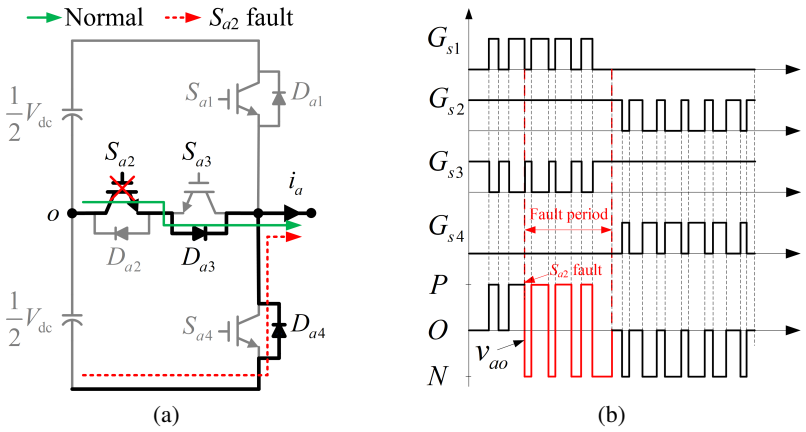


Fig. 4. Phase current and bridge voltage under S_{a2} open-circuit fault: current path (a); gate drive signals and bridge voltage (b)

2.3. Case 3: phase-leg fault in phase-*a*

Among various faults of three-level T-type inverters, the phase-leg fault is a typical one and it can be caused by different power switches or stator windings when used for motor drives [23]. Some fault-tolerant control strategies have been proposed for phase-leg faults as mentioned above. The phase-leg fault will force the current in the faulty phase from normal to zero as shown in Fig. 5(a), which is easy to be concluded [24].

After phase-*a* stops working, two different voltage level include $+V_{\mathrm{dc}}/4$ and $-V_{\mathrm{dc}}/4$ will appear in the bridge voltage v_{ao}. This is because when the phase current $i_a = 0$, the electric potential at the half-bridge midpoint "*a*" in Fig. 1 is equal to the one at the load midpoint "*n*". As a result, the level of the bridge voltage v_{ao} is determined by the other two bridge voltages v_{bo} and v_{co}. At this time, phase-*b* and phase-*c* are still working normally. For example, when $v_{bo} = +V_{\mathrm{dc}}/2$ and $v_{co} = 0$, it can be calculated that $v_{ao} = +V_{\mathrm{dc}}/4$. Other possible level combinations of three bridge voltages are shown in Table 2. The corresponding bridge voltage v_{ao} after the fault occurs is also shown in Fig. 5(b).

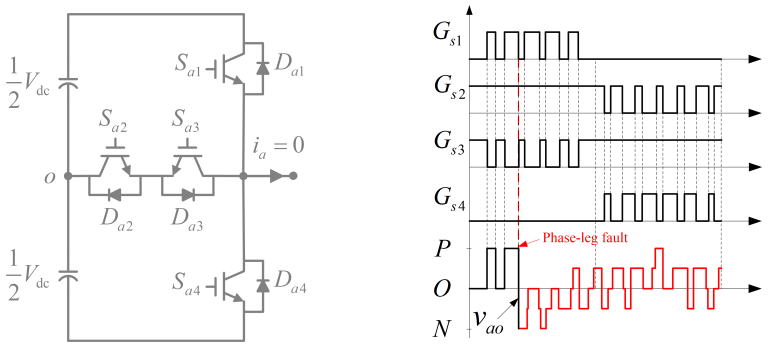


Fig. 5. Phase current and bridge voltage under phase-leg fault in phase-a: current path (a); gate drive signals and bridge voltage (b)

Table 2. Possible levels of bridge voltage v_{ao} when $i_a = 0$

v_{bo}	v_{co}	$v_{ao} = (v_{bo} + v_{co})/2$
$+V_{dc}/2$	$+V_{dc}/2$	$+V_{dc}/2$
$+V_{dc}/2$	0	$+V_{dc}/4$
$+V_{dc}/2$	$-V_{dc}/2$	0
0	$+V_{dc}/2$	$+V_{dc}/4$

3. Fault diagnosis

It can be seen from Section 2 that the bridge voltage will become distorted under different fault modes of the three-level T-type inverter. A fault diagnosis method based on the bridge voltage is proposed to distinguish which case of the fault modes occurs. The flow diagram of the fault diagnosis method is shown in Fig. 6.

Firstly, the acquired bridge voltages should be rectified by a full-wave rectifier for next process. If there is no fault in the inverter, the bridge voltage is in a normal condition. Hence, a fault period

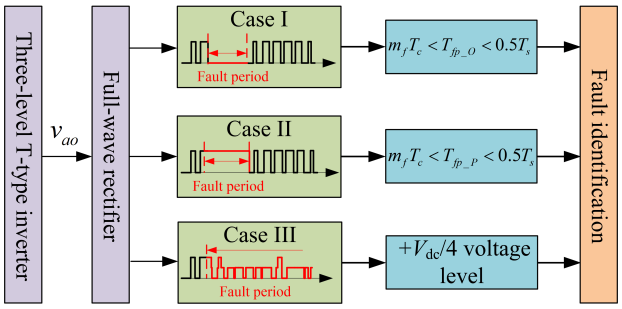


Fig. 6. Flow diagram of the fault diagnosis method for three-level T-type inverter

which is much more than the carrier period T_c will not appear and there is no voltage level equal to $+V_{\mathrm{dc}}/4$. For each case of the three fault modes, the fault period shown in Fig. 6, can be identified. In case 1 and case 2, there are two different types of fault period according to the level of the bridge voltage. If the bridge voltage is $+V_{\mathrm{dc}}/2$ in the fault period, the fault period is named as T_{fp_P}, and if the bridge voltage is zero in the fault period, the fault period is named as T_{fp_O}. In case 3, the voltage level $+V_{\mathrm{dc}}/4$ will appear in the bridge voltage v_{ao}. The fault identification rules are shown below.

1) If $m_f T_c < T_{fp\_O} < 0.5T_s$, where T_c is the carrier period and T_s is the period of the bridge voltage (the same period as the sine modulation wave), an open-circuit fault occurs in S_{a1} or S_{a4}. When the fault period appears in the positive part of the bridge voltage, the fault switch must be S_{a1}. If the fault period appears in the negative part of the bridge voltage, the fault switch must be S_{a4}. Whether the bridge voltage is in the positive part or negative part, can be judged by the polarity of the sine modulation wave as shown in Fig. 2.

2) If $m_f T_c < T_{fp\_P} < 0.5T_s$, an open-circuit fault occurs in S_{a2} or S_{a3}. When the fault period appears in the positive part of the bridge voltage, the fault switch must be S_{a2}. If the fault period appears in the negative part of the bridge voltage, the fault switch must be S_{a3}. The judgment method of the polarity of the bridge voltage is the same as rule 1).

3) If a voltage level equal to $+V_{\mathrm{dc}}/4$ appears in the bridge voltage v_{ao}, the phase-leg fault occurs in phase-a.

In rules 1) and 2), m_f is a coefficient according to the ratio of carrier frequency to modulation frequency. The coefficient $m_f = 5$ in this paper as the carrier frequency is 1.5 kHz and the modulation frequency is 50 Hz. The complete fault diagnosis method for three phases of the three-level T-type inverter can be seen in Table 3.

Table 3. Fault diagnosis method for the three-level T-type inverter

Bridge voltage	**After rectification**	**Fault period**	**Modulation wave**	**Fault mode**
v_{ao}	v_{ao_rec}	$m_f T_c < T_{fp\_O} < 0.5T_s$	$u_{sa} > 0$	S_{a1} open-circuit
			$u_{sa} < 0$	S_{a4} open-circuit
		$m_f T_c < T_{fp\_P} < 0.5T_s$	$u_{sa} > 0$	S_{a2} open-circuit
			$u_{sa} < 0$	S_{a3} open-circuit
		$+V_{\mathrm{dc}}/4$ voltage level		Phase-a-leg fault
v_{bo}	v_{bo_rec}	$m_f T_c < T_{fp\_O} < 0.5T_s$	$u_{sb} > 0$	S_{b1} open-circuit
			$u_{sb} < 0$	S_{b4} open-circuit
		$m_f T_c < T_{fp\_P} < 0.5T_s$	$u_{sb} > 0$	S_{b2} open-circuit
			$u_{sb} < 0$	S_{b3} open-circuit
		$+V_{\mathrm{dc}}/4$ voltage level		Phase-b-leg fault
v_{co}	v_{co_rec}	$m_f T_c < T_{fp\_O} < 0.5T_s$	$u_{sc} > 0$	S_{c1} open-circuit
			$u_{sc} < 0$	S_{c4} open-circuit
		$m_f T_c < T_{fp\_P} < 0.5T_s$	$u_{sc} > 0$	S_{c2} open-circuit
			$u_{sc} < 0$	S_{c3} open-circuit
		$+V_{\mathrm{dc}}/4$ voltage level		Phase-c-leg fault

4. Fault-tolerant control

A fault-tolerant control three-level T-type inverter topology is shown in Fig. 7 in order to obtain high reliability of the inverter system. As it can be seen, there is a redundant leg including half-bridge switches (S_{t1} and S_{t2}) and neutral-point switches (S_{t2} and S_{t3}) connected between the DC bus capacitors and the DC-link midpoint "o" of the conventional T-type inverter. In addition, there are three TRIACs (T_a, T_b and T_c) connected between the midpoint of the redundant leg and the half-bridge midpoint "x" of the conventional T-type inverter. During normal operation or healthy conditions, four IGBTs of the redundant leg and three additional TRIACs are all in the turn-off state. Hence, there is no extra power loss.

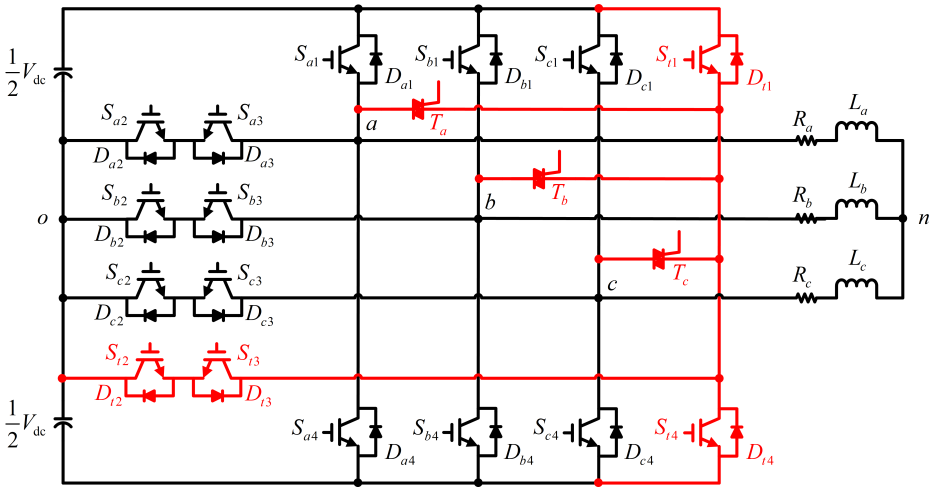


Fig. 7. Proposed fault-tolerant control three-level T-type inverter topology

The proposed fault-tolerant control topology has the capability to tolerate all fault modes that include open-circuit faults and phase-leg faults. The four IGBTs of the redundant leg are sized to be the same as the three main phase legs. Based on the fault diagnosis method mentioned above, once these fault modes are detected and identified, the faulty switch or leg should be isolated firstly, and then the differently modified T-type inverter topologies and fault-tolerant control strategies will be implemented to obtain fault-tolerant function.

If an open-circuit fault occurs in S_{a1} or S_{a4}, the switches S_{a1} and S_{a4} should be both isolated. The modified fault-tolerant inverter topology is shown in Fig. 8 under this kind of fault mode. In the figure, the TRIACs T_a is controlled to be turned on. The switching command for S_{a2} and S_{a3} are not changed and the switches S_{t2} and S_{t3} are controlled to be turned off. The drive signal of the switches S_{a1} and S_{a4} are applied to the switches S_{t1} and S_{t4}, respectively. As a result, the switches S_{t1} and S_{t4} will replace the switches S_{a1} and S_{a4}.

If an open-circuit fault occurs in S_{a2} or S_{a3}, the switches S_{a2} and S_{a3} should be both isolated. The modified fault-tolerant inverter topology is shown in Fig. 9 under this kind of fault mode. In the figure, the TRIACs T_a is controlled to be turned on. The switches S_{t1} and S_{t4} are both

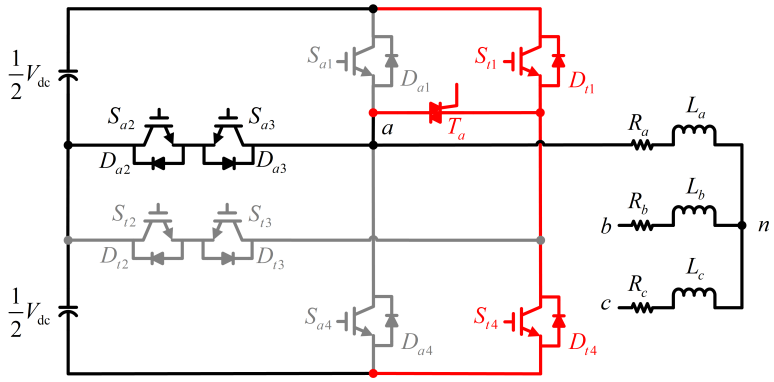


Fig. 8. Modified fault-tolerant control topology under S_{a1} or S_{a4} open-circuit fault

controlled to be turned off. The switching command for S_{a1} and S_{a4} are not changed. The drive signal of the switches S_{a2} and S_{a3} are applied to the switches S_{t2} and S_{t3}, respectively. As a result, the switches S_{t2} and S_{t3} will replace the switches S_{a2} and S_{a3}.

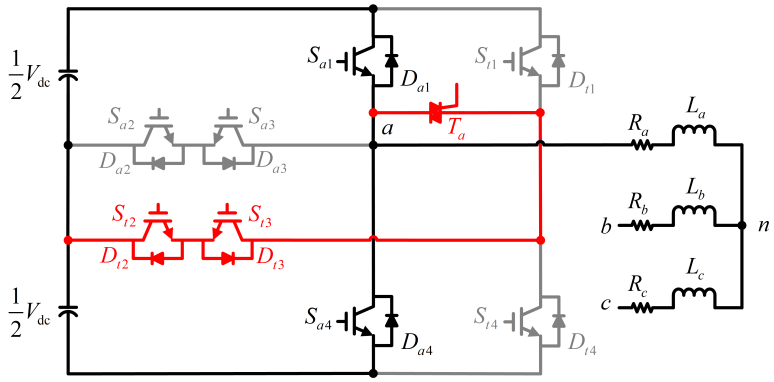


Fig. 9. Modified fault-tolerant control topology under S_{a2} or S_{a3} open-circuit fault

If a phase-leg fault occurs in phase-a, the original switches of phase-a include S_{a1}, S_{a2}, S_{a3}, and S_{a4} should all be isolated. The modified fault-tolerant inverter topology is shown in Fig. 10 under this kind of fault mode. In the figure, the TRIACs T_a is controlled to be turned on. The drive signal of the switches S_{a1}, S_{a2}, S_{a3}, and S_{a4} are applied to the switches S_{t1}, S_{t2}, S_{t3}, and S_{t4}, respectively. As a result, the post-tolerant phase-a composed of switches S_{t1}, S_{t2}, S_{t3}, and S_{t4} is connected to load R_a and L_a through the TRIACs T_a.

Taking the entire three-level T-type inverter into consideration, the switches should be isolated, and the redundant switches controlled to replace the isolated switches under different fault modes are shown in Table 4. The corresponding TRIACs that should be turned on during the fault-operation are listed too. It should be noted that the inverter is able to output the full level and power during the fault-tolerant operation by this fault-tolerant control strategy.

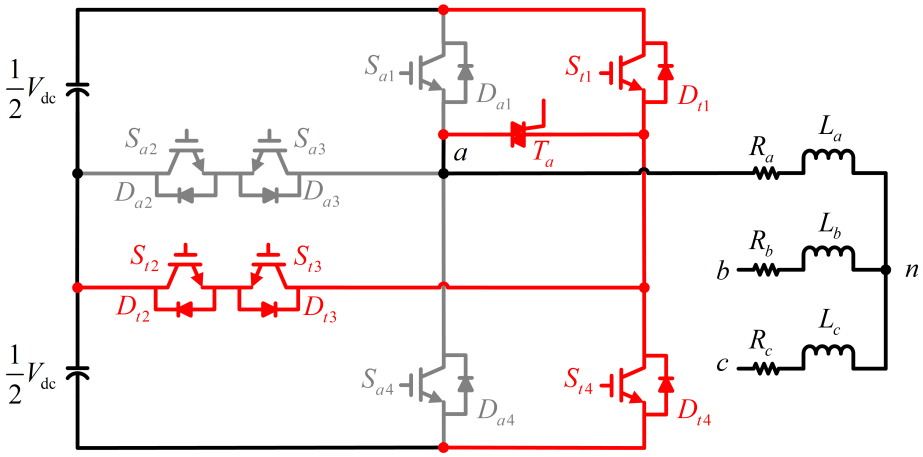


Fig. 10. Modified fault-tolerant control topology under phase-leg fault in phase-*a*

Table 4. Fault-tolerant control strategy of the three-level T-type inverter

Faulty switch	Isolated switches	Redundant switches	On TRIACs
S_{a1} or S_{a4}	S_{a1}, S_{a4}	S_{t1}, S_{t4}	T_a
S_{a2} or S_{a3}	S_{a2}, S_{a3}	S_{t2}, S_{t3}	T_a
S_{b1} or S_{b4}	S_{b1}, S_{b4}	S_{t1}, S_{t4}	T_b
S_{b2} or S_{b3}	S_{b2}, S_{b3}	S_{t2}, S_{t3}	T_b
S_{c1} or S_{c4}	S_{c1}, S_{c4}	S_{t1}, S_{t4}	T_c
S_{c2} or S_{c3}	S_{c2}, S_{c3}	S_{t2}, S_{t3}	T_c
Phase-*a*-leg	S_{a1}, S_{a2}, S_{a3}, S_{a4}	S_{t1}, S_{t2}, S_{t3}, S_{t4}	T_a
Phase-*b*-leg	S_{b1}, S_{b2}, S_{b3}, S_{b4}	S_{t1}, S_{t2}, S_{t3}, S_{t4}	T_b
Phase-*c*-leg	S_{c1}, S_{c2}, S_{c3}, S_{c4}	S_{t1}, S_{t2}, S_{t3}, S_{t4}	T_c

The flow chart of fault diagnosis and the fault-tolerant control strategy is shown in Fig. 11. In the figure, "*x*" represents the three-phase symbols, "*a*", "*b*", and "*c*" as mentioned before. Firstly, three-phase bridge voltages are collected and rectified. Then the fault period of any bridge voltage should be calculated and the level of the corresponding bridge voltage is judged following the fault identification rules described in Section 3. If the calculation results do not meet these rules, it means that the three-level T-type inverter is in the fault-free condition and the three-phase bridge voltages will be collected again. If the calculation results meet any identification rule, the fault mode of the three-level T-type inverter can be confirmed. At last, based on the fault diagnosis results, the fault-tolerant control strategy shown in Table 4 will be implemented to ensure the inverter works under normal conditions.

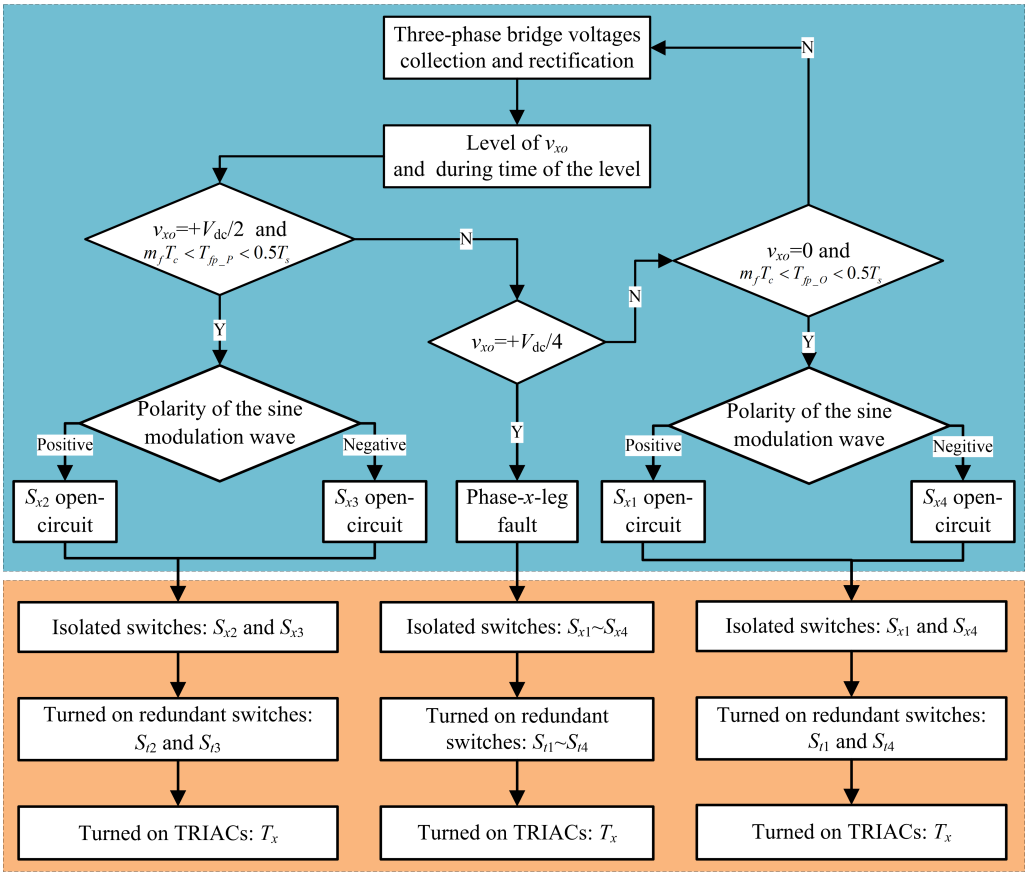


Fig. 11. Flow chart of fault diagnosis and fault-tolerant control strategy

5. Experimental results

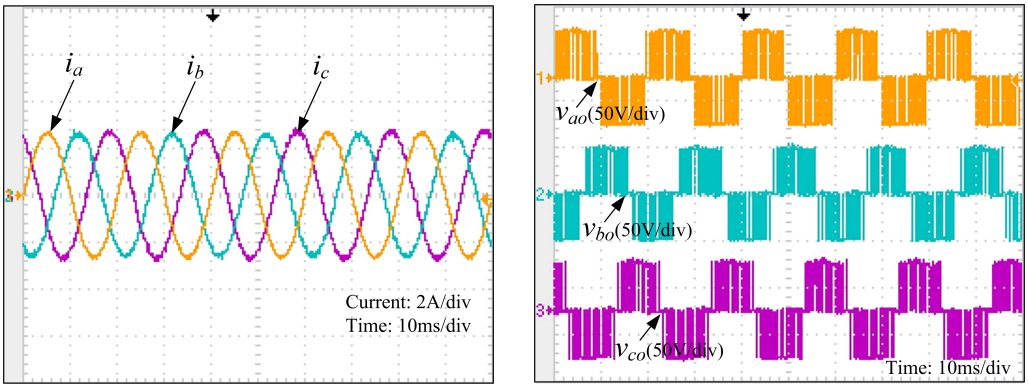
In order to verify the fault-tolerant capability of the proposed three-level T-type inverter topology and control strategy, an experimental platform is built in the laboratory. The experimental parameters are given in Table 5. Infineon IGBT K75EES5 is used to constitute the conventional T-type inverter and the redundant leg. The system is controlled by a digital signal processing (DSP) board based on TMS320F2812. The modulation, fault generation and fault-tolerant control of the inverter system are all implemented by the DSP.

Figure 12 shows the three-phase current and bridge voltage waveforms when there is no fault in the three-level T-type inverter. It can be seen from the figure that the phase current waveform is a sine waveform without any distortion and the bridge voltage is a standard three-level waveform.

In the experiments, the open-circuit fault mode is emulated by setting the drive signals of the power devices to zero which is controlled by the DSP board. The phase-leg fault mode is achieved by setting the drive signals of all power devices of one phase to zero. If an open-circuit fault

Table 5. Parameters of the experimental platform

Parameter name	Symbol	Value	Unit
DC-link voltage	V_{dc}	100	V
Fundamental frequency	f_r	50	Hz
Carrier frequency	f_c	1.5	kHz
Load	R_x	10	Ω
	L_x	20	mH



(a) (b)

Fig. 12. Three-phase current and bridge voltage waveforms of the three-level T-type inverter under normal conditions: there-phase currents (i_a, i_b, and i_c) (a); three-phase bridge voltages (v_{ao}, v_{bo}, and v_{co}) (b)

occurs in S_{a1} or S_{a2}, the experiment results are shown in Fig. 13(a) and Fig. 13(b), respectively. Under fault conditions, the bridge voltage after-rectification v_{ao_rec} represents the fault periods T_{fp_O} and T_{fp_P} that can be used for fault diagnosis based on the fault identification rules. Figure 13(c) shows the experiment results when a phase-leg fault occurs in phase-a. It is obvious that the phase current i_a becomes zero and a voltage level equal to $+V_{\mathrm{dc}}/4$ appears in the bridge voltage after-rectification v_{ao_rec}.

Based on the fault diagnosis results, the fault-tolerant control strategy can be implemented and the experiment results are shown in Fig. 14. In all three experiment results of Fig. 14, the first cycle represents the normal condition, the next cycle represents the fault condition with distorted bridge voltages after-rectification and phase currents, and the last three cycles represents the fault-tolerant condition based on the proposed inverter topology and fault-control strategy. It is shown in the figure that the proposed method can keep its outputs without degradation of performance. In addition, the dead time from the fault occurs time to the fault-tolerant time is about 20 ms, the length of the dead time is depended on the speed of the fault-diagnosis method. If a faster fault-diagnosis method is adopted, this dead time could be shorter.

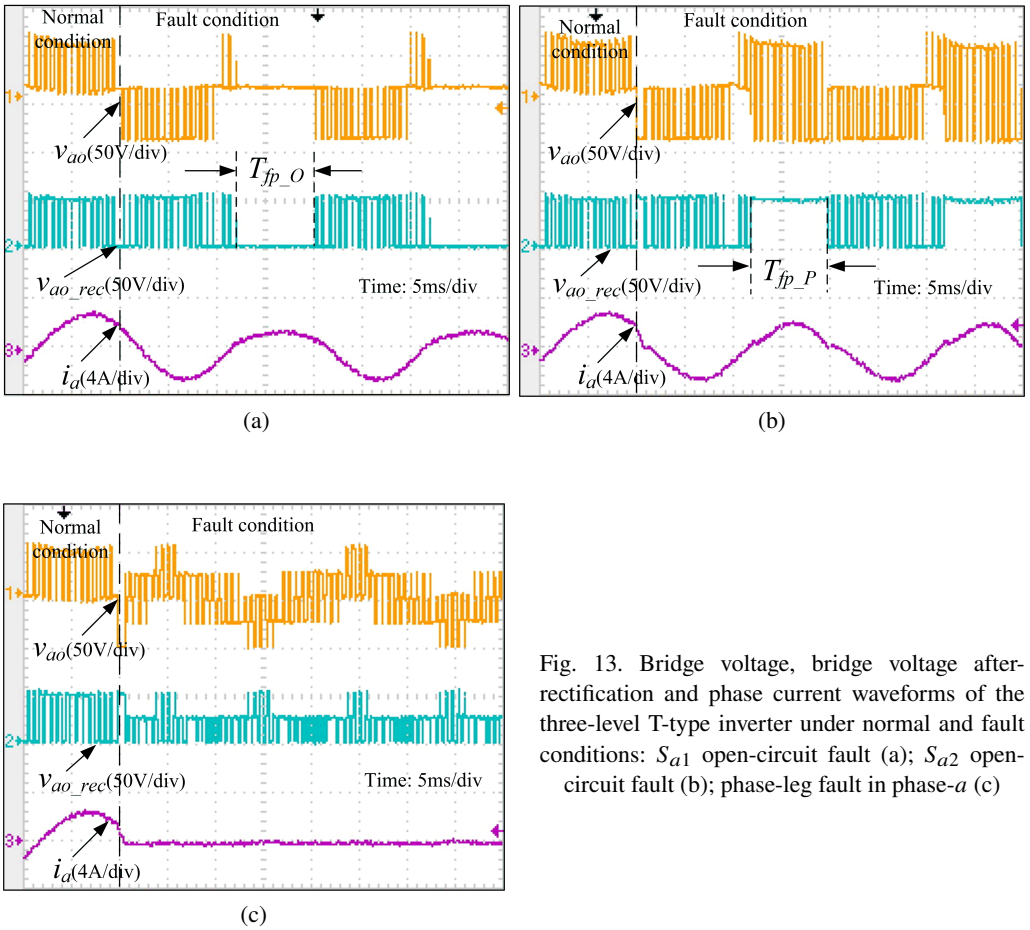
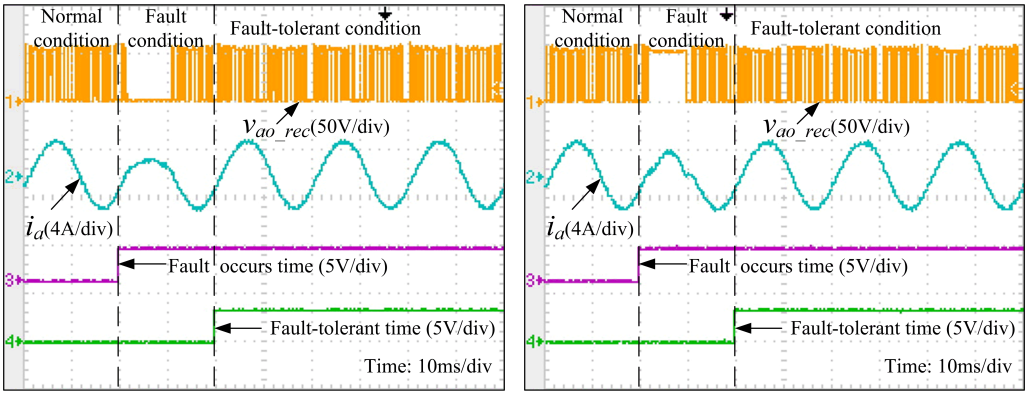
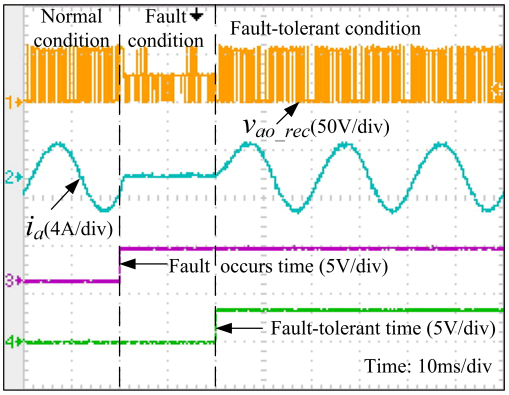


Fig. 13. Bridge voltage, bridge voltage after-rectification and phase current waveforms of the three-level T-type inverter under normal and fault conditions: S_{a1} open-circuit fault (a); S_{a2} open-circuit fault (b); phase-leg fault in phase-a (c)

The efficiency of the proposed three-level T-type inverter under normal and fault-tolerant conditions are both tested and compared at various output power percentages, as shown in Fig. 15(a). In all three cases of the fault-tolerant condition, only one TRIAC semiconductor switch is turned on additionally, compared with the normal condition as shown in Figs. 8–10. Therefore, only the efficiency of the S_{a1} open-circuit fault is tested under the fault-tolerant condition in the experiment. It can be seen that there is a small efficiency degradation under the fault-tolerant condition. For instance, under the 100% output power condition, the efficiency of the fault-tolerant condition is 0.41% lower than the normal condition. The reason is that there is one additional TRIAC semiconductor switch turned on under the fault-tolerant condition, and its conduction loss should be considered. The total power losses are tested under normal and fault-tolerant conditions, as shown in Fig. 15(b), which shows that the total power loss is 14.6 and 15.7 W under 100% output power condition, under normal and fault-tolerant conditions, respectively.

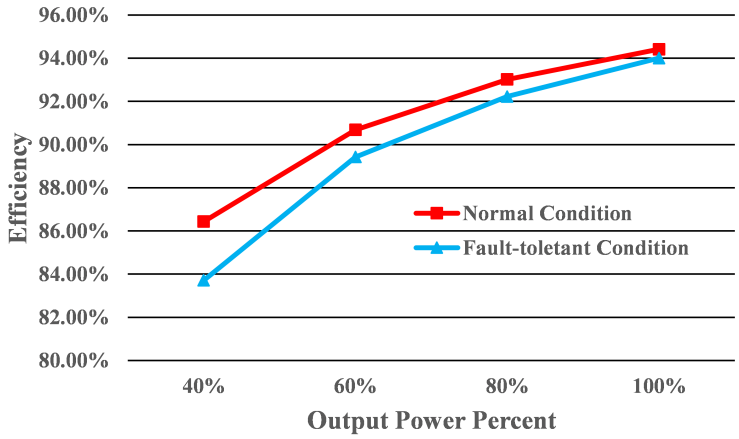


(a) (b)

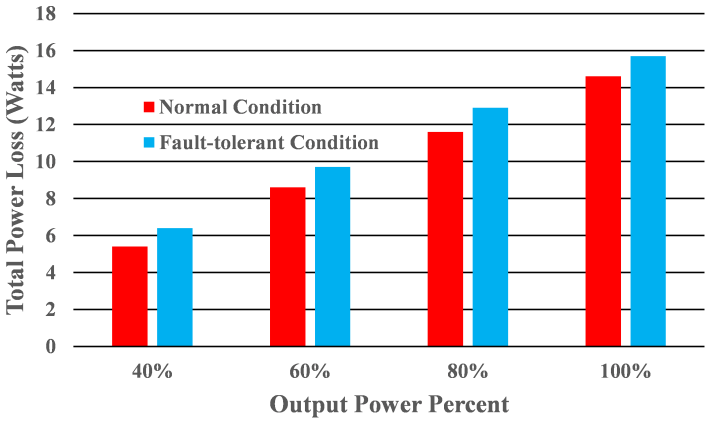


(c)

Fig. 14. Bridge voltage after-rectification, phase current, fault occurs time signal and fault-tolerant signal waveforms of the three-level T-type inverter under normal condition, fault condition and fault-tolerant condition: S_{a1} open-circuit fault (a); S_{a2} open-circuit fault (b); phase-leg fault in phase-a (c)



(a)



(b)

Fig. 15. Efficiency and total power losses of the three-level T-type inverter at various output power percentages: efficiency of the inverter under normal condition and fault-tolerant condition (a); total power losses under normal condition and fault-tolerant condition (b)

6. Conclusions

This paper proposes a fault-tolerant topology and control strategy of the three-phase three-level T-type inverter. The proposed topology is constructed by adding a redundant leg including half-bridge switches and neutral-point switches connected between the DC bus capacitors and the DC-link midpoint of the conventional T-type inverter. A fault diagnosis method based on bridge voltage is introduced to identify which fault mode is occurring in the inverter. Base on the results of the fault diagnosis, the redundant leg can isolate and replace the faulty switch or faulty leg and eliminate their influence. In this paper, the fault-tolerant control of the open-circuit fault of the power switches and the phase-leg fault can both be achieved by the proposed method. As shown in the experimental results, the proposed fault-tolerant three-level T-type inverter is able to output the full voltage level and power during the fault-tolerant operation based on the proposed control strategy. In addition, under normal operational or healthy conditions, the devices of the redundant leg are all in the turn-off state, so no extra power is lost.

Acknowledgements

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