A 400 fJ Per-Cycle Frequency Reference for Internet of Things

Mathieu Coustans, François Krummenacher, Christian Terrier, and Maher Kayal

***Abstract*—This work presents an ultra-low power oscillator designed to target different contexts, such as crystal-assisted time keeping, reference oscillator to optimize the always on domain of a microcontroller or wake-up timer. This oscillator enables ultra-low power operation in 0.18 µm CMOS technology; the core oscillator consumes 2.5 nW at room temperature, with a temperature stability of 14 ppm/°C [-40°C - 60°C] and 0.07 %/V supply sensitivity.**

***Index Terms*—time reference; supply voltage insensitivity; temperature insensitivity; ultra-low power; always on domain optimization.**

I. Introduction

POWER consumption is a critical element in the design of micro-controllers, compact wireless systems, and time keeping applications. Implementation of sleep or even deep sleep modes in such applications is enabled by duty-cycling and keeping track of the time. This standby mode is a key concern for the internet of things. Hence, it is vital to maintain accuracy while at the same time reducing power consumption to ensure proper time keeping or reference clock.

For accurate time keeping, crystal oscillators are the conventional choice [1] due to their excellent temperature and frequency stability [2]. However, they require an external element which drives up the system footprint and cost [3]. Recently, several publications have been made in the area of low-power precision oscillators due to an increasing demand of stable clock sources [4][5][6]. Some work has been done to cover the thermal variations [6][5]. Another type of conventional oscillator is the ring oscillator; the current starved ring oscillator [7] exhibits an improvement by a factor of 2 on phase noise performance (natural value). However, this is not precise enough for time keeping constraints.

Having a look at thermal compensation strategies [8][9], it is not so evident to find how a current controlled ring oscillator could be thermally compensated. The golden rule "make it as simple as possible" is violated, however, some good results were obtained such as in [10] at the cost of extra circuitry and higher frequency ending up in a 150nW design. If you take a step back and look at the concept of an RC oscillator is also a good candidate for resistive or capacitive sensor. A resistive temperature sensor was proposed in [11], where the sensor was a resistor with high temperature coefficient. In some applications the thermal coefficient of the resistor could fit thermal stability constraints [12]. Accurate knowledge of the physics behind a performance is often the correct way to achieve the expected performance through a system level approach.

This paper presents an overview of the limitation for nA design, with a review of fundamental limitations in section II. Section III presents the design of a temperature stable nA design of a RC oscillator. In section IV, we discuss the measurement results

II. Limitation and Challenge of nA Design

Addressing design at nA is a very critical task. State of the art process and design kit that intend to address ultra-low power design should provide:

- Low leakage transistors
- Good models for sub-threshold
- MOSFET edge conductance's removal
- Large resistor (100 MΩ required and 5 GΩ desirable).

Therefore, sticking to 180nm process is a good strategy. EKV 3 compact model were used. Nevertheless edge conductance's removal was not yet available in the used process. A large resistor is one of the fundamental limitations of CMOS processes to proceed in nA design.

A. Relaxation oscillators

Relaxation oscillators rely on the principle of a non-linear electronic oscillator circuit that produces a non-sinusoidal repetitive output signal, such as a triangle wave or square wave.

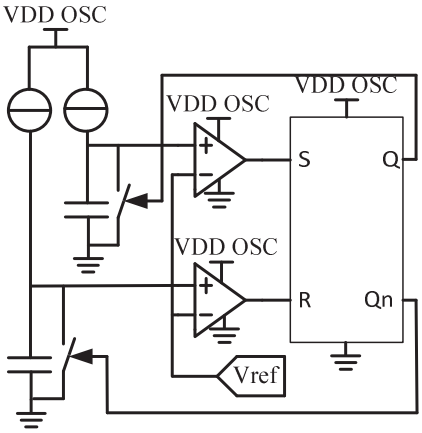

Fig. 1. Relaxation oscillator architecture

M. Coustans, F. Krummenacher and M. Kayal are with the Institute of Electrical Engineering (IEL), École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland (e-mail: mathieu.coustans@epfl.ch)

C. Terrier is with EM Microelectronic-Marin SA, Rue des Sors 3, 2074 Marin-Epagnier, Switzerland

The circuit (Fig. 1) consists of a feedback loop containing a switching device that repetitively charges a capacitor or inductor through a resistance until it reaches a threshold level, then discharges it again. The period of the oscillator depends on the time constant of the capacitor or inductor circuit. The active device switches abruptly between charging and discharging modes, and thus produces a discontinuously changing repetitive waveform. One of the most efficient way to implement such an oscillator is the mono-stable. The comparator could be implemented in a very efficient way with the source coupled comparator [13]. This implementation is taking advantage of weak inversion offset, which could be approximated to threshold voltage mismatch (VT) and could be solved by a larger footprint or offset cancellation technique in a regular comparator [4][6][5]. The fundamental thermal stability trade-off of any implementation of relaxation oscillator is between temperature-dependent comparator delay and comparator power.

B. *Ring oscillators*

Ring oscillators are intrinsically subject to a lot of controversy on their oscillations properties [13]. The simplest proposal is the following one:

$$F_{osc} = \frac{\mathrm{I_{bias}}}{V_{swing} \times C_{eq}} \tag{1}$$

There is a strong relation between power dissipation and operating frequency, which is only valid in a process where the leakage current is fairly negligible and the frequency is not so low that the two devices are simultaneously in conduction.

Another fundamental issue is that circuits such as random number generators are taking advantage of modelling ring oscillator performance as an entropy source, meaning that there is period jitter. While counting time, the lack of period accuracy creates a time count imprecision on the second for example while being perfectly accurate over one hour [14].

Intrinsically, both solutions, ring and relaxation oscillators, need power investment to fulfil thermal stability constraints.

III. Proposed Low Power Topology

A. *Circuit description*

Based on the temperature sensor proposed in [11], the circuit (Fig. 2) is balancing the DC current flowing into an on-chip resistor and the dynamic current supplied to a ring oscillator made of an odd number of CMOS inverters.

This is achieved thanks to a current mirror (M1, M2), which is not 100% true as long as the drain voltage is subject to change and mismatch. In principle, we could match the drains voltages equality by means of an OTA. This proposed solution can as well suffer from the OTA input offset, which is represented by the voltage source Vos.

The following system of equation could be deduced :

$$\mathrm{I_{Res}} = \frac{V_{Res}}{R} \tag{3}$$

$$\mathrm{I_{Ring}} = \mathrm{F}_{osc} \times \mathrm{C_{eq}} \times \mathrm{V_{ring}} \tag{4}$$

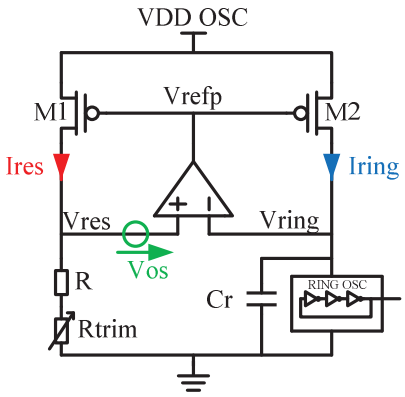

Fig. 2. Circuit architecture

The feedback loop is then imposed :

$$\mathrm{I_{Ring}} = \mathrm{I_{Res}} \tag{5}$$

$$\mathrm{V_{Ring}} = V_{Res} + \mathrm{V_{os}} \tag{6}$$

The oscillation frequency is then:

$$F_{osc} = \frac{1}{R \times C_{eq}} \times \left(1 - \frac{V_{os}}{V_{Ring}}\right) \tag{7}$$

This oscillator is then intrinsically dependent on a RC product, as offset voltage is mostly on the order of mV meanwhile the ring oscillator is operated necessary at a much higher voltage [15] which makes this part of (7) negligible for first order calculations. As a matter of fact, oscillation frequency rely on absolute values which could be trimmed in production, as the capacitance is defined by the inverter itself.

B. *Temperature behavior*

The thermal behaviour of this circuit is expected to be fairly dominated by variations of the thermal coefficient of the passive elements R and C. MOS capacitances were -7300 ppm/°C which is too high to achieve stable oscillation frequency over temperature. For the resistor, it is a trade-off between high resistivity and thermal behaviour. We end-up with a high resistive poly resistor with a thermal coefficient of -1950 ppm/°C which is also too high to achieve stable oscillation frequency for a time reference. To get a complete picture of the thermal dependency, we considered that each element in the expression (7) is subject to temperature drift, the corresponding first-order relative temperature coefficient [ppm/°C] of the oscillation frequency is then given by:

$$T_C = \frac{1}{F_{osc}} \times \frac{\partial}{\partial T} F_{osc} \tag{8}$$

Hence we obtained:

$$T_C = -T_{CRes} - T_{CCeq} + \frac{1}{V_{ring} + V_{os}} \times \left(T_{CVos} - T_{CVring} \frac{V_{os}}{V_{ring}}\right) \tag{9}$$

where the temperature coefficients R and C are expressed in ppm/°C, and temp coefficients of OTA offset voltage and ring oscillator voltage are expressed in µV/°C, in the designed OTA. The above result shows that a first-order compensation of the temperature drift can be achieved under specific conditions.

The novelty is then obtained without any additional current branch or circuitry to compensate the thermal behaviour. A perfectly matched load there remain two uncorrelated phenomena: random mismatch on threshold voltage and geometrical ratio. It could be easily proved that:

$$V_{os} = \sqrt{\left(n \times u_T \times ln(e^{IC} - 1)\frac{\Delta\frac{W}{L}}{\frac{W}{L}}\right)^2 + \Delta V_T^2} \quad (10)$$

To do so a structural mismatch element has been introduced in the differential pair (Fig. 3). The structural offset was implemented in a binary weighted fashion (M8.i, M9.i) additional W, which is between 0 and 31 times more than the other side of the differential pair.

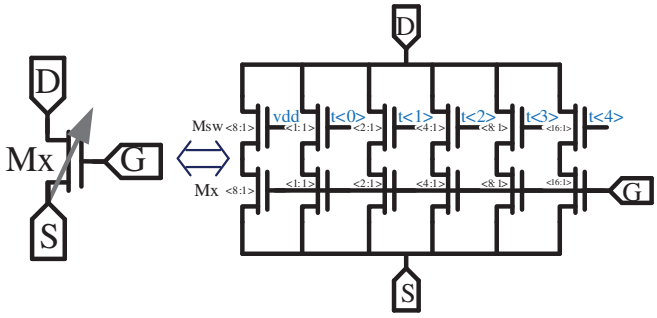

Fig. 3. Equivalent implementation of differential pair transistor

C. Power supply sensitivity

An oscillator is most likely embedded in a complex system on chip where some other blocks tend to generate dynamic IR drop. Accordingly, the sensitivity of the oscillator to a supply voltage variation should be minimized. Therefore, the selection of the OTA is then a very important point. An adaptive self-biased amplifier topology [16] has been proposed. An OTA has been designed (Fig. 4) with the constraints of matching all the PMOS (M3, M4, M5) to the PMOS (M1, M2), so that the current biasing of the amplifier is a fraction of the load currents. Following the guidelines of [16], a ratio of 2 between M6 and M7 in order to maximize the gm/id and acheive a very high DC that almost zeros the input impedence (virtual ground), enabling $V_{\text{Ring}} = V_{Res}$. Any supply dependant offset voltage variation between the amplifier inputs is hence minimized. In order to reduce the start-up time, a start-up circuitry is introduced in order to trigger the positive feedback and suppressed it once the circuit is self-biased. Bias Ripple is mitigated by inserting capacitance at the gate of M8 and M9 (Cripfilt1, Cripfilt2).

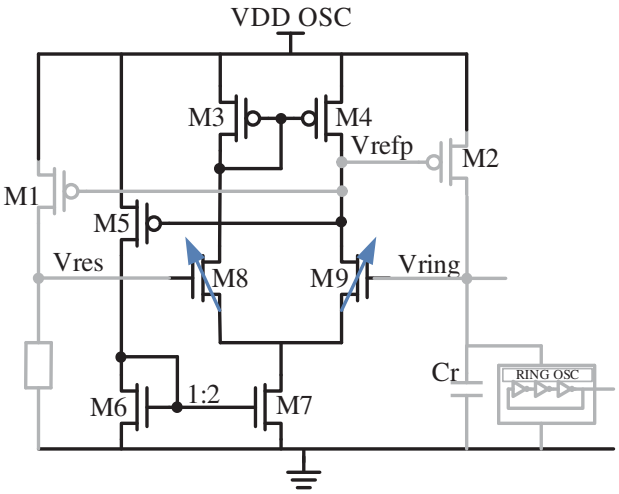

Fig. 4. Self biased OTA simplified schematic

IV. Measurement Results

The proposed nA range oscillator is implemented in 180nm CMOS (Fig. 5).

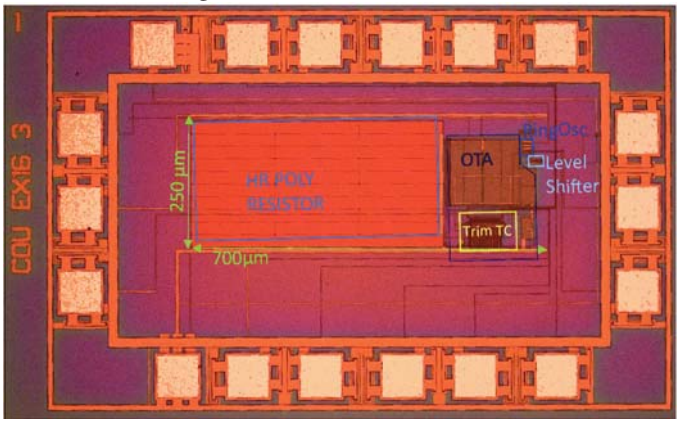

Fig. 5. Die photo of the oscillator in 0.18µm CMOS

This oscillator has been characterized with respect to supply variation and temperature variation, we assessed the core consumption and frequency. We assessed frequency stability by measuring jitter according to JDEC standard JESD65B. Measurements results are discussed in the next sections:

A. Temperature frequency Calibration

In order to demonstrate the effective temperature calibration discussed in Section III, each trimming code was swept over temperature. It is presented (Fig. 6) the typical behaviour without any imbalance as the bold line. The maximum imbalance of the transistor M9 with respect to M8 in red and the maximum imbalance of the transistor M8 with respect to M9 in purple. It was applied in accordance to (10): ±80mV offset to the middle range of M9 with respect to M8. The different measurement results are presented following this convention.

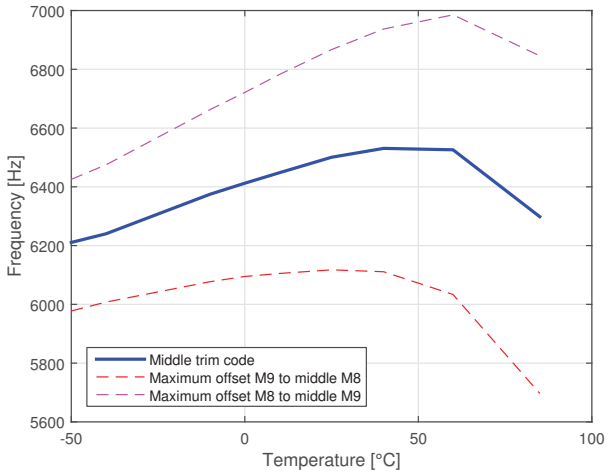

Fig. 6. Frequency stability in commercial temperature temperature range

The calibrated imbalance has been selected as seven additional unity area of the differential pair in order to get that temperature coefficient. The thermal coefficient is extracted as ±7ppm/°C in the temperature defined in usual human wearable electronics of [-40°C - 85°C]. A more exact formulation of that coefficient would be a second order polynomial function as the curve shape is parabola.

$$F(T) = -0.0484T^2 + 3.0314\,T + 6446.5 \qquad (11)$$

The derivative of the above (11) got two extremum as well-being lower than ±7ppm/°C

B. *Supply line frequency dependancy*

This oscillator has a dependency of 710 ppm/V over the operating range 0.8V-1.8V (Fig. 7).

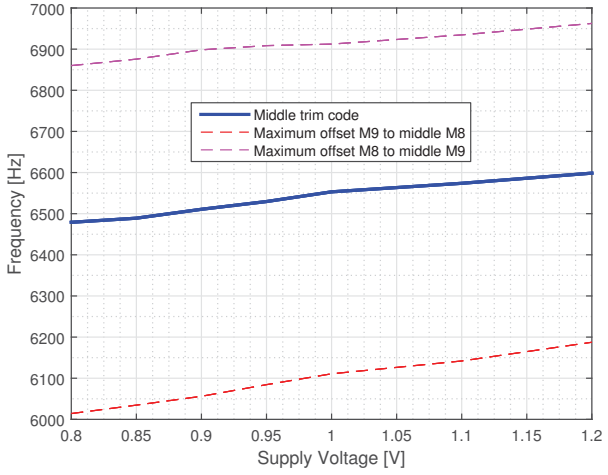

Fig. 7. Frequency sensitivity to power supply

C. *Current consumption*

This oscillator has shown a nA level operation in all its current branch over 0.4V voltage range and 135°C range (Fig. 8 and Fig. 9).

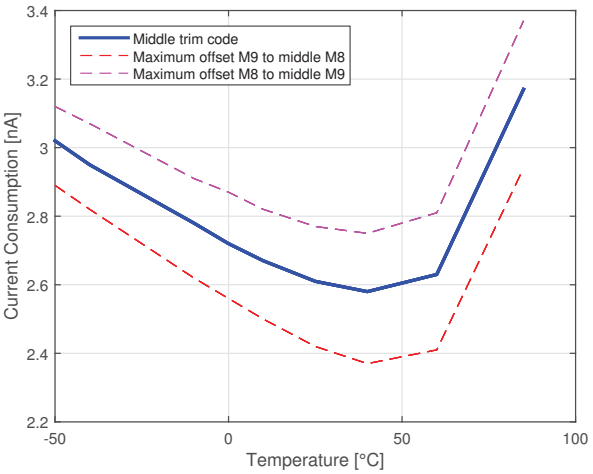

Fig. 8. Current consumption temperature sensitivity

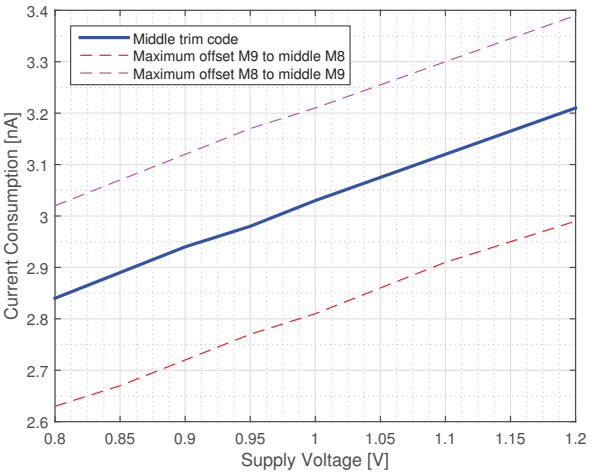

Fig. 9. Current consumption supply sensitivity

D. *Jitter*

Jitter measurement were performed using a universal frequency Counter, with 12 digits/s and 20 ps resolution. The JDEC standard JESD65B suggest the following definition (Fig. 10):

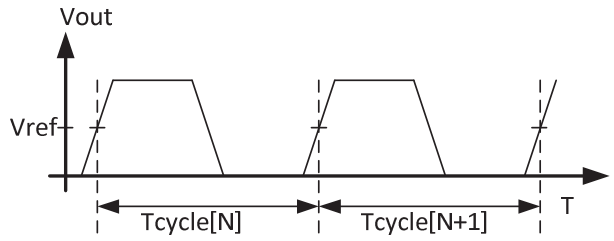

Fig. 10. Output signal

It's measured every interval time or frequency, it is recommended to take a large number of samples and more precisely suggested to take 10'000 cycle as a reasonable sample size. It was accordingly measure every interval between rising edges, and it was logged 10'000 measures

these measure being already the results of several measurements. (Fig. 11). Then it was decided to post-process as period jitter as the measure was intended to measure a long term accuracy. A second reference would not deviate more than 12 PPM correspond to one second per day. A minute reference would not exceed 720 PPM *et cetera*.

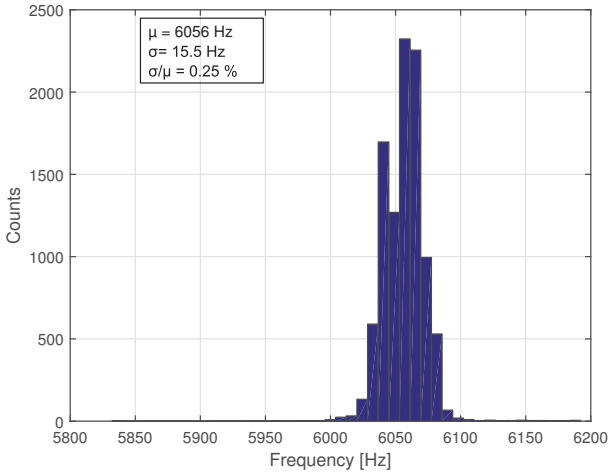

Fig. 11. Jitter measurements according to JDEC standard JESD65B

The measured deviation is 2500 PPM accordingly this reference could not be itself more accurate than 4 minute a day, 2 hour a month *et cetera*. In the case of an IoT sensor time stamp it would fit into most of the state of the art appliances especially IoT nodes including time synchronisation with the network.

V. Figure of Merit and Benchmark

A lot of attempts have been reported, to compare oscillators efficiency such as the frequency over consumption figure of merit which is similar to the power delay introduced for digital gates [17] FOM1. Some more recent concern includes area[18] FOM3, is defined as FoM1·Area/L_{min} ^{2}, where L_{min} is the minimum gate length of the process technology. And finally the IoT thrust, to consider every SoC building bloc consumption as an energy per operation [19] FOM2 presented in Fig. 12.

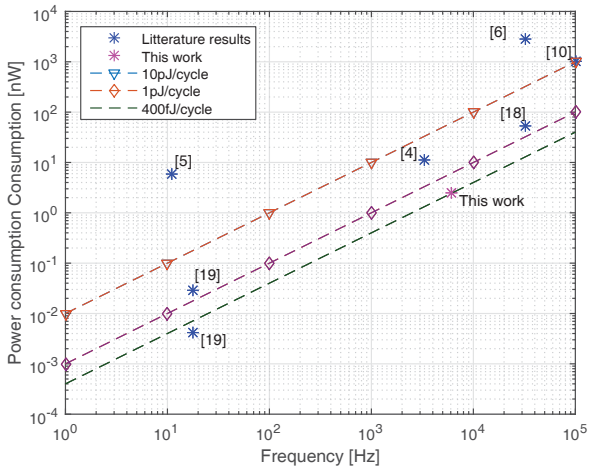

Fig. 12. Figure of merit 1 and 2

This L_{min} work shows a promising figure of merit in the IoT era with 400fJ/cycle end to end with no need for external calibration logic or compensation bloc the temperature trimming could be evaluated in qualification and be applied on the lot level. Power consumption is not the only concern, the following TABLE1 presents a benchmark of the state of the art solution and this work:

TABLE I.
BENCHMARK

Parameter		*This work*	[10]	[5]	[6]
Process [nm]		180	130	180	60
Area [mm^2]		0.175	-	0.24	0.048
Frequency [Hz]		6 050	100 000	11	32 728
T° range [°C]		-40 to 85	20 to 70	-10 to 90	-20 to 100
T° Coefficient [ppm/°C]		14	40	45	32.4
Line sensitivity [ppm/V]		710	-	10 000	35 000
Power [nW]	Un-comp	2,5	100	5.8	2800
	Comp	2,5	1000	5.8	2800
	Average	2,5	150	5.8	2800
Temperature compensation		1st order	yes	yes	yes
Principle		CCO	CCO	Relaxation	Relaxation
FOM1 : $\left[\frac{\mu A}{MHz}\right]$		0,4	1,5	527	85.5
FOM2 : $\left[\frac{fJ}{cycle}\right]$		400	1 500	527 000	8 550
FOM3 : $\left[\frac{\mu A}{MHz}\blacksquare\right] \times 10^6$		2.26	-	3903	1141

VI. Conclusion

This work presents an oscillator that can be used in compact wireless sensors. It describes a novel compensation strategy for thermal behaviour of an RC oscillator that could replace power hungry solutions with a reasonable die-size. As with every work on oscillators, the target frequency is always part of the biased comparison and the reason to insert a Figure of merit expressed in µA/MHz which give an indication of the spent power for a given activity as used with MCU.

Acknowledgment

This work has been sponsored by EM Microelectronic-Marin SA under TULP project.

References

[1] D. Lanfranchi, E. Dijkstra, and D. Aebischer, "A microprocessor-based analog wristwatch chip with 3 seconds/year accuracy," in *Proceedings of IEEE International Solid-State Circuits Conference - ISSCC '94*, 1990, vol. 23, no. 3, pp. 92–93.

[2] E. a. Vittoz, M. G. R. Degrauwe, and S. Bitz, "High-Performance Crystal Oscillator Circuits: Theory and Application.," *IEEE J. Solid-State Circuits*, vol. 23, no. 3, pp. 774–783, 1987.

[3] H. G. Barrow, T. L. Naing, R. a. Schneider, T. O. Rocheleau, V. Yeh, Z. Ren, and C. T. C. Nguyen, "A real-time 32.768-kHz clock oscillator using a 0.0154-mm 2 micromechanical resonator frequency-setting element," *2012 IEEE Int. Freq. Control Symp. IFCS 2012, Proc.*, pp. 277–282, 2012.

[4] U. Denier, "Analysis and design of an ultralow-power CMOS relaxation oscillator," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 57, no. 8, pp. 1973–1982, 2010.

[5] S. Jeong, I. Lee, D. Blaauw, and D. Sylvester, "Timer Using a Constant Charge Subtraction Scheme," pp. 3–6, 2014.

[6] K. J. Hsiao, "A 32.4 ppm/°C 3.2-1.6V self-chopped relaxation oscillator with adaptive supply generation" *IEEE Symp. VLSI Circuits, Dig. Tech. Pap.*, no. 1, pp. 14–15, 2012.

[7] M. Grözing and M. Berroth, "Reduction of CMOS Inverter Ring Oscillator Close-In Phase Noise by Current Mode Instead of Voltage Mode Supply" pp. 97–100, 2006.

[8] P. Nugroho, E. Leelarasmee, and N. Fujii"Tuning Analysis of a CMOS Current Controlled Ring Oscillator," pp. 49–52, 2006.

[9] K. Sundaresan, P. E. Allen, and F. Ayazi, "Process and temperature compensation in a 7-MHz CMOS clock oscillator," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 433–441, 2006.

[10] A. Shrivastava and B. H. Calhoun, "A 150nW, 5ppm/??C, 100kHz on-chip clock source for ultra low power SoCs," *Proc. Cust. Integr. Circuits Conf.*, pp. 12–15, 2012.

[11] D. Ruffieux, F. Krummenacher, A. Pezous, and G. Spinola-Durante, "Silicon resonator based 3.2 µw real time clock with ±10 ppm frequency accuracy," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 224–234, 2010.

[12] R. Schober, I. Opris, F. Krummenacher, "HIGH SENSITIVITY RFID TAG INTEGRATED CIRCUITS," WO/2007/014053, 2007.

[13] S. Docking and M. Sachdev, "A method to derive an equation for the oscillation frequency of a ring oscillator," *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.*, vol. 50, no. 2, pp. 259–264, Feb. 2003.

[14] U. Guler and G. Dundar, "Modeling phase noise and jitter in subthreshold region and assessing the randomness performance of CMOS ring oscillators," in *2012 International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, 2012, vol. 0, no. 3, pp. 257–260.

[15] R. M. Swanson and J. D. Meindl, "Ion implanted CMOS transistors in low voltage circuits," *Jssc*, no. 2, pp. 1–8, 1999.

[16] M. G. Degrauwe, J. Rijmenants, E. A. Vittoz, and H. J. De Man, "Adaptive biasing CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 17, no. 3, pp. 522–528, 1982.

[17] R. Muller, H.-J. Pfleiderer, and K.-U. Stein, "Energy per logic operation in integrated circuits: definition and determination," *IEEE J. Solid-State Circuits*, vol. 11, no. 5, pp. 657–661, Oct. 1976.

[18] H. Asano, T. Hirose, K. Tsubaki, T. Miyoshi, T. Ozaki, N. Kuroki, and M. Numa, "A 1.66-nW/kHz, 32.7-kHz, 99.5ppm/°C fully integrated current-mode RC oscillator for real-time clock applications with PVT stability," in *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, 2016, vol. 2, pp. 149–152.

[19] P. M. Nadeau, A. Paidimarri, and A. P. Chandrakasan, "Ultra Low-Energy Relaxation Oscillator With 230 fJ/cycle Efficiency," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 789–799, 2016.

[20] A. Shrivastava and B. H. Calhoun, "A 150nW, 5ppm/??C, 100kHz on-chip clock source for ultra low power SoCs," in *Proceedings of the Custom Integrated Circuits Conference*, 2012, pp. 12–15.

Mathieu Coustans received the M.S. degree in Electrical Engineering from INPT-ENSEEIHT in 2014. He is currently with the Electronics Laboratory, Swiss Federal Institute of Technology (EPFL). He is currently working towards the PhD degree and his work focuses on Ultra Low Power / energy-efficient Integrated Circuit. His research interests include device reliability and modelling, CMOS analog and mixed-signal energy-efficient circuits design.

François Krummenacher born in Lausanne, Switzerland, in 1955. He received the M.S. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1979 and 1985, respectively. Since 1979, he has been with the Electronics Laboratory, EPFL, where he is currently engaged in research on low-power analog and mixed analog/digital CMOS integrated circuit (IC) design, as well as in deep sub micrometer and high-voltage MOSFET device compact modeling. He is the author or a coauthor of more than 100 scientific publications in these fields. Since 1989, he has also been an Independent Consultant, providing scientific and technical expertise in IC design to numerous local and international industries and research labs

Maher Kayal received M.S. and Ph.D degrees in electrical engineering from the Ecole Polytechnique Fédérale de Lausanne (EPFL, Switzerland) in 1983 and 1989 respectively. He has been with the Electronics laboratories of the Ecole Polytechnique Fédérale de Lausanne (EPFL, Switzerland) since 1990, where he is currently a professor and director of the "Energy Management and Sustainability" section. He has published many scientific papers, coauthor of three text books dedicated to mixed-mode CMOS design and he holds 10 patents. His technical contributions have been in the area of analog and Mixed-signal circuits design including highly linear and tunable sensors microsystems, signal processing and green energy management.

Christian Terrier received the M.S. degrees in electrical engineering from the Conservatoire National des Arts et Métiers (France) in 1974. From 1974-1980, He was at CEA–Leti in the Applied Microelectronic Laboratory. Involved in the fundamentals of MOS analog design of the 70's. He was with EFCIS (now ST Microelectronics) from 1980 to 1986, in the R&D Department. In 1982, he became the technical leader of the Analog Processing Group. He was with Thomson Composants Specifiques From 1986 to 1994, (now E2V). Until end 2010, he was the Technical Design Manager of EM EM Microelectronic-Marin SA and now acting as Technical Expert.