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SIMULATION STUDIES OF PARTIAL PARALLEL ISOLATED DC/DC BOOST CONVERTER

The renewable energy sources or energy storage devices deliver output voltage at the range of around 12 V_{DC} to 48 V_{DC}. In order to obtain at least 350 V_{DC} needed for direct to alternating current conversion the DC/DC power converter should demonstrate significant voltage gain and power conversion efficiency as high as possible. To obtain such level of output voltage at low input voltages transistors of the boost converter must operate with high currents. High efficiency and high voltage gain can be achieved with parallel combination of two or more isolated step-up converters. The converters operate synchronously and in phase, using the same control signals. Balancing transformers are used to ensure the synchronization and equal distribution of current between the power levels. They provide equal distribution of significant input current to a number of smaller current loops. This feature alongside with the use of power MOSFETs with low channel resistance and silicon carbide (SiC) Schottky diodes will reduce losses within the converter and increase the efficiency of entire energy conversion system. This paper presents PSpice simulation results of partial parallel isolated DC/DC boost converter with voltage doubler. In presented circuit high voltage gain and high conversion efficiency were achieved.

1. INTRODUCTION

It is commonly believed that in low input voltage applications achieving significant voltage gain requires high transformer turns ratio which complicate transformer design. Partial paralleling of two or more isolated converters [1]-[3] results in a reduction of the turns ratio, as well as energy losses in power switches. The proposed converter is characterized by high efficiency and high voltage gain and thanks to parallel structure the isolation transformer turns ratio can be reduced by half. The usage of balancing transformers allows even distribution of input current among all of the converter transistors. As the input voltage is in the range of tens of volts transistors with a low drain-source resistance can be applied to the structure.

The simulation model of presented converter incorporates some properties and essential features of the magnetic components very often neglected in this type of research. Models of power transistors and diodes used comes from the manufacturer's websites [4],[5].

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2. PARTIAL PARALLEL ISOLATED DC/DC BOOST CONVERTER TOPOLOGY

2.1. Electrical scheme

Partial parallel isolated DC/DC boost converter with voltage doubler is depicted in Fig. 1a. High input current i_{in} is divided equally into two smaller currents i_{L1},i_{L2}. Balancing transformers *T1*,*T2* split currents flowing through the input inductors *L1*,*L2*. As a result both transistors pairs (*S1*,*S4* or *S2*,*S3*) of the converter conduct only half input current. When the current i_{L1} is rising the current i_{L2} is falling, except the overlap time (S1,S2,S3,S4 in conduction state) when they are both rising. Both parallel connected half-bridges form first section of voltage step-up. Transformers *T3* and *T4* assure galvanic isolation between two power stages. The output diode rectifier (*D1*,*D2*) with capacitors (*C1*,*C2*) double rectified AC voltage of serial connected secondary T3 and T4 transformer windings.

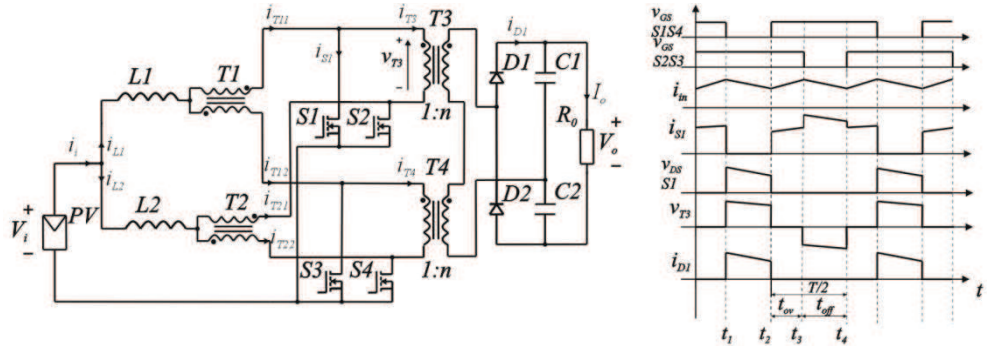

Fig. 1. a) Partial parallel isolated DC/DC boost converter with voltage doubler, b) typical waveforms

2.2. Principle of operation

The converter operation principle can be divided into several time intervals in which all transistors are driven at the same time (t_{ov}) or in pairs S1,S4 and S2,S3 (t_{off}) (Fig. 1b). The sum of all transistor drive time and drive time of transistor pair is equal to half of the period.

$$T = 2(t_{ov} + t_{off}) \tag{1}$$

The *d*, determines the overlap ratio.

$$d = \frac{2t_{ov}}{T} \tag{2}$$

Voltage transfer function of the converter is equal

$$B = \frac{V_o}{V_i} = \frac{4n}{1-D} \tag{3}$$

where duty cycle is

$$D = d + \frac{t_{off}}{T} = \frac{(2t_{ov} + t_{off})}{T} \tag{4}$$

For high-power converters working with constant low-voltage DC source, conduction losses in transistors dominate due to high input currents. They increase with drain to source transistor resistance increase and duty cycle.

3. PSPICE SIMULATION MODEL OF PARTIAL PARALLEL ISOLATED DC/DC BOOST CONVERTER

Partial parallel isolated DC/DC converter model (Fig. 2) is supplied from constant DC source V_{in} = 30 V. Balancing transformers TX1 and TX2 provide equal distribution of input current. The TX3 and TX4 transformers are ensuring galvanic isolation. Since the transformers turns ratio is n = 1:2 and secondary winding of both isolation transformers are connected in series - converter output voltage is multiplied by 2. Output AC voltage of the transformer is rectified by diode half-bridge. Voltage doubler output capacitors C_1 and C_2 (10 μF both) provide third stage of voltage step-up. Output voltage V_o changes as a function of load resistance R_o, overshoot ratio d and operation frequency *f*.

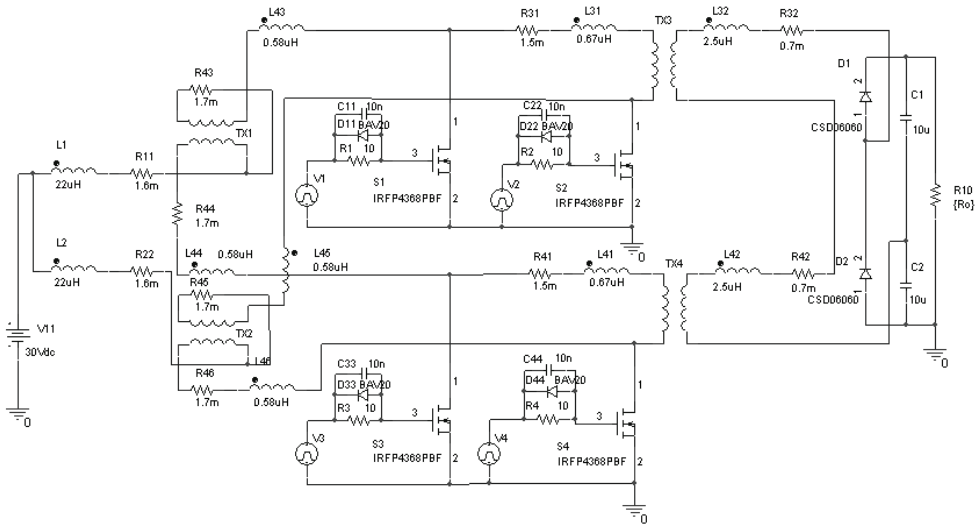

Fig. 2. Pspice model of DC-DC full bridge converter with voltage doubler

Optimal configuration for transistor gate driving was proposed in order to improve the quality of transistor switching. The BAV20 Schottky diode accelerate turning off of the transistor, 10 nF capacitor and 10 Ω resistance all in parallel form the gate circuit at each transistor gate.

3.1. Semiconductors

The partial parallel converter's half-bridges are realized on the low drain to source resistance MOSFET transistors - IRFP4368 ($R_{DS(on)}$=1.46 mΩ) [4]. Drain to source resistance varied between several mili-Ohms significantly reduces conduction losses of the transistors. As the energy losses increase with the current square. In output rectifier simulation models of silicon carbide (SiC) - CSD06060 Schottky diodes were used. SiC diode is characterized by a negligible reverse recovery time - less then 1 ns, which for Si diode is 18 ns (for similar voltage/current rating). Nevertheless, the SiC diode has one disadvantage which is 0.2 V higher forward voltage drop. What will increase the conduction losses in the diode half bridge stage.

3.2. Magnetic Components

In order to create possibly precise PSpice model of the isolation transformers and inductors were designed, manufactured and examined. Listed below are specified parameters provided by the manufacturer and measured with MT4090 RLC meter.It should be noted that the inductance values may vary slightly as a function of frequency. Inductance values included in the simulation model were measured at 10 kHz frequency. Inductors L1,L2 ensure continuity of the current delivered to the load. Measured values of inductance and resistance for fixed frequency f = 20 kHz were equal 22 μH and 1.6 mΩ.

Balancing transformers TX1 TX2 turns ratio *n* is 1:1.Since windings were made of Litz wire with equal cross section and number of turns was the same – parasitic parameters of the both sides will not differ. Measured values of windings resistances are equal 1.7 mΩ. Leakage inductances were equal 0.58 μH. Isolation transformers TX3 TX4 turns ratio *n* is 1:2. Measured values of primary and secondary windings resistances are equal 1.5 mΩ and 0.7 mΩ respectively. Leakage inductances of both sides of transformer were equal 0.67 μH primary and 2.5 μH secondary respectively. Abovementioned parasitic parameters were included in transformers and input inductors simulation model.

4. SIMULATION RESULTS

For fixed frequency 20 kHz ,overshoot ratio of d = 0.1 and load resistance R_o=100 Ω switching transient waveforms are presented on Fig. 3.

Switching nature of the transistor currents and voltages is associated with the control strategy. The maximum current of each transistor is equal to half of the input current and during the overshoot, transistor current is reduced by a half since the input inductor L1 (L2) current $i_{l1(l2)}$ flows through both half-bridge converter branches.

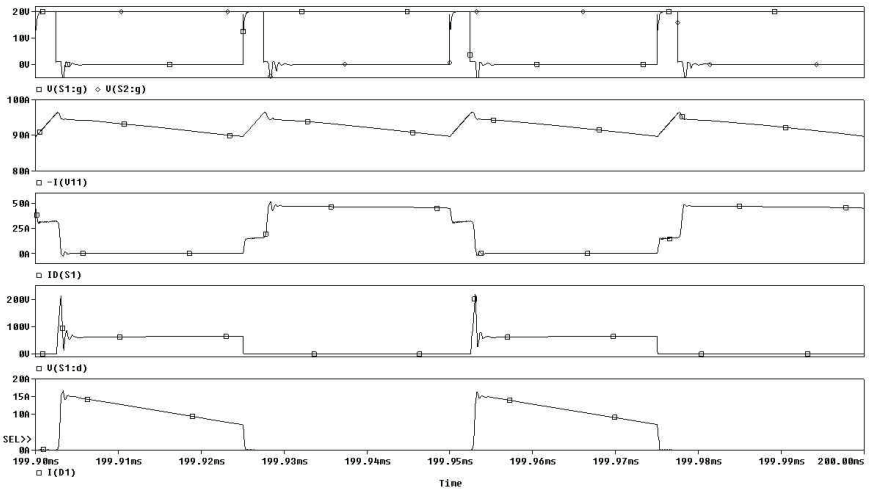

Fig. 3. Transient characteristics of serial parallel DC/DC boost converter; driving voltages of transistors S1, S2- V(S1:g),V(S2:g); transistor S1 current ID(S1); transistor S1drain to source voltage V(S1:d) and output diode D1 current I(D1)

Voltage overshoots are related to transistor parasitic capacitance and leakage inductance of the primary side of the transformer. It has negative effect on overall system efficiency enlarging the transistor power losses (Fig. 4).

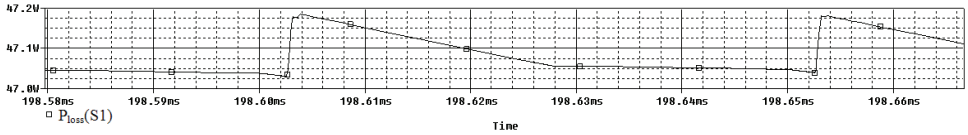

Fig. 4. Transient characteristics of transistor S1 power losses

At input power of 2.4 kW turn-off losses of the transistor that are equal 4.76 W. For comparison, the turn-on losses are 2.18 W. Conduction losses are approximately equal to the average value of total losses that is 47 Watts.

Electrical characteristics were plotted as a function of key parameters (efficiency η, voltage gain B and input current i_i) of the converter as a function of the frequency for fixed output resistance R_o=100 Ω and overshoot ratio d = 0.1 (Fig. 5).

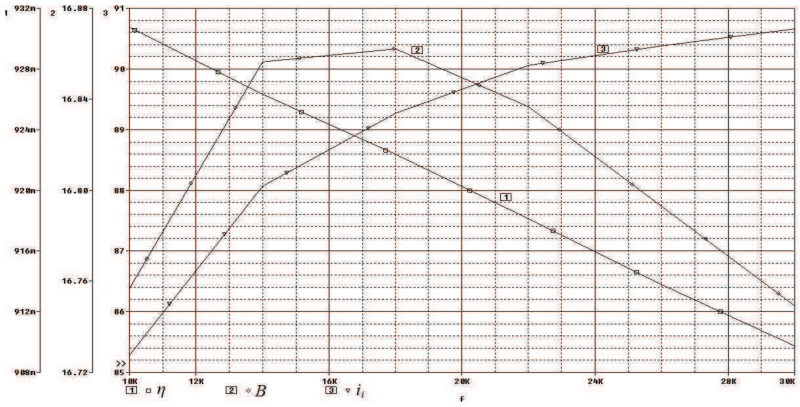

Fig. 5. Efficiency η, voltage gain B and input current i_i as a function of the frequency for fixed output resistance R_o=100 Ω and overshoot ratio d=0.1

The output power varied from 2380 to 2550 watts within 10÷30 kHz frequency range. The highest efficiency achieved was 93% for input current 85.28 A and voltage gain of 16.75 V for 10 kHz operation frequency. As the voltage gain has changed of 0.5 percent across the frequency range, we can assume that it is constant as a function of frequency. The highest voltage gain were achieved for 18 kHz frequency at 89 A of input current and efficiency of 92.24%. That is a satisfactory result for the step-up converter with power range above 2 kW and hard switched semiconductor switches . Efficiency η has decreasing nature in function of frequency. With frequency increase the participation of switching losses grow. It is worth noting that the output voltage was over 500 volt over the whole frequency range.

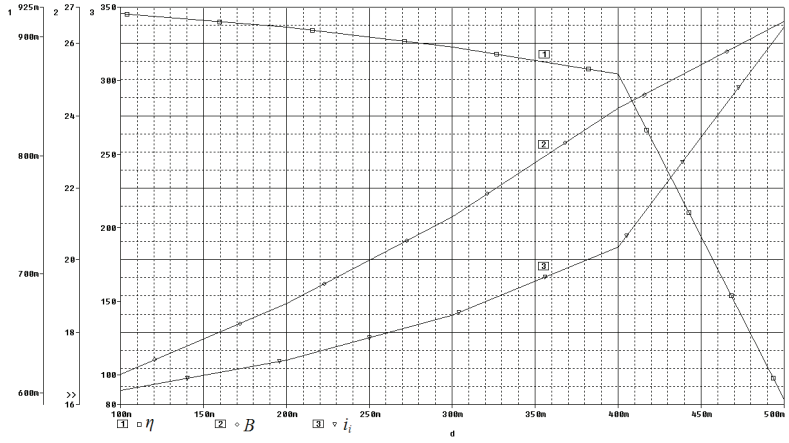

Fig. 6. Efficiency η, voltage gain B and input current i_i as a function of the frequency for fixed output resistance R_o = 100 Ω and frequency f = 0.1

Output voltages varied from 594 to 798 V for 0.1÷0.5 overshoot ratio (d) range (Fig. 6) so that voltage gain over 26 V could be achieved. Unfortunately, such a large value goes along with lower efficiency 86.8 % (d = 0.4, B = 24.2). The highest efficiency achieved was 90.8 for d = 0.1. Above d = 0.4 the converter efficiency rapidly decreases to values below 60% (59.4%). Such large values of output voltages, and thus work with the overshoot ratio d above 0.4 (duty cycle D = 0.7 and more) is rarely useful technically. Characteristics of both converter parameters (B, i_i) have increasing nature in function of overshoot ratio (d) – the longer t_{ov} time the greater amount of energy is accumulated in the input inductors L1 and L2 consequently greater is voltage step-up and input current.

6. CONCLUSION

The proper choice of semiconductor devices and serial paralleling of the two half-bridge step-up converters assured very high voltage gain (26.6 V) and a satisfactory efficiency (above 90%) in a wide range of processed power (from 2.4 to almost 3.3 kW). Maximum efficiency of the converter was 93%. It can be seen that it is not necessary to work with high duty cycle (D) in order to achieve efficiency above 90% with a high voltage gain. The resulting maximum power output of the inverter was almost 6 kW. Obtained in the course of the simulation results confirm the suitability of the serial parallel converter to work with low voltage energy sources. Since the PSpice model does not fully reflect the actual parameters of real circuit it is expected that the results of laboratory tests may vary slightly.

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[5] http://www.cree.com/ - CSD06060 datasheet, spice model

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