QRS detector, Field Programmable Analog Array,
baseline drift, cardiac assist device,
artificial stimulator, pacemaker

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REAL TIME QRS DETECTOR BASED ON FIELD PROGRAMMABLE ANALOG ARRAY

In some applications it is important to detect the QRS complex in the ECG waveform with possibly low time delay. Traditional software detectors of the QRS complex implement algorithms usually based on cascades of digital filters that introduce delays up to parts of a second. On the other hand, hardware QRS detectors fulfil the low delay requirements, but have worse adaptive features for the changing ECG shape. In this paper a new approach to QRS detection is presented. The proposed detector is based on a Field Programmable Analog Array (FPAA). This solution makes it possible to modify the parameters of particular blocks of the detector or even the whole structure without any changes in hardware, while the processing path is fully analog and does not introduce an additional delay. The most interesting feature of the FPAA is the dynamic reconfigurability. The parameters can be changed during runtime without any reset of the circuit or any other disturbances of the system functionality. The prototype QRS detector was built using the AN221E04 circuit from the Anadigm company.

1. INTRODUCTION

In some medical devices, such as cardiac assist devices, artificial heart chambers, defibrillators or pacemakers, the device should be synchronized with the proper phase of a cardiac cycle. Usually, to fulfil this requirement, the QRS complexes should be detected with a small delay, for example for artificial heart chambers - less than 50 ms. Standard software detectors [2] use digital filters that may introduce significant time delay up to parts of a second. Hardware analog detectors allow to avoid this disadvantage.

2. STRUCTURE OF A CLASSICAL HARDWARE QRS DETECTOR

A classical hardware QRS detector contains several analog blocks like amplifiers, filters, peak detectors and comparators [1]. In typical applications these blocks are built using operational amplifiers (OA). Each of them requires one or two OAs and several additional components – resistors, capacitors or diodes. Such a structure fulfils the requirements but any changes of the parameters are rather difficult – tuning of the parameters requires changes in hardware (e.g. potentiometer settings). Field Programmable Analog Array (FPAA) allows to solve this problem by means of software reconfiguration. The parameters and other settings can be changed on-the-run during normal operation of the device. A block diagram of a classical analog QRS detector is shown in Fig. 1.

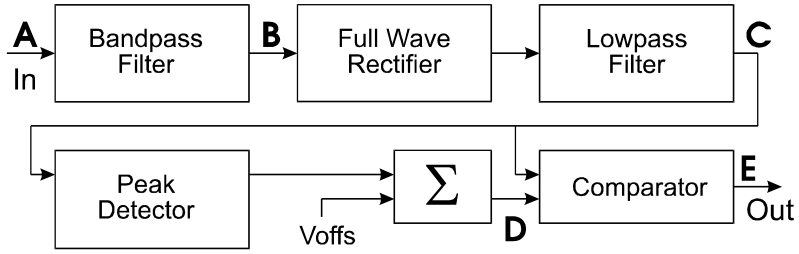

Fig. 1. Classical hardware QRS detector – block diagram [1]

The bandpass filter is tuned to the most significant spectral components of the QRS complex. Its task is to eliminate the baseline fluctuation and reduce the high frequency noise. The rectifier with a lowpass filter creates unipolar response regardless of the input signal polarity. The peak detector holds the maximum peak voltage. Its output voltage decreases with the preset decay time constant and is used for the comparator threshold setting. The comparator gives the pulse on its output when the actual peak value crosses the threshold. The waveforms in particular nodes of the detector are shown in Fig. 2.

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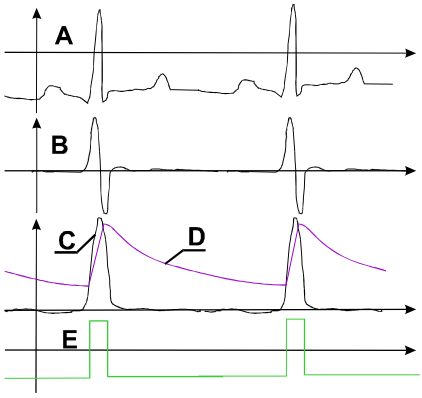

Fig. 2. Waveforms in important nodes of the hardware QRS detector

3. QRS DETECTOR IMPLEMENTATION IN FPAA

The main idea of our work is to implement the QRS detector structure in a programmable device. Field Programmable Analog Arrays (FPAA) give the constructors new possibilities in analog circuits design. There are several vendors of the FPAA circuits that offer different amounts of resources and principles of operation. This research work is based on the AN221E04 circuit from the Anadigm company [5, 6]. The circuit operates on the switched capacitor (SC) principle. It contains 8 operational amplifiers, 4 voltage comparators and a network of digitally controlled switches and capacitors. There are also additional resources like SAR AD converters, look-up table and others. The configuration for the AN221E04 device can be created and downloaded to the device using an easy to use “drag-and-drop” CAD tool named AnadigmDesigner®2 available on the Anadigm homepage. AN221E04 can be reconfigured dynamically (“on the run”). The microcontroller connected to the AN221E04 device can calculate new component values and load the new configuration data to the device still working in its previous configuration. The configuration data can then be swapped in a single clock cycle.

3.1. ANALOG PART

The resources available in the AN221E04 device are sufficient to implement nearly all blocks that are used in a hardware analog QRS detector. The block diagram of the QRS detector implemented in FPAA generally corresponds to the basic structure shown in Fig. 1. The implementation created in AnadigmDesigner®2 is presented in Fig. 3 (AnadigmDesigner®2 screenshot).

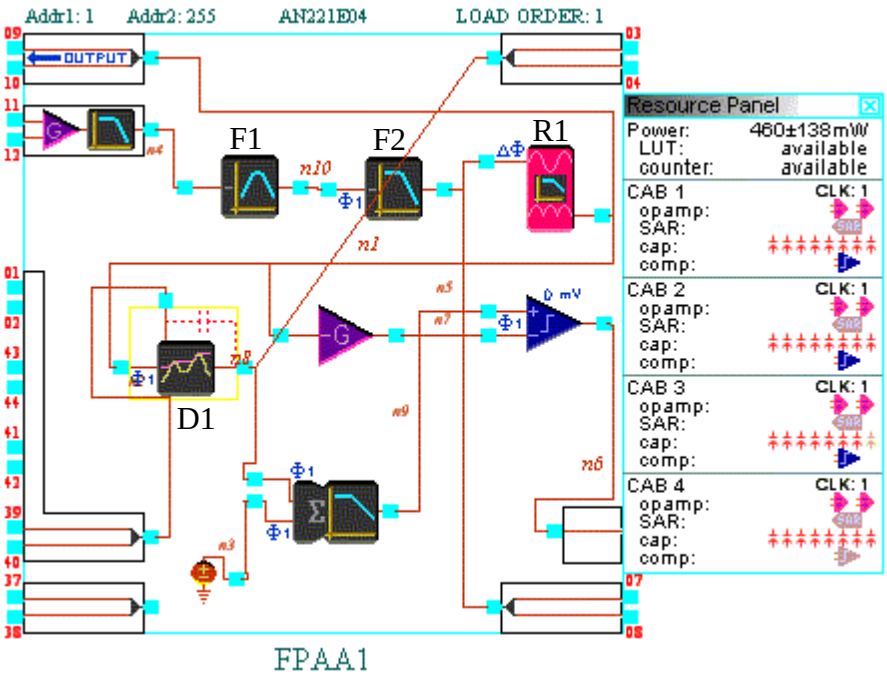

Fig. 3. The schematic of the QRS detector

The initially amplified signal is applied to the input cell (pins 11 and 12) comprising an amplifier and an antialiasing filter. Then specific filtering is applied to the signal by SC filters F1 & F2. The band-pass filter with centre frequency of 16Hz (F1) is used to eliminate baseline drift and to separate QRS components from the input signal. Additionally, a second-order low-pass filter with cut-off frequency of 20Hz (F2) reduces high frequency components. A full-wave rectifier (R1) with a smoothing filter is the next block of the QRS detector. The rectified signal is supplied to a peak detector (D1) with a programmable output voltage slew rate and a falling output signal time constant. Small offset voltage is added to the detector output voltage to enhance detector's immunity to noise. When the rectifier output voltage exceeds the voltage value held in the peak detector, the comparator generates a pulse indicating that the QRS complex is detected. The comparator output waveform can be standardized to a constant width pulses by a simple monostable multivibrator or a microcontroller outside the FPAA.

The Anadigm AN221K04 Development Board Kit [7] was used for implementation of the prototype detector circuit. Apart from FPAA, the development board comprises input and output buffering amplifiers (level translators) and a microcontroller PIC used to transfer configuration data from a PC computer to the array. The development board is designed in such a way that it is easy to reconfigure the conditioning amplifiers, connect additional devices and turn off not used hardware components.

Some limitations of the AN221K04 Development Board Kit cause problems that had to be solved during the design process. The details of these solutions are described in the following subparagraphs.

Clock signal frequency: All SC blocks of the analog array are clocked by signals obtained as a division of the standard clock signal applied to ACLK input. For the AN221K04 Development Board Kit the standard clock frequency is 16MHz. For the maximum division factor of 510 the obtained clock frequency is too high for the QRS detection purposes. Therefore an additional quartz oscillator with a frequency of 3 MHz was built. For the division factor of 480, this oscillator provides the clock signal frequency of 6,25 kHz. Such frequency is low enough to implement filters with corner frequencies required for QRS detection purpose.

Peak detector: The maximum output voltage decay time constant of a standard PeakDetect2 module is about 20ms, which is insufficient to achieve required parameters of the detector. Therefore the PeakDetectExt module (from an external library) was implemented in the QRS detector. Two external capacitors connected outside the circuit are necessary to ensure proper time constant. An important advantage of the applied module is the possibility of independent regulation of the peak slew rate and the decay time constant.

Offset voltage source: To enhance the noise immunity a small offset voltage was added to the exponential decay voltage at the output of the peak detector. There is no adjustable constant voltage source in the AN221E04 standard module library. Therefore a constant voltage source of 3V was applied to a summing amplifier input with the gain set to the minimum value of 0,011. That results in detector offset voltage of 33 mV.

3.2. DIGITAL PART

The digital part of the QRS detector is realized using the ADuC7020 microcontroller from Analog Devices. The processor core is based on ARM7 architecture. In the prototype version of the QRS detector only the basic tasks are handled by the software of the microprocessor. However, its resources allow to implement many more functions.

The microcontroller performs the following tasks:

- Downloading the primary configuration to the FPAA on reset via the SPI interface;
- Forming the standardized square pulses according to the signal received from the comparator;
- Measuring the RR intervals and sending the results to the host computer via RS323link.
- Preparing the reconfiguration data and downloading them to the FPAA in the dynamic reconfiguration mode on-the-run.

The program for the microcontroller is written in C language in the IAR Embedded Workbench environment from the IAR Systems AB [8]. Primary FPAA configuration and the reconfiguration data are created using the source files generated by AnadigmDesigner®2 software according to so called "algorithmic method". These files contain functions that allow to change parameters of any CAM block implemented in the FPAA. As an example there can be shown a function that changes the parameters of a second order bandpass filter. To change any parameter of this filter (or all of them together) one should call SetBQBandPassFilterII function. Its declaration part looks as follows:

```
void an_SetBQBandPassFilterII(an_CAM cam, double Fo, double G, double Q);
```

The function has the following parameters: an_CAM - id of the CAM module, Fo - center frequency in kilohertz, G - maximum gain and Q - the quality factor. The function body is written in ANSII C language, so any C compiler that implements the floating point arithmetic should compile it correctly and include it into a larger project. As a result, this function generates a string of the reconfiguration data that should be sent through the SPI link to the FPAA. AnadigmDesigner®2 generates similar functions for all blocks used in the project and also for configurable input and output cells. In the prototype solution the dynamic change of two parameters was tested: the gain of the full wave rectifier and the decay time constant of the peak detector.

4. EXPERIMENTAL RESULTS

4.1. TUNING THE DETECTOR

The parameters of particular blocks of the detector were tuned using the reference ECG waveform generated by the Arbitrary Generator DG2000 from Rigol. The settings were optimized for the proper detection of the QRS complexes of the amplitude range from $40mV_{p-p}$ up to $1V_{p-p}$. It gives the dynamic range for the noise-free ECG signal of about 28dB. Pulses with lower level are not always detected correctly, while for signals higher than the top limit there can be seen saturation effects. For the optimal operation the input conditioning amplifier should amplify the measured voltage level to about $200mV_{p-p}$.

4.2. QRS DETECTION VERIFICATION USING ECG SIGNALS FROM DATABASE

The source ECG signal was taken from the Physionet MIT-BIH Arrhythmia Database [3, 4]. As a generator of the test waveforms the PC analog I/O card PCI6221 from National Instruments was used. The I/O card was controlled by an application prepared in the LabVIEW [9] environment also from the National Instruments Corporation. The control panel of the virtual instrument is shown in Fig. 4.

The data sampled with the frequency of 360Hz are sent to the DAC registers. This virtual instrument allows to output the whole ECG data from the file or only a selected part of it. It is also possible to change the active channel on the fly, without reading the whole data to memory.

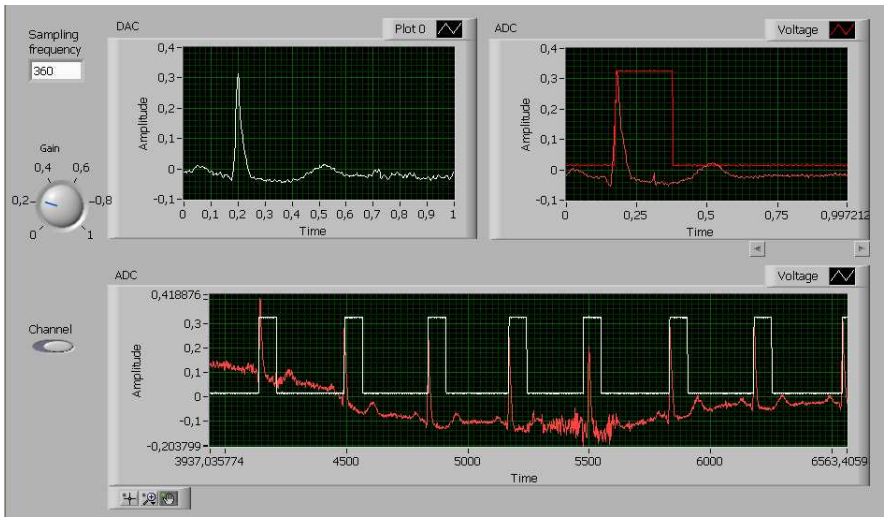

Fig. 4. Screenshot of the virtual instrument for ECG output and data acquisition

Analog to digital converter samples both the detector output signal and detector input signal. It is required for the synchronization and comparison of our detection results with the reference signal from the database. The block diagram of the test bench is shown in Fig. 5.

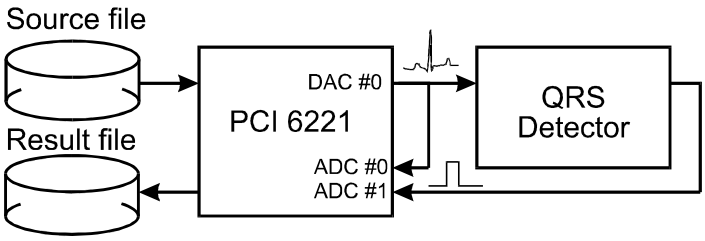

Fig. 5. Test workbench – block diagram

The final processing of the data was performed in an application prepared in the MatLab environment. Overall results are presented in table 1.

Table 1. Overall detection efficiency (results)

File Num. MIT-BIH database	Ref. QRS num.	Detect. QRS num.	Correct detections		Lost QRS (false negative)		Additional detections (false positive)		Premature detections (50–200ms before)	
100	2274	2271	2271	99.87%	3	0.13%	0	0.00%	0	0.00%
101	1874	1667	1659	88.53%	207	11.05%	2	0.11%	8	0.43%
102	2192	2189	2126	96.99%	5	0.23%	2	0.09%	60	2.74%
103	2091	2084	2083	99.62%	7	0.33%	1	0.05%	1	0.05%
112	2550	2543	2513	98.55%	9	0.35%	3	0.12%	28	1.10%
114	1890	1906	1872	99.05%	10	0.53%	26	1.38%	8	0.42%
115	1962	1953	1952	99.49%	6	0.31%	0	0.00%	4	0.20%
116	2421	2397	2361	97.52%	27	1.12%	3	0.12%	29	1.20%
118	2301	2313	2195	95.39%	21	0.91%	34	1.48%	86	3.74%
121	1876	1865	1839	98.03%	12	0.64%	3	0.16%	23	1.23%

The total time of the measurement data collected in our system is about 5 hours. It contains about 21 400 QRS complexes. If the detected point appeared within ±50 ms window around the reference point, the result was counted as a correct detection. If the reference peak was missed the result was counted as false negative, if there was no reference point around a detected point the result was counted as false positive.

4.3. EXAMPLES OF DETECTION RESULTS AND DISCUSSION

Some examples of the signals from database and detection results are presented in Fig. 6 and 7. One can see the raw ECG signal and the detector output. For better visualization on the ECG trace, reference detection (from annotation files) – stars, and detected points – squares, are added.

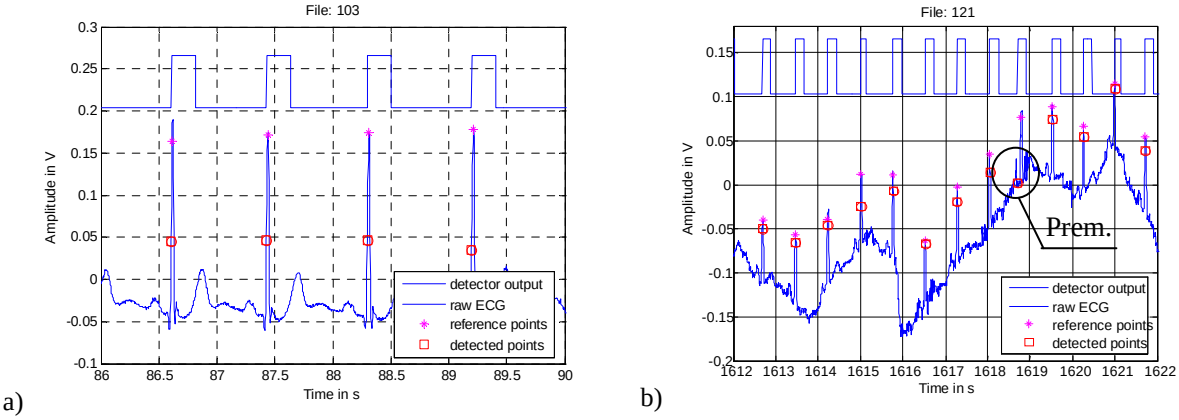

Fig. 6. Sample detection results: a) – high quality signal, b) – baseline drift

The detector works correctly during slow baseline drift, even when the changes are higher than the QRS amplitude – see Fig. 6b).

It should be noted that there is a relatively high number of false positive detections. Fig. 7a) and 7b) show pieces of the ECG signal incorrectly recognized as QRS complex.

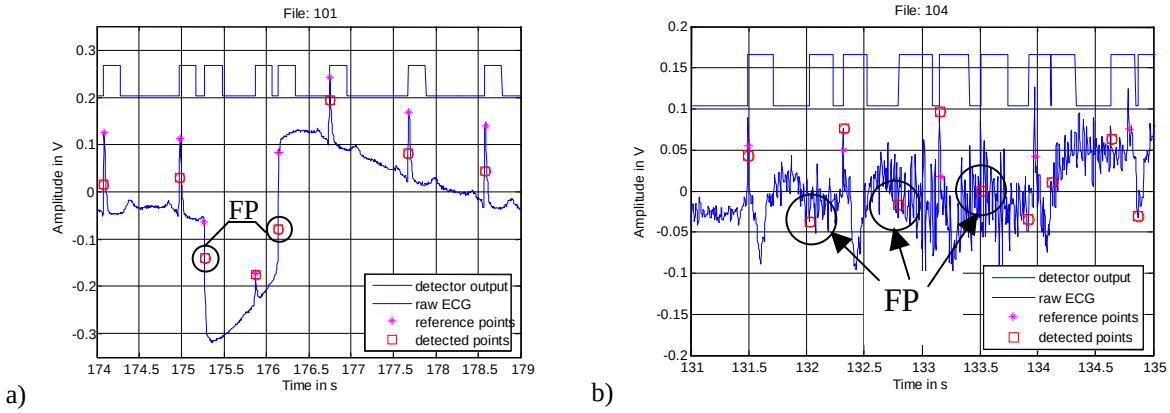

Fig. 7. Sample detection results: a) – baseline step change, b) – high frequency noise

In Fig. 7a) one can see a step change of the baseline that can be a result of any interference (eg. momentary disturbance of the electrode contact). Unfortunately, the step change of the input signal creates a pulse at the band-pass filter output, which is detected by the comparator as a normal QRS complex. There is no way to eliminate this problem in the analyzed analog structure. This disadvantage can be properly detected and eliminated offline in digital software detectors, however their results are always delayed against the input signal. There are applications where such a delay is unacceptable.

Another reason for false positive detection results was the high frequency noise – Fig. 7b). The wrong pulse appeared when noise voltage at the comparator input was equal to the exponentially decreasing voltage of the peak detector. This kind of errors could be reduced by the following methods: a) increase of the input filter attenuation for higher frequencies, b) increase of the comparison threshold in the comparator block, c) increase of the damping time constant in the peak detector.

Solution a) requires higher order input filters but in our circuit it is impossible while the hardware resources utilization is about 100%. The quality factor of the band pass filter can also be increased, but it would create oscillations in the filter output waveform and worsen the quality of the correct peaks detection. Solution b) leads to decrease of the circuit sensitivity and loss of the dynamic range. The c) approach would lead to a loss of small pulses that appear shortly after high pulses and the number of false negative detection would be greater. An optimum solution will have to utilize the dynamic reconfigurability of the Field Programmable Analog Array. An adaptive algorithm must be implemented in the microcontroller software. Realization of these ideas is a subject of future works in this area.

5. CONCLUSIONS

A new QRS detector structure has been built. The structure is based on a Field Programmable Analog Array AN221E04 form the Anadigm company. The processing path and the detection process is fully analog, which allows to avoid delays typical for most digital detectors. The results obtained in the prototype circuit show that the error rate of the QRS detection is low and can be accepted in most real time applications.

Dynamic reconfigurability of the FPAA gives us the possibility of building an adaptive QRS detector circuit as well as other adaptive analog circuits, which are very difficult to obtain in classic structures. Adaptive QRS detector is a subject of further research work.

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