Early Power Estimation of Mixed-Signal Design

Lukasz Kotynia, Muralikrishna Sathyamurthy, Felix Neumann, and Eckhard Hennig

***Abstract*—In this paper, we present the idea of using dynamic power estimation during the system-level design. A mixed-signal wireless IC with energy harvesting is used as an example of a device where power exploration and optimization plays a key role during the architecture planning. The novelty of this approach lies in introducing the activity profile for the mixed-signal chip as an important indicator of the power consumption that can drive the design phase. The method presented in this paper is based on modeling of the complete chip in order to apply it with a mixed-language Universal Verification Methodology (UVM) environment. It was decided to use the Verilog-D, SystemVerilog and Verilog-AMS languages to represent behavior of the digital and analog/mixed-signal parts of the chip..**

***Index Terms*—power profiling, Universal Verification Methodology, mixed-signal design**

I. Introduction

LOW power analyses and modeling techniques have become one of the major challenges with today's integrated circuit (IC) design. Still increasing complexity mixed-signal chips, comprising digital, analog and wireless blocks in a single die, fuels investigation of new ways of calculating expected power demands of chips long before tape-out.

Actual power demand of a chip is a function of number of factors including, but not limited to, technological process, loads, number of logic gates or supply voltage levels. However, with advent of more advanced low power techniques such as switching power domains, activity of internal nodes has become a key aspect in calculating the total power. Assuming constant toggling probability at the chip's inputs might not be sufficient for power estimation especially for wireless applications where peak power (current) consumption is critical. Obviously, getting a real-life activity data would require results from extensive functional simulations based on stimuli that mimic real-life device operation. These data are difficult to obtain employing only standard direct-testbench approach where numerous tests are exercised with input signals that are generated manually by verification engineers.

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This paper addresses the issue of power estimation at early design stage when physical implementation is not available. We investigate how expected peak power consumption can influence architecture and functionality of the design. With the proposed approach, the chip operation can be adjusted based on power estimation long before the actual transistor/gate implementation is completed. Information on peak power periods can be used to modify the control logic in order to stagger or postpone some operations in time. In our approach, the entire mixed-signal chip is modeled and simulated, thus the power estimate comes from both digital and analog/mixed-signal domains. The proposed method is based on commercially available tools from Cadence Design Systems. Consequently it can be easily applied with other mixed-signal as well as purely digital designs.

A passive Radio Frequency Identification (RFID)-based smart-sensor system is used in this paper in order to demonstrate the proposed power estimation methodology. The chip is an example of a project with digital and analog blocks which realize features like wireless communication and energy harvesting. The processor will be briefly described in section 3 of this paper. More details about the RFID can be found in [1].

This paper is organized as follows. The first section surveys available tools and techniques that have been introduced in both digital and analog/mixed-signal low-power design domain with special attention paid to recent technological advances in this field. Additionally, state of the art of power estimation methodologies is presented. In the second section, the RFID-Smart-Sensor architecture is briefly described. The next section includes more detailed description of the proposed early power estimation technique together with an UVM framework that was created in order to automate functional verification of the chip. The simulation results that were accomplished using software tools from Cadence Design Systems are also included in this section. Finally, section 4 contains concluding remarks and possible extensions of the proposed power estimation method.

II. Low Power Techniques

A. Digital Domain

Power demand was foreseen as one the key limiting factors of the digital ICs as early as at the beginning of the 1980's. In reference [2], one can find remarks about switchable power predicted to be implemented in the processors. In this scenario, called today a multi-supply

voltage methodology, most of the chip can be in stand-by mode while only relevant part of the chip is working. Growing complexity of battery-operated devices is one of the major causes of development and improvements in low power design techniques. Tighter requirements on total power dissipated by a single chip forces designers to use more sophisticated methods such as power switch-off domains and adaptive or dynamic voltage frequency scaling [7]. With today's projects, dynamic power optimization, clock gating structures or employing high-threshold-voltage transistors for non-critical timing paths are not always considered as a lower power-techniques but rather classified as a part of standard, baseline implementation flows.

It has to be noted, however, that implementing advanced low power design techniques may connected with introducing additional circuitry for power managing which increases even more level of complexity of the design which, in turn, impacts verification process. As a consequence a new branch of Electronic Design Automation (EDA) tools was introduced – called low power verification. This group of EDA solutions is aimed at checking whether power intent of the design does not disturb normal functionality of the processor. Common Power Format (CPF)[8] or Unified Power Format (UPF)[9] files have been introduced in order to facilitate specification of low power features in structured and organized manner. Another group of low power tools, which includes power integrity analyses, addresses issues such as voltage drop on the supply power lines (so called IR drop). These tools have direct impact on the chip implementation phase when power structure and floorplan are developed.

B. Analog Domain

Development of methods of comprehensive chip verification with presence of power shutoff or multiple supply voltage (MSV) domains manifests itself also in the mixed-signal simulation field. In this case, translating signals between digital and analog domains can no longer be done without providing crucial information about the power specification (voltage levels for each domain, etc.) coded using for instance a CPF file. Varying logic levels of signal coming from digital domain may have a critical impact on functionality of the analog portion of the design.

All of the mentioned low power solutions focus on chip implementation aspects where it is assumed that RTL code and transistor-level schematics are already mature enough to be realized in silicon. In contrast, this paper concentrates on power profiling – i.e. correlation between power consumption in time and actual operation (state) of the chip. With the proposed approach, violation of peak power consumption can be reliably tracked at early stage of the design when changes to the chip architecture or sequence of operation can be easily introduced without a need of employing Engineering Change Order (ECO) flows.

C. Power estimation techniques

Paul Ladman [3] gives an interesting survey of available methods of power estimation for digital blocks. The presented methods can be divided into two categories: Analytical and Empirical. The latter solution based on predicting power consumption derived from existing implementations is out of scope of this paper.

The analytical power estimation methods, which attempts to relate power losses with key design parameters, can be further divided into Complexity- and Activity- based methods. In the first scenario, power demand of a digital block is related to number of arbitrary chosen equivalent gates that realize given logic functionality [4]. Although there were some developments of the power estimation that take into account different design parts (logic, memory, interconnects)[5], the complexity-based methods is based on the fixed activity factor that needs to be provided by the user. Taking into account that more and more digital designs employ techniques such as clock gating or power-switch-off domains, the fixed and constant activity rate can lead to serious imprecision in estimating total power consumption.

Nemani and Najm in [6] propose different power estimation technique for RT-level design which belongs to so called activity-based group. In this approach switching activity of internal nodes of the design is estimated based of properties of entropy function used commonly in information theory as a metric for average activity of the design. However, this methodology does not include any timing information during the power analysis. As a consequence, internal glitching is not taken into account during estimation. Also, if we take into account that in today's designs individual blocks can work with changing frequency, applicability of entropy-besed power estimation method is limited.

In the presented approach power estimation is based on transient simulations in a complete mixed-signal environment. In contrast to other vector-dependent power estimation techniques, we do not employ arbitrary set of typical input vectors for gathering activity data of RT-level blocks. Activity of the digital portion of the chip is derived from full-system simulations using stimuli generated in mixed-signal UVM environment. This way, we are able to link behavioral simulations with peak power consumption which can be a critical figure of merit for type devices concerned in this paper.

III. RFID- Smart-Sensor System Verification

A. RFID-Smart-Sensor Architecture

Figure 1 shows a simplified schematic of the RFID-Smart-Sensor architecture. The major application of the chip is the automated laboratory stand. The individual parts of the design were color-coded accordingly to its verification domain. The main components of the chip are:

- analog front-end which is used for communication with external world via modified version of RFID protocol – analog part
- sensor array with Analog-to-Digital Converters (ADCs) – mixed-signal part
- power management and control unit with instruction decoder/encoder – digital part

Apart from RF communication, the presented IC also provides energy harvesting capabilities. Thus, it is crucial that power consumption of the presented system should be kept in well-defined limits.

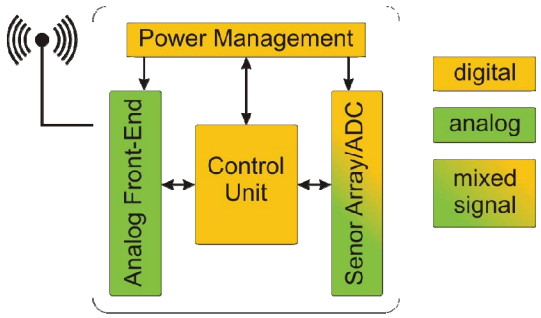


Figure 1. Simplified architecture of the RFID sensor tag.

IV. Early Power Estimation

The goal of the proposed method is to indicate peak power periods and associate it with internal operational state of the chip (more precisely internal finite state machine, FSM) in order to enable architectural or RTL optimization and its refinement before physical implementation takes place. Figure 2 schematically shows the proposed idea. Different parts of the chip are associated with power indicators. More details about deriving these indicators will be described later in the paper. By observing peak power (current) consumption, it is possible to determine hot spots in time waveforms. Since the design is still at early stage of development, we are able to combine peak power consumption periods with current state of the control unit logic.

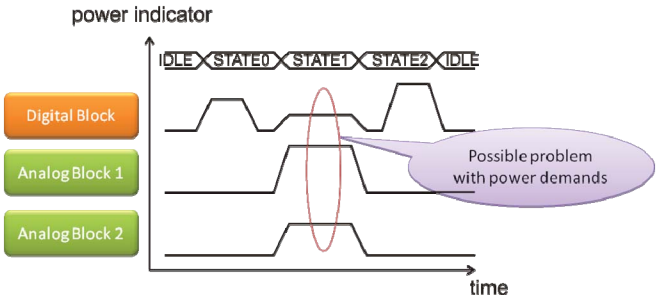


Figure 2. Power profiling in mixed-signal environment – general idea.

The proposed method can be divided into three major points:

- Behavioral modeling of the chip
- Mixed signal simulation
- Extracting power indicators for analog and digital domain

The method presented in this paper is based on modeling of the complete chip in order to apply a mixed-language UVM environment. It was decided to use the Verilog-D to represent behavior of the digital portion of the chip. Behavioral description of digital part using Hardware Description Language (HDL) like Verilog-D which enables time-efficient simulations has been known to bring significant improvements to a verification process. A growing need of applying similar behavioral modeling manner to analog parts can be observed as well. As a result, a number of description languages have been developed over last few years. In our approach, SystemVerilog together with Verilog-AMS were used to reproduce behavior analog/mixed-signal parts of the chip. What is more, in order to further limit simulation time, Real Valued Modeling (RVM) [10] approach was used. In this method, behavior of analog (or mixed-signal) blocks of the chip is represented using discretely simulated real values (wreal ports in Verilog-AMS modules). In this way, simulations of analog parts can be done using only digital solvers what noticeably accelerates the functional verification process. Obviously, the compromise between simulation time and accuracy of observed results needs to be established.

By combining RTL models with SystemVerilog and Verilog-AMS abstract models, we are able perform intensive verification of the mixed-signal chip by accelerating simulations. Our approach is well-suited to be linked with advanced verification techniques such as UVM or assertion based verification.

Figure 3 shows block schematic of the UVM-based test environment that was developed for sake of the RFID Smart-Sensor system verification. The testbench module which wraps the mixed-signal chip is aimed at generating constrained random test inputs for the Device under Test (DUT) and collecting its response. The UVM module collects signals from the DUT, compares them against expected results and reports any possible mismatches with regards to both timing and received data values.

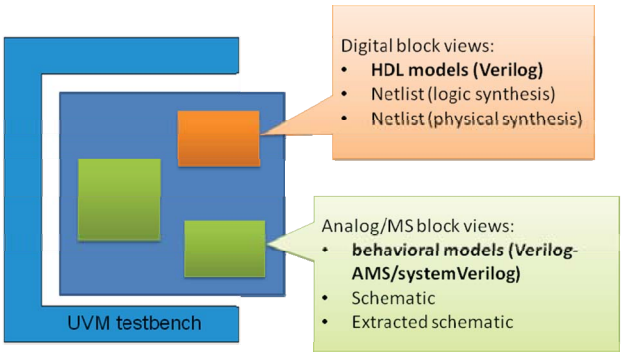


Figure 3. Verification environment.

Figure 4 shows an example of a textual report generated using the proposed UVM environment. In the top part of the report one can see the generated packet which includes a number of records (items), where *Req* is name of a packet, *Sen_sel* selects one of the on-chip sensors. There is also field *coded_1of4* which stores bits required by the UVM driver to implement ASK-modulated signal for the RFID chip – see figure 5. Other parameters needed for the simulation like stimuli for sensors and supply power conditions are also randomized within given ranges. In the lower part of the report from Figure 4, one can see the results of performed timing checks (in dotted rectangles). Finally, solid green line marks the data check in this case for the illumination sensor.

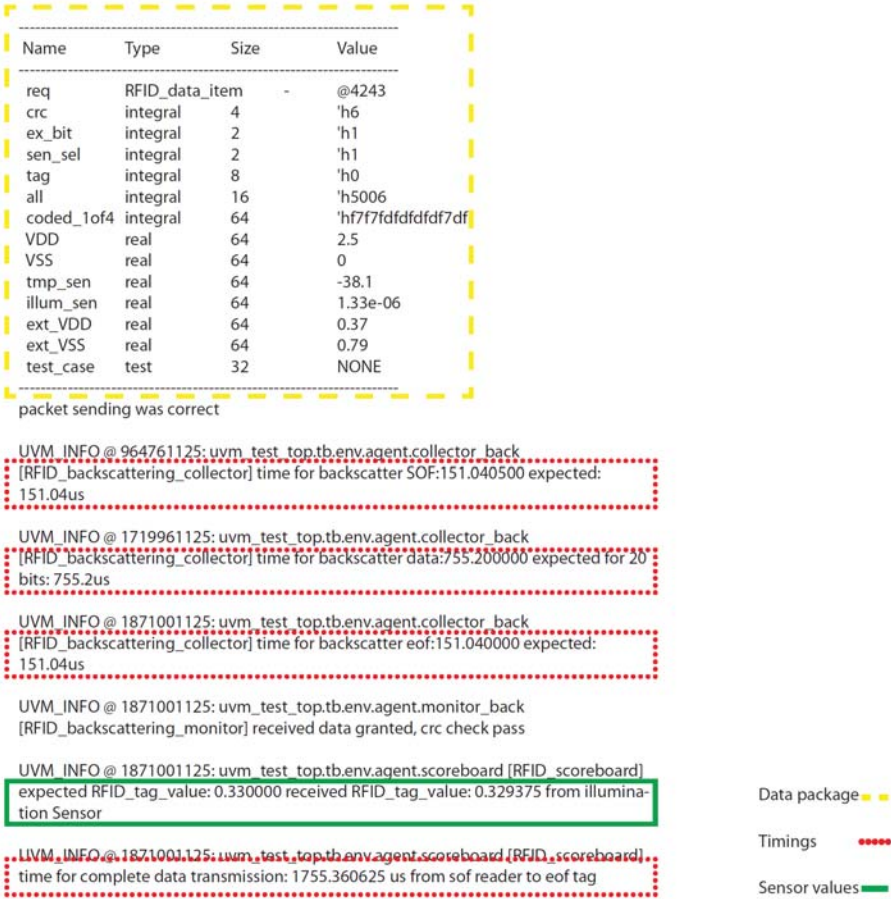


Figure 4. Example textual report generated by the proposed UVM environment.

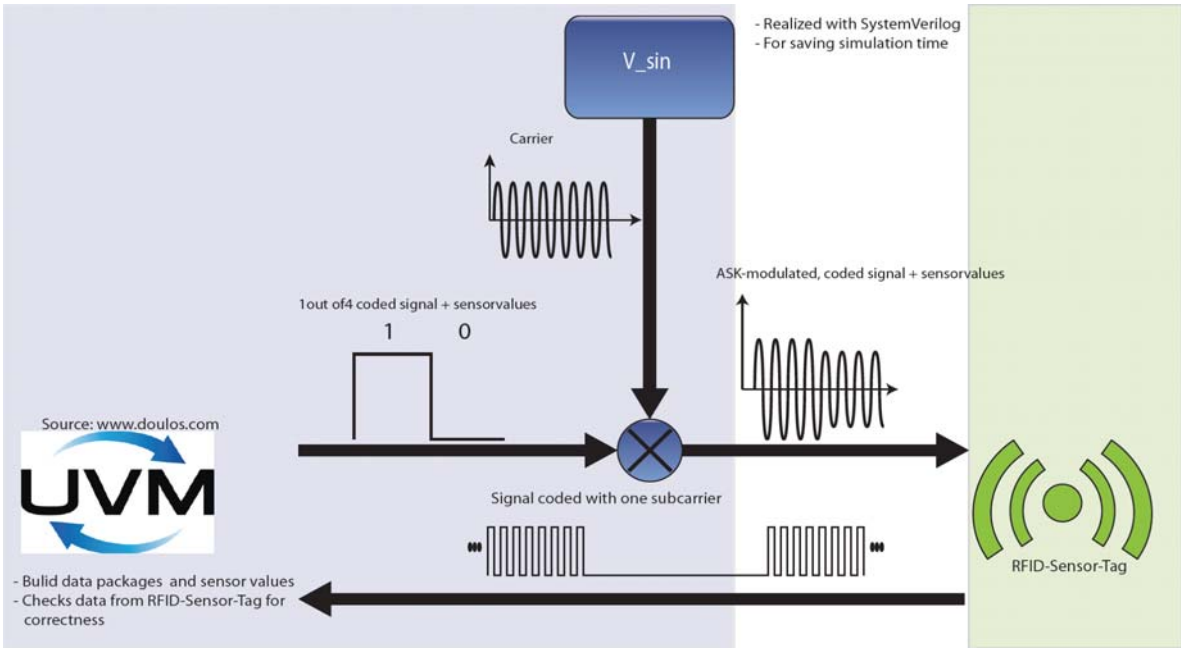


Figure 5. Generation of input signal for the RFID chip.

The described approach has a clear advantage over standard direct test vectors, since numerous test scenarios can be applied. Constrained random sequences of input data generated with UVM environment may lead to unpredicted system behavior that are hard to foreseen while creating input test vectors manually. The simulations are done in Cadence DFII environment which enabled us to switch between different abstraction levels. In this paper, we focus on early stage of the design process when only behavioral models are available.

More details about generating UVM testbench structures can be found in references [11], [12]. More detailed description of the test verification environment for RFID Smart-Sensor System can be found in [1].

In order to retrieve power information during functional verification, a power estimator needs to be defined. In our approach, the analog blocks were equipped with special ports sinking/sourcing dc current to represent power losses when the block is turned on. The current value can be derived from supply current specified in a block-level power budget of the entire design. Moreover, we assume, that current changes in discrete moments of time between finite set of values. This way activity of the analog parts can be easily bound with the current system state within simulation environment – in this case SimVision from Cadence.

In case of the digital block, a different power estimation technique was employed. In general, power dissipated by a digital block can be divided into three major components [13]

$$P = P_{dyn} + P_{dp} + P_{static},$$

where P_{dp} is dynamic (capacitive) power dissipation, P_{dp} is power loss due to direct current between supply and ground lines due to finite input and output signal slew rate during gate switching and P_{static} – static power loss due to leakage current that flows through the gate without any input stimuli. Only two first terms of Equation (1) depend on switching activity of the cells inside of a digital block – i.e. frequency of energy consuming transitions $f_{0\to1}$. We assume that static power does not play a major role.

In the proposed approach, we treat activity of internal nodes in the design as a good indicator of power consumption. Obviously, one cannot expect an absolute value of energy dissipated over a period of time based only on number of toggling count in the design. However, at very early stage of development, we are interested in getting the information on relative power consumption rather than absolute accurate power calculation.

The proposed estimation method relies heavily on quality of calculating activity of digital cells. In a traditional (direct testbench) approach getting toggling count would require writing numerous input test vectors. The novelty of our approach is to employ the UVM environment to generate a real-life activity profile. The developed simulation environment was adjusted in order to collect nodes activity in Value Change Dump (VCD) file [14]. As a consequence, the proposed power estimation method can be seen as an addition to the UVM framework.

After creation of a VCD file during an UVM session, Encounter RTL Compiler (RC) tool is used to generate a database which includes activity profile for the digital blocks. It has to be emphasized that RC is not used, in our approach, to compute power based on liberty-format models but to generate so called timing profile. The simulation time is being divided into time windows (in our case clock cycles). Each time window is assigned a value of a toggle count for a specific digital module (not its power figure). The simulation results for the digital blocks are shown in 6a). Top strip includes cumulative toggling count – our power loss estimator. Peak periods are clearly visible around *175* and *530 μs*.

Finally, by combining the current-analog models and power profile based on a VCD file, we can identify timing windows with highest activity and thus power consumption. Both indicators (dc current from analog blocks and digital block's toggle count) can be presented together with the original testcase using SimVision environment. So the state of the IC or a sequence of states that leads to the peak estimated power consumption can be traced.

The complete mixed-signal design was built in a schematic-on-top flavor. Using combination of OSS netlister, INCISIV platform together with RTL Compiler makes the simulation process smooth and reusable. The SST2 database format was used in order to combine waveform information from functional simulations and activity profiling.

Figure 6 depicts simulation results of 4 RFID sensor-tags. The input signal (Input RFID-Sensor-Tag) represents the ASK-modulated input to the sensor-tag from test environment. The signal generator is shown schematically in Figure 5. Output RFID-sensor-tag represents the encoded information to be backscattered from the tag. As it can be seen, textual representation shown in Figure 4 is much more convenient for debugging.

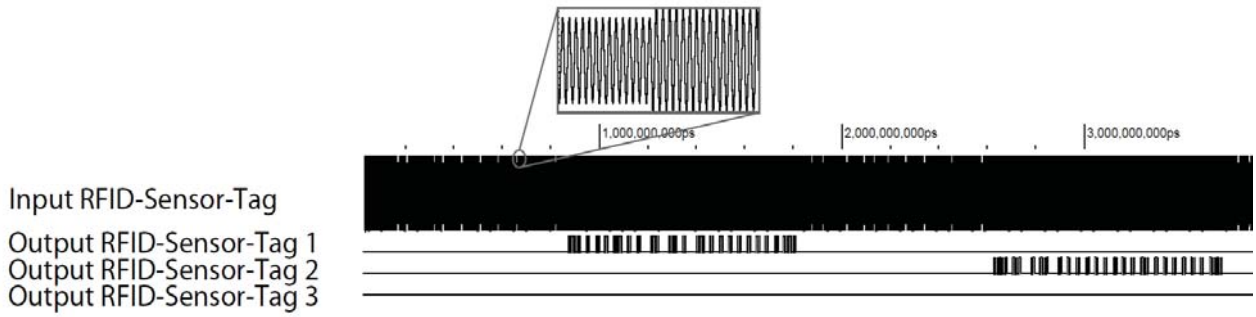


Figure 6. Functional simulation results for RDID sensor tags using UVM [1].

The functional simulations were enriched with power information gathered using the proposed method. Figure 7 gathers both functional and power simulation results generated using the proposed UVM environment. The two top charts presents nominal operation of a single RFID sensor tag while the other charts show the proposed power estimators: dc current and activity for analog/mixed-signal blocks (sensors, receiver, and analog-to-digital converters, ADCs) and digital blocks, respectively. As the on-chip receiver is always on, it generates constant dc current of 1 μA. The ADC and sensor part is active only for short period after simulation time of 1 s. As it can be seen in the figure, total current generated by analog portion of the chip is in fact ADC/sensor current offset by the value of constant current flowing through the receiver. Finally, the bottom chart shows activity of the digital part of the chip. As it can be seen, the chip was designed in order to ensure that peak activity of the digital part does not overlap with sensors or ADC operation (power consumption). The short peak of digital activity (more than 800) at the beginning of the simulation is related with system reset.

V. Other Simulation Scenarios

Although this method deals with early-stage digital power estimation, the verification UVM framework can be re-used with transistor-level schematic and/or block-level netlist for analog and digital block, respectively. Cadence DF II environment enables easily switching between different abstraction levels through the Hierarchy Editor tool.

The proposed power estimate method based on RTL code activity measuring depends on the quality of RTL code. Badly written hardware description may lead to many unnecessary toggling of the internal nodes. More accurate results can be obtained when the RTL code is optimized after logical or physical synthesis. Disadvantage of this solution is the fact that cross-probing of the original behavioral description is more difficult. Additionally, the toggle count for the digital part of the chip can be replaced with the actual current waveforms generated with Encounter Power System. More accurate, technology dependent power analysis, requires however additional technological data – power-grid libraries for the standard cells. Figure 8b) depicts simulation results for the chip after digital place and route. One can see that unit-less toggle count number is replaced by current which can be easily translated to power. It is important to notice, that peak power periods are were aligned with initial estimation from Figure 8a).

VI. Conclusion

In this paper, we present UVM-based verification environment together analog block modeling which enables early power estimation. UVM simulations provide real-life vectors that can be used for dynamic power prediction for the digital blocks when gate/transistor-level implementation is not available. The resulting data shows peak power consumption periods which can be used in order to refine RTL code or entire chip architecture.

The proposed method employs commercial tools from Cadence and can be easily implemented as an addition to standard verification and implementation methodologies.

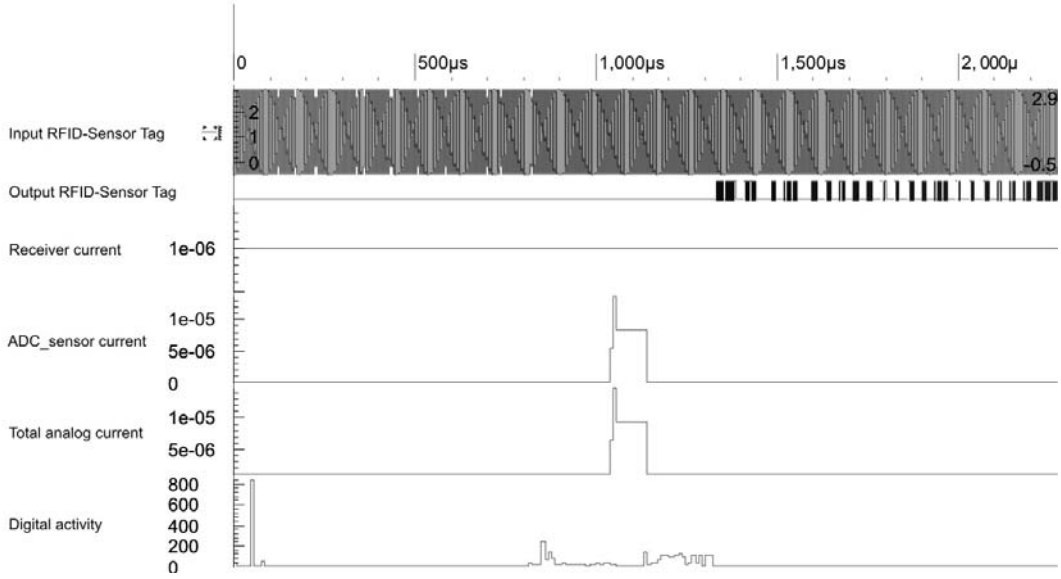
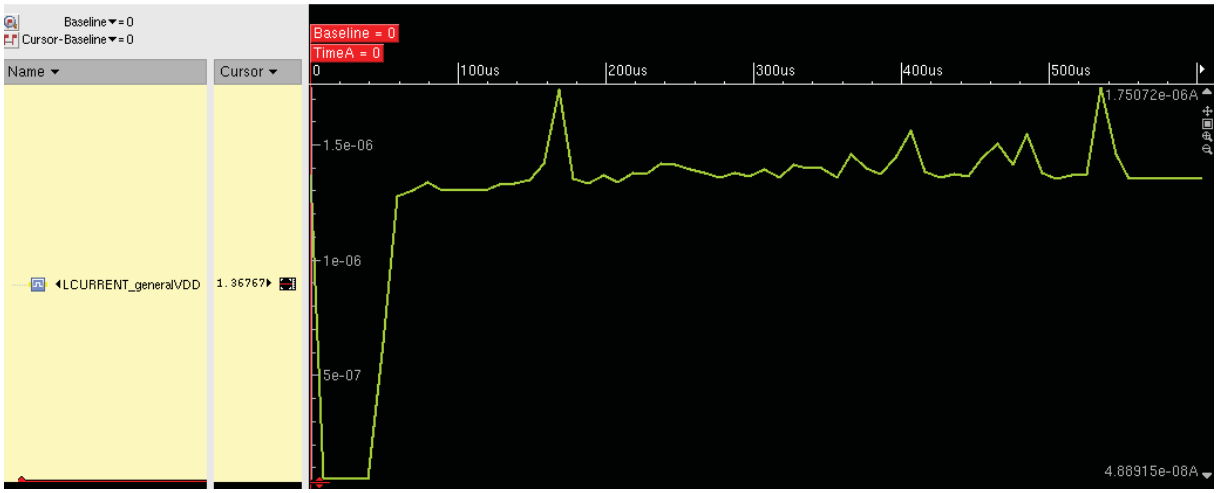


Figure 7. Functional and power simulation results of RFID sensor tag.

(a)



(b)

Figure 8. Power profiling simulation results: RTL models (a), Power-Grid-Library models (b).

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