# Analysis and Design of a First - Order ΔΣ Modulator based on Ultra Incomplete Settling and Considering Non-ideal Effects

Błażej Nowacki, Nuno Paulino, *Member, IEEE*, and João Goes, *Senior Member, IEEE*

***Abstract*— One of the main building blocks of a Delta-Sigma modulator (ΔΣM) is the integrator circuit. Usually this is implemented either in discrete or in continuous time domains using amplifiers. This paper analyses a ΔΣ circuit based on the implementation of passive switched-capacitor (SC) integrator using ultra incomplete settling. The behavior of a 1st order ΔΣM is fully analyzed and explained, as well as its non-ideal effects, which become more significant for higher clock frequencies. This work compares performance of ΔΣM clocked with $F_{clk}$=100 MHz and $F_{clk}$=300 MHz. Electrical simulations show that the ΔΣM ($F_{clk}$=300 MHz) achieves a peak signal-to-noise-plus-distortion ratio (SNDR) of 67.5 dB, a peak signal-to-noise ratio (SNR) of 69.7 dB for a signal with a bandwidth (BW) of 400 kHz, while dissipating only 232 μW from a 1.1 V power supply voltage, resulting in a figure-of-merit (FOM) of 165 fJ/conv.-step (simulated).**

***Index Terms*—Delta–sigma modulator, passive integrator, analog-to-digital (A/D) conversion, passive SC filter.**

## I. Introduction

In order to build an analog delta-sigma (ΔΣ) modulator (ΔΣM) it is necessary to use circuits that implement two basic functions: filtering and comparing. The filtering function is typically built using discrete time (DT) integrators, which can be implemented using a switched-capacitor (SC) circuit. However, in order to obtain a lossless integrator (pole located at DC), an ideal amplifier (with infinite DC gain) is required. Since the Gain-Bandwidth product (GBW) of any amplifier is finite, a SC integrator is always a first order low-pass filter. For large clock frequencies, the amplifier circuit can dissipate a large power, since it must be designed to achieve a GBW large enough to guaranty a small settling error during the clock period [1].

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All authors are with the Centre for Technologies and Systems (UNINOVA/CTS) and Departamento de Engenharia Electrotécnica, Faculdade de Ciências e Tecnologia, Universidade Nova de Lisboa (UNL), Campus FCT/UNL, 2829-516 Caparica, Portugal.
B.Nowacki, email: b.nowacki@campus.fct.unl.pt.
N.Paulino, email: nunop@uninova.pt.

It is possible to use a passive SC circuits to implement the filtering function of the ΔΣM to reduce the power dissipation of the modulator, such as the modulators described in [2], [3] and [4]. These circuits are based on a first order *RC* circuit where the resistor is replaced by a SC branch. The transfer function of this circuit is given by [4]:

$$H(z)=\frac{\dfrac{C_R}{C_R+C_1}}{z-\dfrac{C_1}{C_R+C_1}}=\frac{\alpha}{z-\beta} \tag{1}$$

where $C_R$ is the capacitor implementing the resistor in the *RC* circuit and $C_1$ is the capacitor of the *RC* circuit. From this expression it is possible to conclude that moving the pole closer to the unity circle (by making $C_1$ larger than $C_R$) results in a decrease in the gain of the filter ($\alpha$). Another approach is to use ultra incomplete settling in order to implement a passive SC filter as theoretically proposed, for the first time, in [5] by the same authors of this paper.

This paper is organized as follows. Section II describes a concept of ultra incomplete settling in a SC integrator. Section III provides an in-depth analysis of proposed ΔΣM. Study of nonlinear effects, which figure in ΔΣM, is depicted in Section IV. Finally, the design examples and conclusions are presented in Section V and VI respectively.

## II. Concept of Ultra incomplete Settling in a SC Integrator

The capacitor voltage in an *RC* circuit after a step input with amplitude $V_{in}$, is given by:

$$v_c(t)=V_{in}\cdot\left(1-e^{-t/R_{on}\cdot C}\right)+V_{C0}\cdot e^{-t/R_{on}\cdot C} \tag{2}$$

where $V_{C0}$ is the initial voltage in the capacitor, just before the input step. Fig. 1 shows a plot of equation (1) as a function of time, for generic values of $C$ and $R_{on}$.

In the normal operation of a SC circuit it is expected that the capacitor is either (almost) completely charged or discharged at the end of the clock phase, corresponding to the complete settling area in the graph of Fig. 1.

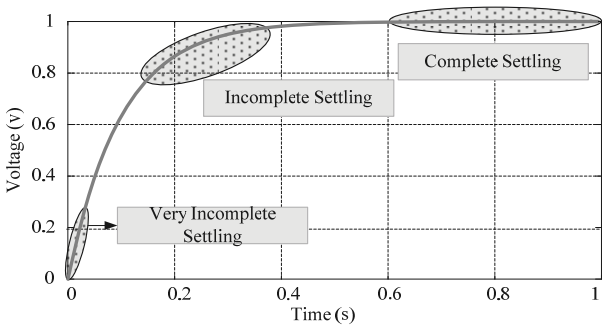


Figure 1. Capacitor voltage for a step input (normalized time).

If the duration of the clock phase is much smaller than the time constant of the circuit, the *RC* circuit operates under the ultra incomplete settling condition $T_s << R_{on} \cdot C$. This can be achieved by adding an explicit resistance, with the appropriate value, in series with the switch. In the case of ultra incomplete settling, the voltage in the capacitor at the end of the phase becomes a function of the input voltage ($V_{in}$) and of the capacitor voltage value in the previous clock cycle ($V_{C0}$).

## III. First Order Delta-Sigma Modulator

A complete ΔΣM can be built using the passive SC circuit that was described in the previous section. Fig. 2 depicts the schematic of the proposed first-order differential ΔΣM working with clock frequency $F_{clk}$=100 MHz. A passive sample-and-hold (S/H) circuit is used because the incomplete settling behavior of the filter circuit means that its cut-off frequency is low, therefore it would significantly attenuate the continuous time input signal.

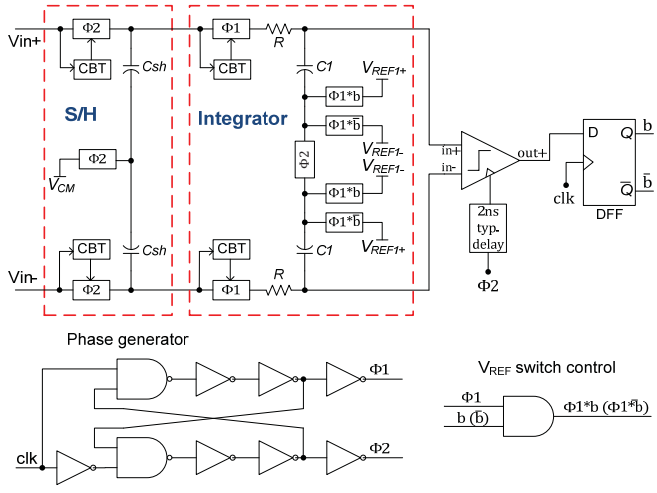


Figure 2. Complete schematic of the **ΔΣ** modulator circuit ($F_{clk}$=100 MHz).

Assuming incomplete settling in the SC integrator circuit, the input signal is firstly sampled in $C_{SH}$ at the end of phase $\Phi_2$ and then, during phase $\Phi_1$, $C_{SH}$ is connected to $C_1$ through series resistor *R*. The SC integrator is followed by comparator with zero threshold voltage and by a D-type flip-flop (D-FF) producing the output bit stream. Moreover in the design the clock bootstrapped (CBT) switches are used because they maintain good resistance linearity.

### A. Discrete Time Transfer Function and Z Transfer Function of the SC Integrator

Fig. 3 a) depicts circuit of S/H and integrator in phase $\Phi_1$. Fig. 3 b) and c) show its transformation that is being analyzed underneath in order to obtain discrete time transfer function and *Z* transfer function of the SC integrator.
Equation for the voltages in the loop depicted in Fig. 3 c) is:

$$2 \cdot v_1(t) + 2 \cdot R \cdot i_C(t) - 2 \cdot v_{SH}(t) + V_{DD} = 0 \tag{3}$$

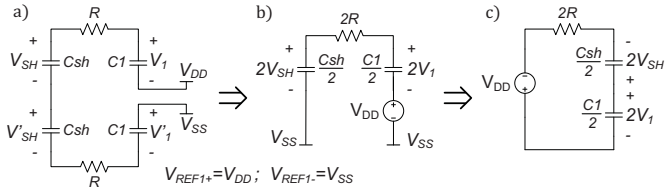


Figure 3. Circuit in phase $\Phi_1$ (a) and its transformation (b, c).

From the equation for current flowing through capacitors:

$$C_1 \cdot \frac{dv_1(t)}{dt} = -C_{SH} \cdot \frac{dv_{SH}(t)}{dt} \tag{4}$$

we can write:

$$v_{SH}(t) = -\frac{C_1}{C_{SH}} \cdot v_1(t) + \frac{C_1}{C_{SH}} \cdot v_1(0) + v_{IN} \tag{5}$$

where $V_{IN} = v_{SH}(0)$, represents the sampled value of the input voltage in phase $\Phi_2$. From (3) and (5) it is obtained:

$$v_1(t) \cdot \left[\frac{C_{SH} + C_1}{C_{SH}}\right] + R \cdot C_1 \cdot \frac{dv_1(t)}{dt} = \frac{C_1}{C_{SH}} \cdot v_1(0) + V_{IN} - \frac{V_{DD}}{2} \tag{6}$$

The permanent and transient solutions of (6) are considered.

$$v_1(t) = v_{1p}(t) + v_{1t}(t) \tag{7}$$

For the permanent solution $dv_1(t)/dt = 0$, and it can be written:

$$v_{1p}(t) = \frac{C_1}{C_{SH} + C_1} \cdot v_1(0) + \frac{C_{SH}}{C_{SH} + C_1} \cdot \left(V_{IN} - \frac{V_{DD}}{2}\right) \tag{8}$$

In transient solution, we assume zero initial conditions and zero values of all the inputs.

$$v_{1t}(t) = -\tau \cdot \frac{dv_1(t)}{dt} \tag{9}$$

$$v_{1t}(t) = V_0 \cdot e^{-\frac{t}{\tau}} \tag{10}$$

In above equations $\tau = R \cdot C_{EQ}$ and $C_{EQ} = C_1 \cdot C_{SH} / (C_1 + C_{SH})$.
By substituting (8) and (10) into (7) we achieve:

$$v_1(t) = V_0 \cdot e^{-\frac{t}{\tau}} + \frac{C_1}{C_{SH} + C_1} \cdot v_1(0) + \frac{C_{SH}}{C_{SH} + C_1} \cdot \left(V_{IN} - \frac{V_{DD}}{2}\right) \tag{11}$$

Obtaining $V_0$ by solving (11) for $t$=0:

$$v_1(0) = V_0 \cdot e^0 + \frac{C_1}{C_{SH}+C_1}\cdot v_1(0) + \frac{C_{SH}}{C_{SH}+C_1}\cdot\left(V_{IN} - \frac{V_{DD}}{2}\right) \quad (12)$$

$$V_0 = \frac{C_{SH}}{C_{SH}+C_1}\cdot\left(v_1(0) - V_{IN} + \frac{V_{DD}}{2}\right) \quad (13)$$

yields to:

$$v_1(t) = \frac{C_{SH}}{C_{SH}+C_1}\cdot\left(v_1(0) - V_{IN} + \frac{V_{DD}}{2}\right)\cdot e^{-\frac{t}{\tau}} + \\ + \frac{C_1}{C_{SH}+C_1}\cdot v_1(0) + \frac{C_{SH}}{C_{SH}+C_1}\cdot\left(V_{IN} - \frac{V_{DD}}{2}\right) \quad (14)$$

The (switched) *RC* circuit operates under the ultra incomplete settling condition $T_s << \tau$. Therefore we can write:

$$e^{-\frac{T_S}{2\cdot\tau}} \approx 1 - \frac{T_S}{2\cdot\tau} \quad (15)$$

By substituting (15) into (14) once can obtain:

$$v_1\left(\frac{T_S}{2}\right) \approx v_1(0)\cdot\left(1 - \frac{T_S}{2\cdot R\cdot C_1}\right) + \\ + V_{IN}\cdot\frac{T_S}{2\cdot R\cdot C_1} - \frac{V_{DD}}{2}\cdot\frac{T_S}{2\cdot R\cdot C_1} \quad (16)$$

$$v_1\left(\frac{T_S}{2}\right) \approx v_1(0)\cdot\beta + \alpha\cdot V_{IN} - \alpha\cdot\frac{V_{DD}}{2} \quad (17)$$

where $\alpha = \frac{T_S}{2\cdot R\cdot C_1}$ and $\beta$=1-$\alpha$. Equation (17) provides the voltage in capacitor $C_1$ at the end of the phase $\Phi_1$, which is the output voltage of the integrator. Fig. 4 depicts voltage changes in capacitors $C_1$ and $C_{SH}$ (which samples and holds $V_{IN}$).

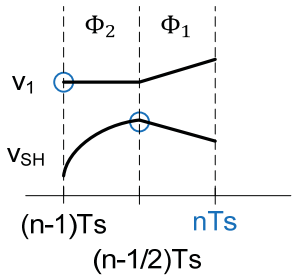


Figure 4. Typical voltage waveforms in capacitors $C_1$ and $C_{SH}$.

Note that during phase $\Phi_2$ capacitor $C_{SH}$ operates under the complete settling condition. Taking into consideration that $v_1(0) = v_1[n-1]$ and $v_{IN} = V_{SH}(0) = V_{IN}[n-0.5]$ (Fig.4) and (17), one can write:

$$v_1[n] = v_1[n-1]\cdot\beta + V_{IN}\left[n-\frac{1}{2}\right]\cdot\alpha - \frac{V_{DD}}{2}\cdot\alpha \quad (18)$$

At this point it is important to note from (18) that, as long as the ultra incomplete settling condition is valid, the voltage $v_1$ is independent of the value of the input sampling capacitance $C_{SH}$. Assuming that $\alpha$ is small the amplitude of $V_1$ is small and therefore in order to obtain a digital level from this voltage it is necessary to use a comparator, which can saturate its output voltage (to either $V_{DD}$ or $V_{SS}$) in a short time.

From (18), assuming reference input equal to zero, the *Z* transfer function of the integrator can be obtained.

$$H(z) = \frac{v_1(z)}{V_{IN}(z)} = \frac{\alpha\cdot z^{-\frac{1}{2}}}{1-\beta\cdot z^{-1}} \quad (19)$$

This expression shows that a SC branch, under the right condition, can behave as a passive DT first-order filter. The maximum and minimum gain values of (19) (note that $\beta$=1-$\alpha$) are given, respectively, by:

$$H_{\max} = |H(z=1)| = \left|\frac{\alpha}{1-\beta}\right| = 1 \\ H_{\min} = |H(z=-1)| = \left|\frac{\alpha}{1+\beta}\right| \approx \frac{\alpha}{2-\alpha} \quad (20)$$

These expressions show that in order to increase the ratio between the maximum and minimum gain it is necessary to reduce the gain of the circuit ($\alpha$), which means that the signal amplitude will be very small. Using a small $\alpha$ moves the pole of the circuit closer to the unity circle (by making $\beta$ closer to 1).

### *B. Thermal Noise Analysis*

It is known [6] that, in equilibrium, the sampled thermal noise power at the terminals of a capacitor inside an *RC* circuit is given by $k\cdot T/C$. In the case of ultra incomplete settling, the voltage in the capacitor does not have time to reach the equilibrium condition and therefore it is necessary to recalculate the thermal noise power in the capacitor considering that the switch is closed during a finite time $T_s$. In the following considerations we analyze circuit depicted in Fig. 3 c) assuming that $V_{DD}$ is replaced with $V_x$. The step response of this circuit is composed of two parts, the first occurs before the switch opens ($t<T_s$) and is given by:

$$v_1(t) = C_{SH}\cdot\left(\frac{1}{C1+C_{SH}} - \frac{e^{\frac{-t}{C_{EQ}\cdot Ron}}}{C1+C_{SH}}\right)\cdot V_x \quad (21)$$

the second occurs after the switch opens ($t>T_s$) and is given by a constant (the sampled voltage value). The impulse response of the circuit is given by the derivative of the step response $\left(h(t) = \frac{dv_1(t)/dx}{V_x}\right)$, resulting in:

$$h(t) = \begin{cases} \frac{1}{R\cdot C_1}\cdot e^{\frac{-t}{C_{EQ}\cdot R}} & 0 \le t \le T_S \\ 0 & t > T_S \end{cases} \approx \begin{cases} \frac{1}{R\cdot C_1} & 0 \le t \le T_S \\ 0 & t > T_S \end{cases} \quad (22)$$

The transfer function, in the frequency domain, can be obtained by applying the Fourier transform to the previous expression:

$$H(f)=\int_{-\infty}^{\infty}h(t)\cdot e^{-2\cdot\pi\cdot f\cdot t}dt=\frac{\sin\left(\pi\cdot f\cdot T_S\right)}{\pi^2\cdot f\cdot C_1\cdot R} \tag{23}$$

The thermal noise power sampled into the capacitor, at the end of a clock period, is given by:

$$P_{NT}=\int_0^{\infty}4\cdot k\cdot T\cdot R\cdot\left|H(f)\right|^2df=\frac{2\cdot k\cdot T\cdot T_S}{C_1^2\cdot R} \tag{24}$$

The input referred noise can be calculated by:

$$P_{NTinput}=\frac{P_{NT}}{\alpha^2}=\frac{2\cdot k\cdot T\cdot R}{T_S}=\frac{2\cdot k\cdot T}{C_1\cdot\alpha} \tag{25}$$

This expression shows that, since $\alpha$ is small, the input referred noise power is necessarily higher than in an active SC circuit (a similar result was also reached for the passive SC circuit in [4]). This means that, passive SC circuits should use larger capacitance values than active SC circuits, in order to achieve similar thermal noise performances. However, it is important to notice that this is only a minor drawback in terms of area, since the (static) power dissipation does not increase because there are no amplifiers in the circuit. Moreover, the amount of charge that the reference voltage buffers need to supply to the circuit is very small due to the incomplete settling behavior of the circuit. Hence, there is also no significant overhead in terms of dynamic power dissipated in charging and discharging the capacitors. In fact, this is the most significant advantage of our solution based on very-incomplete settling, when compared with other passive SC approaches such as the one in [4].

### C. Block Diagram and Transfer Function of the Modulator

The block diagram of the ΔΣ modulator is shown in Fig. 5. In this diagram passive filter is represented by its *Z* transfer function. This diagram also includes all the noise sources of the circuit; namely: thermal noise, comparator noise and quantization noise.

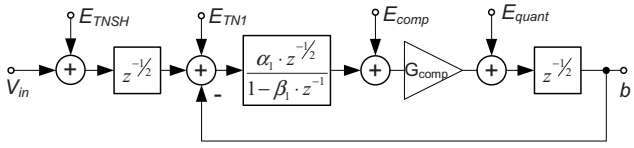


Figure 5. Block diagram of the passive ΔΣ modulator.

The gain of the comparator ($G_{comp}$), considered as a ratio of the rms value of the output of the comparator to rms value of its input can only be determined from simulation. However $G_{comp}$ can be estimated using the approach described in [2]: when the input of the modulator is 0, the output bit-stream will be a square wave with a frequency equal to $F_s/2$. The feedback signal will be a square wave with amplitude equal to $V_{DD}$, this signal will be attenuated by the passive filter of the loop resulting in a signal with a small amplitude at the input of the comparator. Therefore, $G_{comp}$ can be estimated by calculating the transfer function from the output to the input of the comparator and evaluating this function at $F_s/2$. According to approach described in [2] the estimated value of $G_{comp}$ is:

$$G_{comp}=\frac{1}{\left|H\left(\frac{F_S}{2}\right)\right|}=\frac{1}{\left|H(z=-1)\right|}=\frac{2-\alpha}{\alpha}\approx\frac{2}{\alpha} \tag{26}$$

However, in the previous analysis the influence of the quantization noise, which lowers the value of $G_{comp}$, was ignored. In order to estimate correct value of $G_{comp}$, a transient simulation with a sinusoid input signal was performed. The FFT of both the input and output signals of the comparator was computed and the power in the signal bin was calculated. The comparator gain is obtained by dividing the output power by the input power the resulting value of $G_{comp}$ was to:

$$G_{comp}=\frac{1}{\alpha} \tag{27}$$

The signal transfer function of the modulator depicted in Fig. 5 is given by:

$$STF=\frac{G_{comp}\cdot\alpha\cdot z^{-\frac{3}{2}}}{1+\left(G_{comp}\cdot\alpha-\beta\right)\cdot z^{-1}} \tag{28}$$

The plot of |*STF*|, depicted in Fig. 6, shows a plateau at the level of 0 dB.

### D. Noise Transfer Functions

The quantization NTF of the ΔΣ modulator can be calculated using the block diagram (Fig. 5) and it is given by:

$$NTF_{quant}=\frac{b}{E_{quant}}=\frac{(1-\beta\cdot z^{-1})\cdot z^{-\frac{1}{2}}}{1+\left(\alpha\cdot G_{comp}-\beta\right)\cdot z^{-1}} \tag{29}$$

As expected, the $NTF_{quant}$ is a high-pass transfer function; the gain of this function at DC is given by (using $G_{comp}\approx 1/\alpha$ ):

$$\left|NTF_{quant}(z=1)\right|\approx\frac{\alpha}{1+\alpha}\approx\alpha \tag{30}$$

Fig. 6 presents the plot of $|NTF_{quant}|$, which shows that for low frequencies the quantization noise is significantly attenuated, as it results from (30).

The thermal noise transfer function and its DC gain are given by:

$$\begin{aligned}NTF_{therm}&=\frac{G_{comp}\cdot\alpha\cdot z^{-1}}{1+\left(G_{comp}\cdot\alpha-\beta\right)\cdot z^{-1}}\\ \left|NTF_{therm}(z=1)\right|&\approx\left|\frac{-1}{1-\alpha}\right|\approx 1\end{aligned} \tag{31}$$

The plot of $|NTF_{therm}|$ (Fig. 6) shows a similar behavior to the *STF*, which indicates the thermal noise has significant meaning within the range of the low frequencies.

The input referred noise voltage of the comparator ($E_{comp}$) can be critical in a passive ΔΣM because the input voltage of the comparator has small amplitude [2]. The gain of the $NTF_{comp}$ in DC of the comparator noise is given by:

$$NTF_{comp} = \frac{G_{comp} \cdot \left(1 - \beta \cdot z^{-1}\right) \cdot z^{-\frac{1}{2}}}{1 + \left(\alpha \cdot G_{comp} - \beta\right) \cdot z^{-1}}$$
$$\left|NTF_{comp}(z=1)\right| \approx \frac{1}{1+\alpha} \approx 1 \quad (32)$$

One can notice that, within the range of low frequencies, the graph of $NTF_{comp}$ coincides with the one of $NTF_{therm}$, and comparator noise is amplified in high frequencies range.

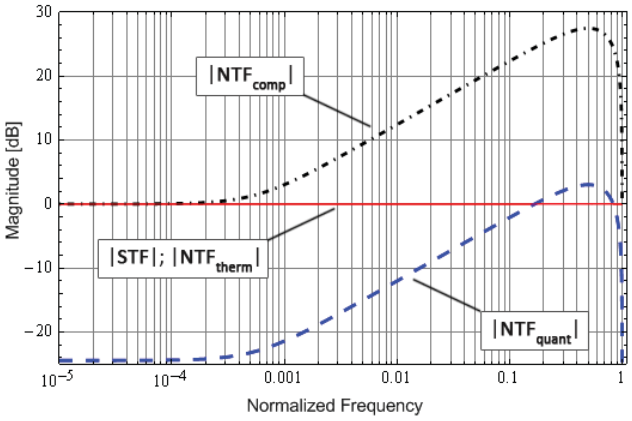


Figure 6. Graphs of signal and noise transfer functions.

## IV. Nonlinear Effects in ΔΣM Circuit

The existence of non-ideal effects in the circuit, such as parasitic capacitances and on-resistances in the switches, influences the performance of the Delta-Sigma Modulator, these effects become more important for higher clock frequencies. Therefore it is important to take into consideration these effects while designing high $F_{clk}$ ΔΣM.

### A. Parasitic Capacitances

For ΔΣMs operating with $F_{clk}$ around 100 MHz parasitic effects can be negligible. However they become more important with increasing the $F_{clk}$ of modulator. Fig. 7 depicts single-ended branch of the integrator including the relevant parasitic capacitances. In phase $\Phi_1$ the integrator's input switch is closed and the signal from S/H passes, through resistor R, to capacitor $C_1$ (integration), simultaneously charging $C_P$ (parasitic capacitance due to the switch and resistor). In phase $\Phi_2$ the voltage on $C_1$ should be held to let the comparator to produce correct value. However, the previously charged $C_P$ discharges through $R$, causing an unwanted integration during this phase Due to the UIS, even a small value $C_p$ is enough to provide the same amount of charge to C1 as the one received during the integration phase. This second integration increases the gain of the integrator and can cause early saturation of the modulator for higher magnitude values.

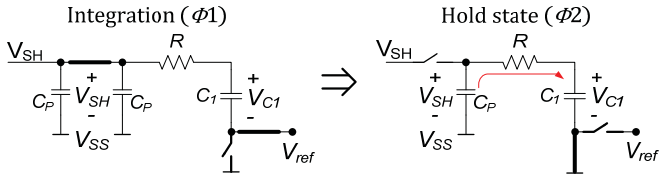


Figure 7. Single-ended branch of the integrator.

There is a simple solution that can reduce significantly the influence of this parasitic capacitance: moving $R$ before the integrator's input switch. This causes the resistor $R$ to be disconnected from the integrating capacitor, therefore eliminating the integration during the second phase. Since $C_P$ is now connected in parallel with $C_1$ it does not cause integration. One can notice that moving $R$ does not change any of the equations derived in Section III.

### B. ON resistance of switches

Fig. 8 shows single-ended branch on the integrator with switch $SW_{\mathrm{REF}}$ illustrated by parasitic elements $R_{ON}$ and $C_P$. The voltage $V_1$ in the integration phase ideally should be equal to $V_{\mathrm{ref}}$. However, because of parasitic components of $SW_{\mathrm{REF}}$ this voltage has an exponential characteristic (Fig. 9). Big value of $R_{ON}$ causes that $V_1$ slower achieves level of $V_{\mathrm{ref}}$, which results in additional distortion. Moreover from the analyses of ΔΣM introduced in Section III we know that factor $\alpha$ depends on $R$. At this point one can conclude that value of $\alpha$ depends on $R$ and ON resistance of the integrator's input switch $SW_{\mathrm{IN}}$. These extra resistance should be taken into consideration because $\alpha$ can change its value by few percent from expected one. In case of above described phenomena it is necessary to maintain low values of ON resistances of the switches.

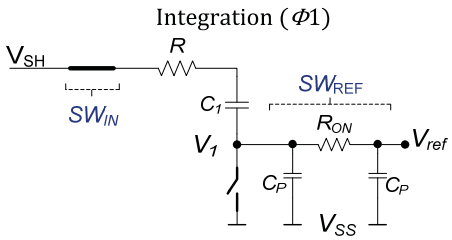


Figure 8. Single-ended $RC_1$ branch in the integration phase.

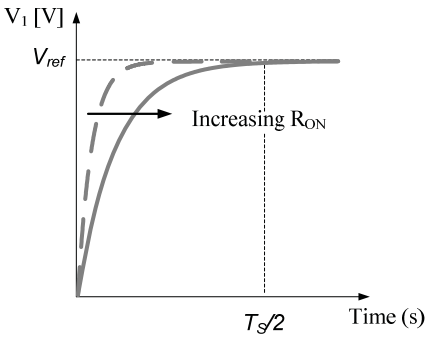


Figure 9. Characteristic of voltage $V1$ in the integration phase.

### C. Jitter

Fig. 10 illustrates the $RC_1$ branch of the integrator and a graph of current flowing through $C_1$.

Usually, typical DT ΔΣMs are immune to clock jitter because voltage on capacitor is settled and any changes of clock phase's duration do not result in its significant change (Fig. 10 b). However keeping in mind that presented ΔΣM is based on DT SC filters using ultra incomplete settling, jitter becomes a significant issue.

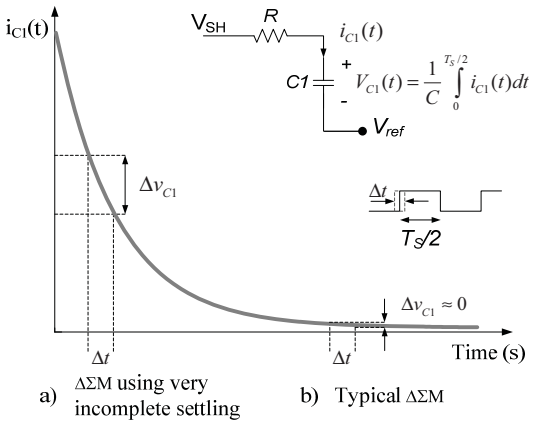


Figure 10. Integrator's capacitor voltage change vs. jitter.

In this case, similarly to continuous time ΔΣMs, shorter or longer phase duration causes that voltage on $C_1$ can be encumbered with a voltage error (Fig. 10 a) that depends on the time instant when the switch opens. Hence, the higher $F_{clk}$ is used, the more significant this error can be. Because of jitter sensitive of presented architecture, the careful design and consequently layout is required.

## V. Design Example

As a proof of concept, two ΔΣMs architectures (with $F_{clk}$=100 MHz and $F_{clk}$=300 MHz) were designed and simulated at electrical level. The electrical simulations were performed using a differential circuit corresponding to the circuit of Fig. 2 and Fig.11.

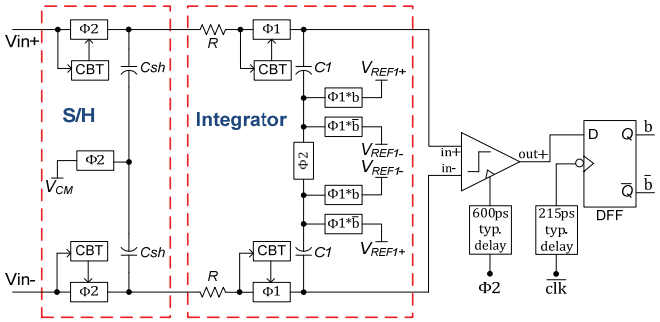


Figure 11. Complete schematic of the ΔΣ modulator circuit ($F_{clk}$=300 MHz).

These circuits were designed in a 0.13 µm logic CMOS technology (resistors where implemented using HR-poly, the capacitors using metal-insulator-metal structures (MiM) and only standard $V_T$ transistors were used) with a power supply voltage value of 1.1 V. Since obtaining incomplete settling requires adding explicit resistors, it is natural to use a high sampling frequency in order to reduce the area of the resistors. This is because two examples of ΔΣMs were selected:

- with clock frequency of 100 MHz and an OSR value of 167 (corresponding to a signal BW of 300 kHz);
- with clock frequency of 300 MHz and an OSR value of 375 (corresponding to a signal BW of 400 kHz).

SC circuits operating in ultra incomplete settling (small value of $\alpha$) have necessarily very small signal amplitudes. This means that a larger capacitance $C_1$ value must be used to obtain acceptable SNR values. Due to the ultra incomplete settling behavior this large capacitance needs only a small amount of charge and therefore the current required from the reference voltages is very small. The comparator must amplify the small amplitude signal at the output of the second integrator into a digital level (1.1V or 0V) and therefore it should have a large gain. This is achieved by employing positive feedback in the comparator. This type of comparator has very high voltage gain and therefore, after a short time, it will always saturate its output voltage to either $V_{DD}$ or $V_{SS}$. In case of using even smaller value of $\alpha$, a pre-amplification block for comparator would be required, which could be realized by applying parametric amplification as proposed in [7]. The circuit of the comparator (adapted from [8]) used in the simulations is shown in Fig. 12.

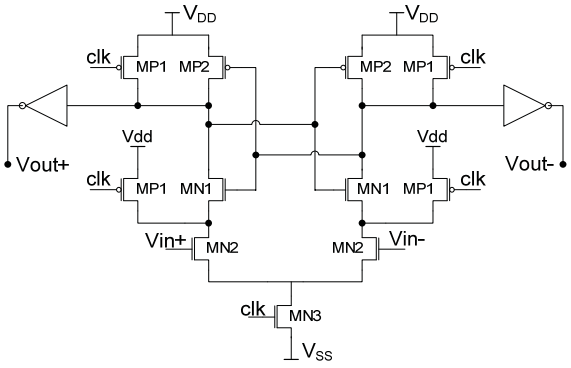


Figure 12. Electrical schematic of the fully-dynamic comparator.

The circuits of the both ΔΣMs, with $F_{clk}$=100 MHz and $F_{clk}$=300 MHz, were tested by applying input sinewave signals with frequencies of 40 kHz and 46 kHz respectively. The FFTs of the output signals for an input signal with amplitude of 300 mV, obtained by electrical transient noise simulations, are shown in Fig. 13 and Fig. 14 respectively.

The optimized modulator design parameters are summarized in TABLE I. These parameters result in $\alpha$ equal to 0.0036 (for $F_{clk}$=100 MHz) and 0.0028 (for $F_{clk}$=300 MHz). Exhaustive electrical transient-noise simulations show that the proposed ΔΣM circuits achieve performance parameters depicted in TABLE II. One can notice that circuit with increased clock frequency obtained better figure of merit.

TABLE I. ΔΣM DESIGN PARAMETERS

| Parameter | $F_{clk}$ | $C_{SH}$ | $R$ | $C_1$ | $V_{ref+}$; $V_{ref-}$ [V] |
|---|---|---|---|---|---|
| Value | 100 MHz | 10 pF | 140 kΩ | 10 pF | 1.1; 0 |
| | 300 MHz | 10 pF | 60 kΩ | 10 pF | 0.85; 0.25 |

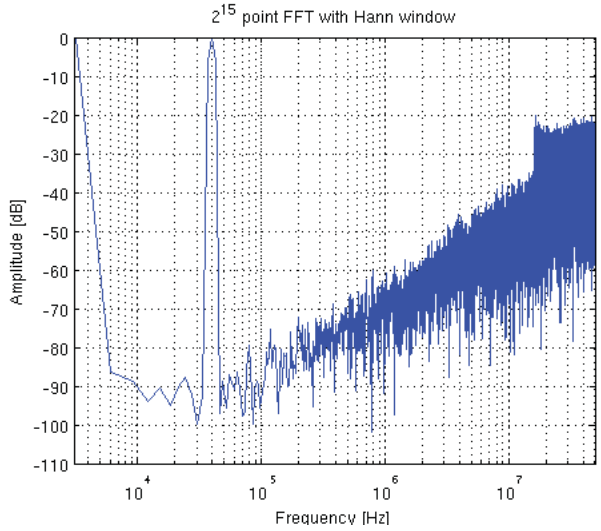


Figure 13. FFT with $2^{15}$ point of the output bit-stream of the ΣΔM with $F_{clk}$=100 MHz, obtained by electrical transient noise simulation of the complete circuit, for 300 mV amplitudes of the input signal.

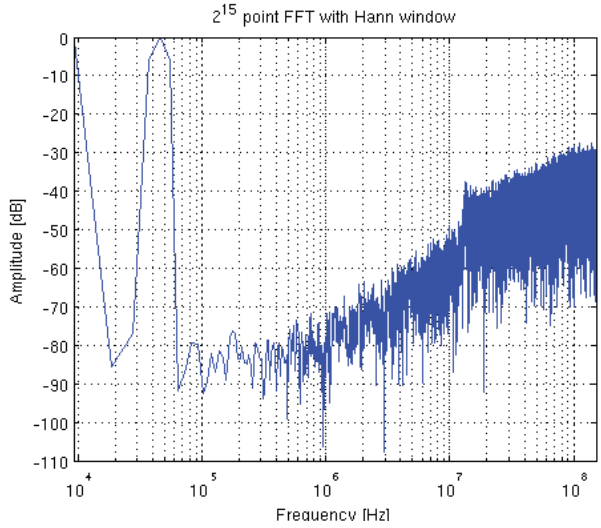


Figure 14. FFT with $2^{15}$ point of the output bit-stream of the ΣΔM with $F_{clk}$=300 MHz, obtained by electrical transient noise simulation of the complete circuit, for 300 mV amplitudes of the input signal.

TABLE II. SIMULATED KEY PERFORMANCE PARAMETERS

| Techno-logy [nm] | $V_{suply}$ [V] | BW [kHz] | SNR [dB] | SNDR [dB] | THD [dB] | *Pc* [µW] | FOM [fJ/ conv.-step] |
|---|---|---|---|---|---|---|---|
| 130-CMOS | 1.1 | 300 | 63 | 62 | -69 | 114 | 196.7 |
| | | 400 | 69.7 | 67.5 | -71.4 | 232 | 165 |

## VI. CONCLUSIONS

This paper presented a 1st order ΔΣM based on the implementation of DT SC filter using ultra incomplete settling. This approach allows building a ΔΣM with dynamic elements and reducing the power dissipation because only the comparator becomes the remaining active block in the modulator. Two examples of 1st order ΔΣM architectures using this technique were presented and analyzed in detail together with its nonlinear effects. Electrical transient noise simulations show the validity of the proposed concept.

## REFERENCES

[1] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Trans. Circuits Syst*.-I, vol. 52, no. 11, pp. 2358–2367, Nov. 2005.

[2] F. Chen and B. Leung, "A 0.25-mW low-pass passive sigma–delta modulator with built-in mixer for a 10-MHz IF input*," IEEE J. Solid-State Circuits*, vol. 32, pp. 774–781, Jun. 1997.

[3] F. Chen; Ramaswamy, S.; Bakkaloglu, B.; "A 1.5V 1mA 80dB passive ΣΔ ADC in 0.13µm digital CMOS process," *Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International* , vol., no., pp. 54- 477 vol.1, 2003.

[4] Yousry, R.; Hegazi, E.; Ragai, H.F.;"A Third-Order 9-Bit 10-MHz CMOS ΔΣ Modulator With One Active Stage," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol.55, no.9, pp.2469-2482, Oct. 2008.

[5] B. Nowacki, N. Paulino, J. Goes "A Second-Order Switched-Capacitor ΔΣ Modulator Using Very Incomplete Settling" *IEEE International Symposium on Circuits and Systems, ISCAS'2011, May 2011*

[6] Nyquist H., "Thermal agitation of electric charge in conductors", Physical Review 1928;32:110–3.

[7] Oliveira, J.P.; Goes, J.; Esperanca, B.; Paulino, N.; Fernandes, J.; , "Low-Power CMOS Comparator with Embedded Amplification for Ultra-high-speed ADCs," *IEEE International Symposium on Circuits and Systems, ISCAS'2007,* , pp.3602-3605, May 2007.

[8] Kobayashi, T.; Nogami, K.; Shirotori, T.; Fujimoto, Y., "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," *Journal of Solid-State Circuits, IEEE*, vol.28, no.4, pp.523-527, Apr 199