Surface Potential Modeling of a High-*k* HfO_2-Ta_2O_5 Capacitor in Verilog-A

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***Abstract*—A compact model of a high-*k* HfO_2–Ta_2O_5 mixed layer capacitor stack is developed in Matlab. Model equations are based on the surface potential PSP model. After fitting the *C–V* characteristics in Matlab the model is coded in Verilog-A hardware description language and it is implemented as external library in Spectre circuit simulator within Cadence CAD system. The results are validated against the experimental measurements of the HfO_2–Ta_2O_5 stack structure.**

***Index Terms*—Device modeling, compact models, PSP, circuit simulation, high-k gate dielectric, Verilog-A, Spectre**

I. Introduction

THE semiconductors industry has been facing new challenges due to CMOS device downsizing. Linear scaling will not be possible in the future unless new materials are introduced in CMOS device structures or unless new device architectures are implemented. The strong association between devices and materials research is the key enabler here. The demand for low voltage, low power and high performance are the great challenges for the engineering of sub 45-nm gate length CMOS devices.

In this context device modeling is the milestone to efficiently implementing design objectives based on the new materials [1]. The scaling of classical bulk Si CMOS transistors approaches its physical limits. The SiO_2 gate dielectric thickness of a few atoms raises unwanted quantum effects such as electron tunneling and gate leakage currents that compromise the classic MOS transistor operation. To maintain the Moore's law progress in microelectronic technologies [2] it is needed to use new materials with higher dielectric constant (high-*k* materials) to replace the conventional SiO_2. The high-*k* gate dielectrics are also required for ensuring high-performance and low-power CMOS applications in the 45 nm technology node and beyond [3]. The emerging nanoelectronic transistors will rely on non-silicon high-*k* materials with target effective oxide thickness (EOT) of less than 10 Å to advance beyond the sub-20 nm regime [2], [4].

There are many high-*k* candidates being studied. Ionic metal oxides, having highly polarized metal-oxygen bonds, would have much larger *k* values than that of the covalent dielectric materials. Amongst those materials, Hf-based materials, such Hf silicates, Hf aluminates, have been considered as the most promising materials and have already been used in the state-of-the-art CMOS technology.

Promising high-*k* candidates for alternative gate dielectric materials are the multicomponent dielectrics based on a multiple metal oxides. Ta_2O_5 is best high-*k* candidate for storage capacitors of nanoscale DRAMs; HfO_2 appears to be the respective candidate for nanometer MOSFETs [4], [5], [6]. The electrical characteristics prove that the structure composed of HfO_2–Ta_2O_5 mixed layer on Si performs as a high-*k* layer in terms of permittivity, allowable level of leakage current, and appropriate oxide interface properties [7].

This paper presents a compact model for circuit simulation of the high-*k* MOS capacitor with HfO_2–Ta_2O_5 mixed layer structure from [8]. The electrical characteristics prove that the multicomponent structure composed of HfO_2–Ta_2O_5 mixed layer deposited on Si performs as high-*k* layer in terms of permittivity, allowable level of leakage current, and appropriate oxide interface properties [8]. The compact model is coded in Verilog-A HDL based on the PSP model equations. Capacitance-voltage (*C–V*) and current-voltage (*I–V*) characteristics are compared to the measurements to validate the model.

II. Surface Potential Modeling Approach

Compact device models need to be physical, simple (compact), accurate, and technology independent. Fitting of device data from different technologies across the industry with high accuracy is the most challenging task. The models are generally coded in circuit simulators using general-purpose languages. Accordingly, they are targeted specifically to the interface and internal data structures of their host simulator, and hence are inherently non-portable. In this context modification and optimization of a given model becomes a time-consuming and error-prone task.

An effective approach to obtain flexible modeling approach is to formulate open source code models in analog hardware description languages (HDLs) such as Verilog-A/AMS or VHDL-AMS. In the recent years Verilog-A has become increasingly viewed as most promising candidate for compact modeling purposes [9]. There are basically two types of compact models where model equations are directly derived from device physics. The first type of models is based on

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surface potential analysis – surface-potential based approach [8] (often called charge sheet models [10]). These models are inherently continuous in all regions of operation of the device. The current can be accurately determined using these models, but the equations themselves are complex, involving transcendental expressions, and often require iterations just to compute the surface potential for a given bias condition. They are thus not very suitable for VLSI circuit simulation, although recently they have been used for simulation of small circuits [11].

The second type of analytical models is the piece-wise modeling approach (also called regional approach or threshold-voltage based approach) the result of applying various approximations to the semiconductor equations, based upon decisions as to which physical phenomena dominate [12], [13]. Thus, different equations are required to represent different regions of operation of the device. A fundamental problem is the discontinuity of drain current characteristics which is solved by smoothing functions to interpolate the *I-V* characteristic between linear and saturation regions.

In this paper a compact model for circuit simulation of the high-*k* MOS capacitor HfO_2–Ta_2O_5 mixed layer structure presented in [7] is developed. The model is coded in Verilog-A HDL based on the PSP model core. Capacitance–voltage (*C–V*) characteristics are compared to the measurements to validate the model. The BSIM3v3 formulation of the model of this same HfO_2–Ta_2O_5 structure is described in [14].

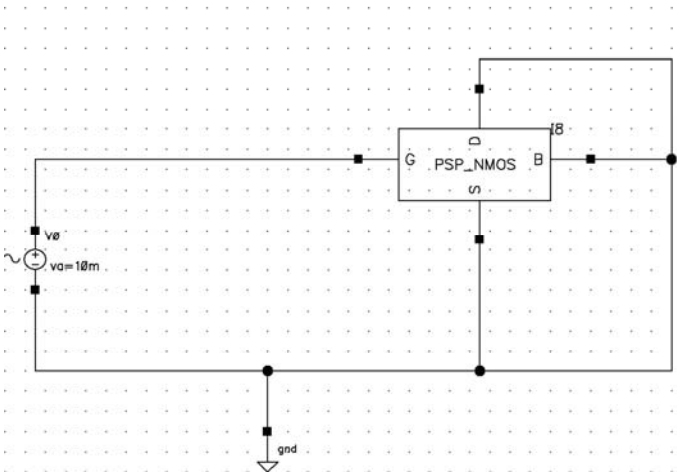

Fig. 1. Circuit for simulation of *C-V* and *I-V* characteristics of MOS capacitor. For the *C-V* characteristic V0 is a sine AC voltage source and for the *I-V* characteristic V0 is a DC voltage source.

III. Device Model Equations and Parameter Values

The test prototype structures for electrical measurements are MIS capacitors with a back side electrode of ~ 300 nm evaporated Al. The detailed characteristics of the modeled structure can be found in [7]. The capacitors are electrically characterized by means of *C–V* (Fig. 1) curves in the frequency range 50 kHz ÷ 100 kHz for minimizing the effects of parasitic series-parallel circuits [15].

C-V and *I-V* characteristics of the MOS capacitor are studied and the MOS capacitor is modeled based on PSP model equations in Verilog-A. The circuit in Fig. 1, created in Cadence Schematic editor, is used for the characterization process with channel length and width $L = W = 100$ μm.

A. Examination of the C-V Characteristic

C-V characteristics simulations are made at small signal with amplitude 10 mV, frequency 50 kHz and voltage sweep between -5 V to 5 V. All input parameters are left with their default values besides the channel length and width – their values are changed to $L = W = 100$ μm (cf. Fig. 2).

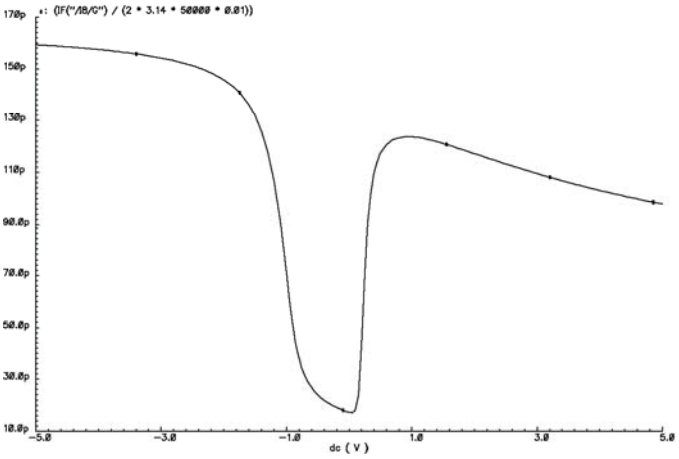

Fig. 2. *C-V* characteristics simulation of NMOS transistor at frequency 50 kHz and $L = W = 100$ μm; the rest of parameters are with their default values.

The simulations are done at 1 Hz and 1 MHz as well and no significant deviations from the characteristic in Fig 2 are observed.

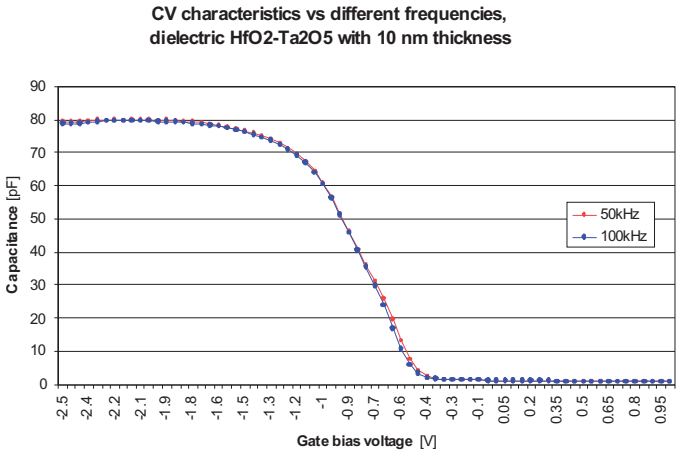

Fig. 3. *C–V* characteristics measured by RLC meter versus two frequencies across 10 nm HfO_2-Ta_2O_5 capacitor stack.

B. Examination of the I-V Characteristic

I-V characteristic simulations are performed at voltage sweep between -5 V to 5 V. Again all input parameters are with default values and $L = W = 100$ µm. Thus, we obtain zero value for the leakage current and hence *I-V* characteristic cannot be simulated with the default parameter values in the PSP model.

The preliminary examinations showed that the PSP model can be used with its default values for modeling the MOS capacitor and fitting *C-V* characteristics in the frequency range of 50 kHz ÷ 100 kHz (Fig. 3) for minimizing the effects of parasitic series-parallel circuits [15].

C. Parameter Extraction

The modeled high-*k* dielectric capacitor stack has parameters which are directly measured after its fabrication – gate area defined by width *W* and length *L*, and type of substrate conductivity (acceptor or donor). These parameters are typical design inputs which can be changed depending on the requirements of the layout.

Other parameters needed for the model are: relative permittivity of the dielectric, dielectric thickness, substrate doping concentration and flat band voltage. These parameters are technology dependent inputs for model adaptation which are not changed during layout design. Their values are summarized in Table I and they are determined either by direct measurements or by extraction based on the characterization *C-V* curves.

TABLE I
SUMMARY OF PRELIMINARY MEASURED OR EXTRACTED TECHNOLOGY PARAMETERS

Parameter	Value	Dimension
Relative dielectric permittivity – ε_{rox}	9	dimensionless
Substrate doping concentration – N_{sub}	$1.25 \cdot 10^{21}$	[m^{-3}]
Flat band voltage – V_{FB}	-0.55	[V]
Dielectric thickness – t_{ox}	10	[nm]

In order to determine the flat band voltage V_{FB} we have to keep in mind that the MOS capacitor stack is a combination of capacitances C_{sub} and C_{ox} connected in series; C_{ox} is not dependent on applied voltage while C_{sub} depends on it and changes in depletion and inversion modes. Hence, the equivalent capacitance at flat band voltage is

$$C'_{FB} = \frac{C'_{FBS} C'_{ox}}{C'_{FBS} + C'_{ox}} \quad (1)$$

where

$C'_{ox} = \frac{\varepsilon_{ox}}{t_{xo}}$ – specific capacitance of gate oxide; ε_{ox} – dielectric constant of oxide, t_{ox} – oxide thickness

$C'_{FBS} = \frac{\varepsilon_{Si}}{\lambda_p}$ – specific capacitance of *p*-substrate at V_{FB}, ε_{Si} – dielectric constant of silicon,

$\lambda_p = \sqrt{\frac{\varepsilon_{Si} kT}{q^2 N_{sub}}}$ – Debye length for *p*-type semiconductor

These formulas do not take into account dielectric charge, differences in work functions of Si/dielectric and dielectric/gate electrode, non-uniform concentration of impurities in the bulk.

After calculating the values of λ_p, C'_{ox} and C'_{FBS} we obtain for $C_{FB} = C'_{FBWL} \approx 8.2$ pF. Now the flatband voltage can be interpolated from the measurement data : $V_{FB}^{theory} \approx -0.51$ V (Fig. 4).

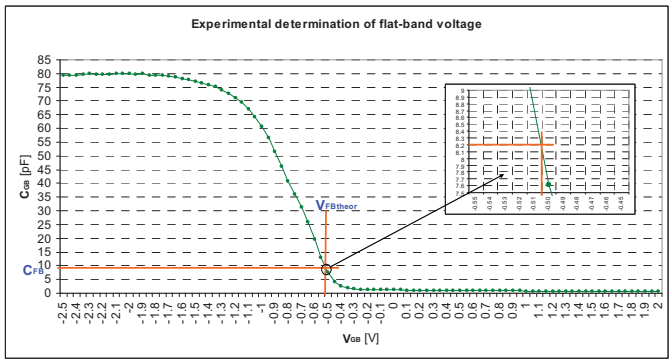

Fig. 4. Flatband voltage V_{FB} is interpolated from the *C-V* measurements and the calculated flatband capacitance C_{FB}.

D. PSP Model Simplification to Model the High-k Structure

The objective of our MOS capacitor compact model is to enable simulation of the high-*k* MOS device using different design and technology parameters keeping model equations as simple as possible while giving highly accurate results. A model meeting the above requirements was already developed in [14] based on the BSIM3v3 core which is one of the most well-known regional models. It describes different operating regions with different equations.

Here we are focusing on development of a compact model based on the surface-potential approach proceeding from PSP model equations that inherently possess continuous *I-V* characteristics. In this approach the equations are explicit functions of the surface potential ϕ_s instead of the applied voltage and as a result they are continuous for all bias conditions [16]. The main disadvantage is the requirement of separate iterative procedure for calculation of the surface potential ϕ_s as function of the applied voltage. In this model the iterative procedure is replaced with regional approach that incorporates all significant effects into the surface potential description.

Below we will simplify the PSP model to adapt for describing the high-k dielectric stack. Thus we will exclude the complex formulas for effects that do not correspond to the technological nature of the modeled structure and effects that have negligible impact over *C-V* characteristic. In particular we exclude the following parts of the PSP model: 1) polysilicon depletion, 2) quantum corrections and 3) geometry scaling. The influence of each of these effects is shown in Fig. 5.

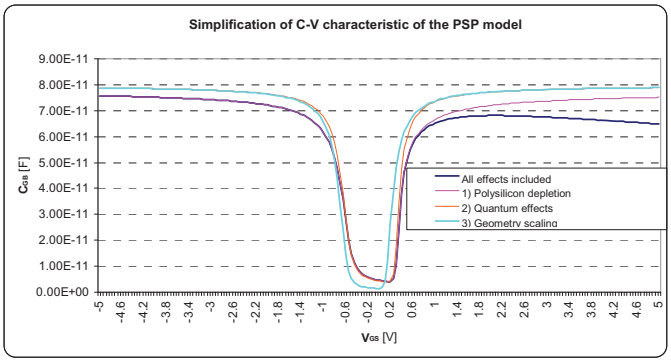

Fig. 5. Simplified C-V characteristics after exclusion of 1) polysilicon depletion, 2) quantum corrections and 3) geometry scaling; input parameters $L = W = 100$ µm, $\varepsilon_{ox} = 9$, $N_{sub}=1.25\times10^{21}$ m^{-3}; $V_{FB}= -0.51$ V.

The analysis of the PSP model [17] and the stack structure [7] shows that the high-*k* stack capacitance is described by the equation for the gate-substrate charge: $I_g = dQ_g/dt$. After simplifying the original PSP equations the intrinsic charge at the gate is expressed with the product of the oxide capacitance C_{ox} and the mid-point voltage V_{oxm}:

$$Q_g = C_{ox} V_{oxm} \tag{2}$$

$$C_{ox} = (\varepsilon_{rox}\varepsilon_o WL)/t_{ox} \tag{3}$$

$$V_{oxm} = \phi_T . x_{gm} \tag{4}$$

where $\phi_T = kT/q$ is the temperature potential and x_{gm} is a variable which depends on the surface potential described by the following expressions:

$$x_{gm} = G.\sqrt{D_m + P_m} \tag{5}$$

$$D_m = [1/E_s - x_s - 1 - \chi(x_s)]\Delta_{ns} \tag{6}$$

$$P_m = x_s - 1 + E_s \tag{7}$$

In equations (6) and (7) x_s is dimensionless potential at the silicon substrate surface which is computed from the temperature and real surface ϕ_s potentials:

$$x_s = \phi_s / \phi_T \tag{8}$$

The parameter G is calculated from the body effect coefficient γ:

$$G = \gamma / \sqrt{\phi_T} \tag{9}$$

where $\gamma = \sqrt{2.q.\varepsilon_{Si}.N_{sub}}\,/\,C'_{ox}$. The parameter $C'_{ox}=(\varepsilon_{rox}\,\varepsilon_0)\,/\,t_{ox}$ is the oxide capacitance per unit gate area.

The variables E_s and $\chi(x_s)$ are functions of the surface potential:

$$E_s = \exp(-x_s) \tag{10}$$

$$\chi(x_s) = x_s^2 / \left(2 + x_s^2\right) \tag{11}$$

The variable Δ_{ns} is in exponential dependence from the dimensionless bulk potential deep in the silicon substrate $x_{ns} = \phi_B/\phi_T$:

$$\Delta_{ns} = \exp(-x_{ns}) \tag{12}$$

Equations (2) ÷ (12) show the modeled charge is explicit function only of the surface potential and it is already described with same formulas for all bias operation regions.

However, the surface potential is not described continuously even in the PSP model. It is split into two regions separated by the marginal dimensionless band bending parameter x_{mrg} calculated from the body effect coefficient:

$$x_{mrg} = 10^{-5}\left(1 + G/\sqrt{2}\right) \tag{13}$$

The dimensionless band bending caused by the bias voltage is:

$$x_g = (V_{GB} - V_{FB} - ST_{V_{FB}}\Delta T)/\phi_T \tag{14}$$

The parameter ST_{VFB} is the temperature coefficient of the flat band voltage and ΔT is the temperature difference from the nominal temperature (21 °C).

The surface potential is described in two regions:

- *Accumulation and depletion when* $x_g < x_{mrg}$

$$x_s = A_1\eta + a.\tau/(a + c) \tag{15}$$

$$\tau = -A_2\eta + A_3 \ln\left(a/G^2\right) \tag{16}$$

$$a = (-x_g - \eta)^2 \text{ and } c = 2(-x_g - \eta) \tag{17}$$

$$\eta = \left(z + 10 - \sqrt{(z-6)^2 + 64}\right)/2 \tag{18}$$

$$z = -1.25x_g / \xi \tag{19}$$

In (15) and (16) A_1, A_2, A_3 are fitting parameters.

- *Inversion and depletion when* $x_g \geq x_{mrg}$

$$x_s = B_1\eta + a.\tau/(a+c) \tag{20}$$

$$\tau = x_{ns} - \eta + B_2 \ln\left(a/G^2\right) \tag{21}$$

$$\eta = \left(x_g + b_x - \sqrt{(x_g - b_x)^2 + 5}\right)/2 \tag{22}$$

$$b_x = x_{ns} + 3 \tag{23}$$

In (20) and (21) B_1 and B_2 are fitting parameters. For the variables a and c are used expressions (17).

After the above described simplification the model is coded in Matlab where it can be easily fitted. Its validity is demonstrated by comparison between the *C-V* characteristics obtained from Cadence Spectre simulator and Matlab (in Cadence Spectre the model is input as Verilog-A code). The differences are negligible and are due to the different algorithms for differentiating.

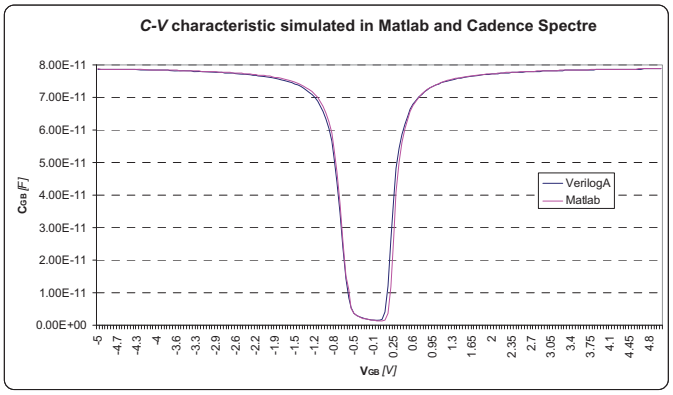

Fig. 6. Simplified *C-V* characteristics after exclusion of 1) polysilicon depletion, 2) quantum corrections and 3) geometry scaling; input parameters $L = W = 100$ µm, $\varepsilon_{ox} = 9$, N_{sub}=1.25×10^{21} m^{-3}; V_{FB}= –0.51 V.

IV. Simulation and Fitting

Model fitting starts with finding an optimal value for the flatband voltage V_{FB} at which the integral error is minimal. After several iterations it found that V_{FB} = –0.55 V.

The above model equations are coded in Matlab. Equations (15), (16), (20), (21) are simplified PSP equations in which the fitting non-physical variables A_1, A_2, A_3, B_1 and B_2 are introduced. The need for further fitting of these variables arises after comparing measurements versus simulation results at $A_1 = A_2 = A_3 = B_1 = B_2 = 1$ (Fig. 7).

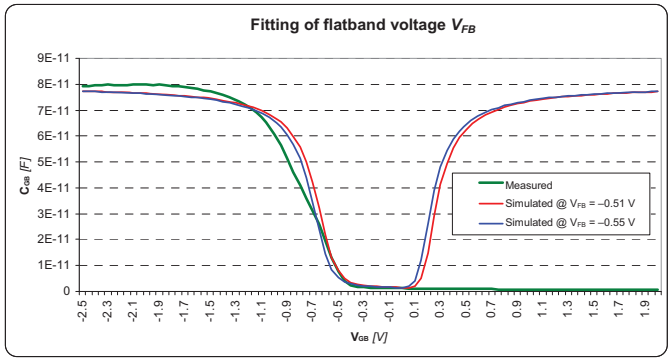

Fig. 7. Simulations at different V_{FB} for fitting purposes.

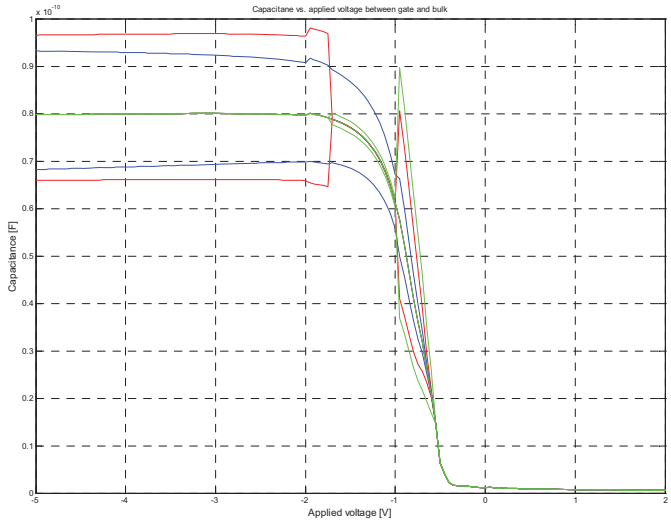

Fig. 8. Fitting *C-V* curves by changing variables A1 (green), A2 (red) and A3 (blue) in accumulation and depletion regions.

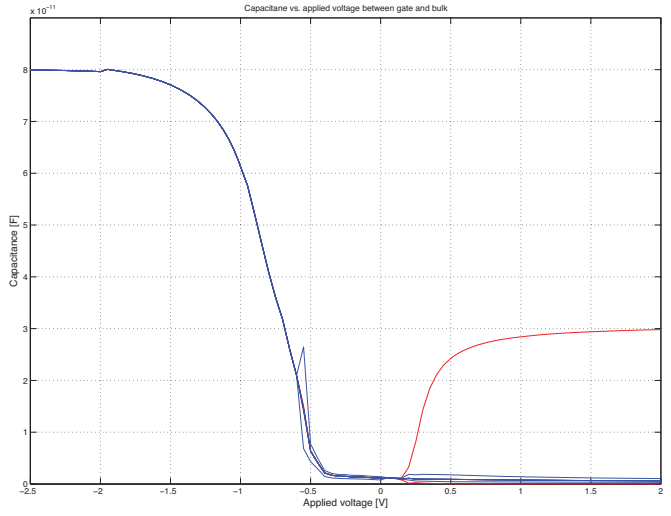

Fig. 9. Fitting *C-V* curves by changing variables B_1 (blue) and B_2 (red) in inversion and depletion regions.

The surface potential is considered in two regions: $x_g < x_{mrg}$ and $x_g \geq x_{mrg}$. Both regions are additionally split into smaller pieces where different effects are dominant over different parts of the curve. In Figures 8 and 9 it is observed how the MOS capacitor characteristics are changed after applying the piece-wise fitting of the variables.

The performed additional split enables further easy adjustment of the surface potential so that the integral error of the mismatch between the simulations and measurements curves is calculated to be below a certain maximum of e.g. 3% (which is below the measurements' error). The outcomes from fitting of the variables within the entire bias range are given in the lookup Table II. The achieved matching between the model and the experimental data is presented in Fig. 10.

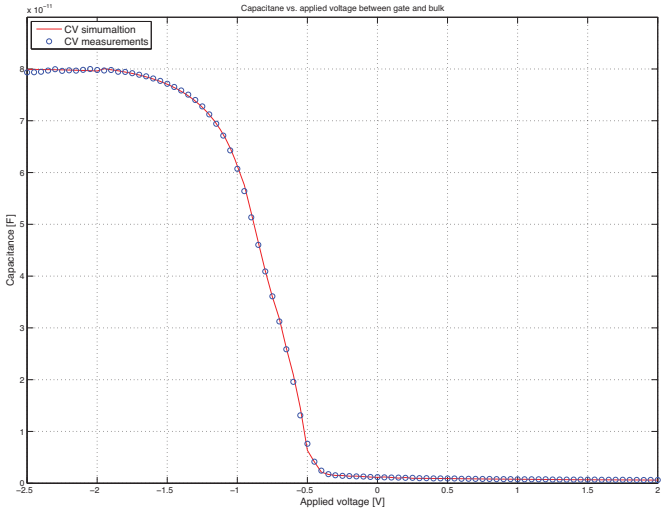

Fig. 10. Plot of *C-V* simulation compared to experimental data after fitting. Highly accurate matching is achieved.

TABLE II
LOOKUP TABLE OF THE FITTING VARIABLES A_1, A_2, A_3, B_1 AND B_2

Parameters Bias Voltage Range [V]	A_1	A_2	A_3	B_1	B_2
$< (V_{FB} - 2.0)$	1	0.955	0.979	1.7	0.5
$(V_{FB} - 2.0) \div (V_{FB} - 1.75)$	1	1.022	1.02	1.7	0.5
$(V_{FB} - 1.75) \div (V_{FB} - 1.0)$	0.04	0.002	0.987	1.7	0.5
$(V_{FB} - 1.0) \div (V_{FB} - 0.65)$	1.15	1.84	1.5	1.7	0.5
$(V_{FB} - 0.65) \div (V_{FB} - 0.5)$	1.3	1.94	1.5	1.7	0.5
$(V_{FB} - 0.5) \div (V_{FB} - 0.45)$	1.3	1.94	1.5	1.5	0.5
$(V_{FB} - 0.45) \div (V_{FB} - 0.4)$	1.3	1.94	1.5	0.6	0.5
$(V_{FB} - 0.4) \div (V_{FB} - 0.3)$	1.3	1.94	1.5	0.5	0.5
$(V_{FB} - 0.3) \div (V_{FB} - 0.2)$	1.3	1.94	1.5	0.6	0.5
$(V_{FB} - 0.2) \div (V_{FB} - 0.0)$	1.3	1.94	1.5	0.7	0.5
$(V_{FB} - 0.0) \div (V_{FB} + 0.15)$	1.3	1.94	1.5	0.9	0.5
$(V_{FB} + 0.15) \div (V_{FB} + 0.25)$	1.3	1.94	1.5	0.938	0.5
$> (V_{FB} + 0.25)$	1.3	1.94	1.5	0.94	0.5

Essential part of the model is the surface potential ϕ_s and its function of the applied voltage is plotted in Fig. 11. The abstract description of the surface potential is very important because it is developed together with the technology of the researched high-*k* MOS devices.

To perform the circuit simulations, the Matlab code was recoded in Verilog-A in order to input it to Spectre circuit simulator as an external model. The existing MOSFET in Cadence design kit can be simulated as MOS capacitor if the source, bulk, and drain nodes are connected together as described in [16]. The *C–V* characteristics are simulated in AC mode by plotting the capacitance as a calculation based on the amplitude of the current through the gate node for a frequency of 50 kHz. The input voltage is sinusoidal with fixed small signal amplitude of 10 mV and DC voltage sweep between –5 V ÷ +5 V.

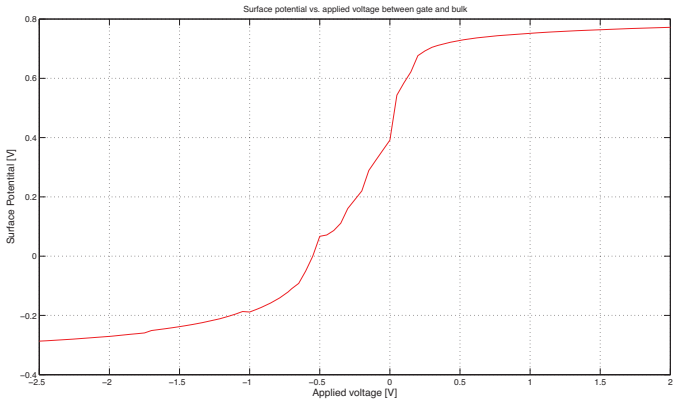

Fig. 11. Plot of the surface potential versus the applied voltage. This function is technology dependant.

Simulations with the developed model can be run well beyond the bias range (–2.5 ; 2.5) V for which we have experimental data. Outside this range the device behavior follows the natural asymptotic expectations. This is proven with parametric simulations within twice extended range (–5 ; 5) V using the dielectric thickness for parameter. The simulation plots in Fig. 12 validate the model by confirming the proper asymptotic behavior.

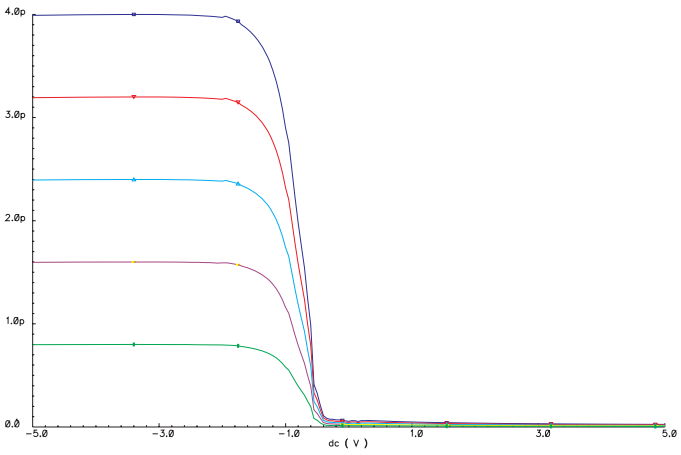

Fig. 12. Plots of parametric *C-V* simulations for different values of dielectric thickness in extended bias range. The model behaves naturally as expected.

V. VERILOG-A CODE

Below we list an excerpt of the Verilog-A code of our model showing the computation of the surface potential and the continuous description of the intrinsic charge.

```
//Surface potential expressions
if (xg < -margin) begin
//accumulation and depletion reqions
SP_S_ysub  = -1.25 * xg * inv_xi;
SP_S_eta   = 0.5 * (SP_S_ysub + 10 -
               pow(((SP_S_ysub - 6.0) *
               (SP_S_ysub - 6.0) + 64.0),0.5));
SP_S_temp   = -xg - SP_S_eta;
SP_S_a    = SP_S_temp * SP_S_temp;
SP_S_c      = 2.0 * SP_S_temp;
if(Vgs<(-2.0+VFBO+0.55)) begin
SP_S_tau = -0.955*SP_S_eta +
            0.979*ln(SP_S_a * inv_G02);
end
if((Vgs>=(-2.0+VFBO+0.55))&&(Vgs < (-1.75 + VFBO +
       0.55))) begin
SP_S_tau    = -1.022*SP_S_eta + 1.02 *
               ln(SP_S_a * inv_G02);
end
if((Vgs>=(-1.75+VFBO+0.55))&&(Vgs < (-1.0 + VFBO +
       0.55))) begin
SP_S_tau    = -0.002 * SP_S_eta + 0.9875 *
               ln(SP_S_a * inv_G02);
end
if((Vgs>=(-1.0+VFBO+0.55))&&(Vgs < (-0.65 + VFBO +
       0.55))) begin
SP_S_tau    = -1.84*SP_S_eta + 1.5*ln(SP_S_a *
               inv_G02);
end
if(Vgs>=(-0.65 + VFBO + 0.55)) begin
SP_S_tau    = -1.94*SP_S_eta + 1.5*ln(SP_S_a *
               inv_G02);
end
nu    =  SP_S_a + SP_S_c;
x_s   =  -(SP_S_eta +SP_S_a * SP_S_tau / nu);
if((Vgs>=(-1.75 + VFBO + 0.55))&&(Vgs < (-1.0 +
       VFBO + 0.55))) begin
x_s   =  -(0.04*SP_S_eta + SP_S_a * SP_S_tau/nu);
end
if((Vgs>=(-1.0 + VFBO + 0.55))&&(Vgs < (-0.65 +
       VFBO + 0.55))) begin
x_s   =  -(1.15*SP_S_eta + SP_S_a * SP_S_tau/nu);
end
if(Vgs>=(-0.65 + VFBO + 0.55)) begin
x_s   =  -(1.3*SP_S_eta + SP_S_a * SP_S_tau/nu);
end
end
else begin
//inversion and depletion regions
SP_S_bx   = xn_s + 3.0;
SP_S_eta  = 0.5*(xg + SP_S_bx - pow(((xg -
              SP_S_bx)*(xg - SP_S_bx)+(5.0)),0.5));
SP_S_temp = xg - SP_S_eta;
SP_S_a    = SP_S_temp * SP_S_temp;
SP_S_c    = 2.0 * SP_S_temp;
SP_S_tau  = xn_s - SP_S_eta + 0.5*ln(SP_S_a/G02);
nu        = SP_S_a + SP_S_c;
if(Vgs<(-0.5+VFBO+0.55)) begin
x_s  =  1.7*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>=(-0.5 + VFBO + 0.55)) begin
x_s  =  1.5*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>(-0.45 + VFBO + 0.55)) begin
x_s  =  0.6*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>(-0.4 + VFBO + 0.55)) begin
x_s  =  0.5*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>(-0.3 + VFBO + 0.55)) begin
x_s  =  0.6*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>(-0.2 + VFBO + 0.55)) begin
x_s =  0.7*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>(VFBO + 0.55)) begin
x_s =  0.92*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>(0.15 + VFBO + 0.55)) begin
x_s =  0.938*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
if(Vgs>(0.25 + VFBO + 0.55)) begin
x_s =  0.94*SP_S_eta + SP_S_a * SP_S_tau / nu;
end
end
//Calculation of the intrinsic charge//
temp      =  1.0 / (2.0 + x_s * x_s);
xi0s      =  x_s * x_s * temp;
delta_1s  = exp(x_s);
Es        =  1.0 / delta_1s;
delta_1s  =  delta_ns * delta_1s;
Dm   = delta_1s - delta_ns * (x_s + 1.0 + xi0s);
Pm   =  x_s - 1.0 + Es;
Xgm  =  G0 * pow((Dm + Pm),0.5);
Voxm =  xgm * phit;
COX  = `EPSO * EPSROXO * W * L / TOXO;
Qg   =  Voxm * COX;
```

VI. CONCLUSION

The MOS capacitor behavior of high-k HfO_2-Ta_2O_5 layer stack was studied proceeding from the surface potential description embedded in the intrinsic charge PSP model. For fitting purposes the model is coded first in Matlab where the curves are fitted to the experimental data published in [7] with high accuracy – below 3% error. The curves also meet the natural asymptotic expectations. The optimized code was then programmed in Verilog-A to integrate with the Spectre simulator of Cadence Design Framework CAD tool.

In addition to the simulation results themselves the model realization represents a flexible and straightforward approach for adaptation and development of compact model equations in a portable, open-source environment applicable to various simulation platforms.

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REFERENCES

[1] G. Angelov, T. Takov, and St. Ristiç "MOSFET Models at the Edge of 100-nm Sizes", *Proc. of the 24th Intl. Conf. on Microelectronics (MIEL 2004)*, Niš, Serbia and Montenegro, Vol. 1, pp. 295-298, 2004.

[2] The International Technology Roadmap for Semiconductors: http://www.itrs.net

[3] R. Chau et. al. "Application of High-k Dielectrics and Metal Gate Electrodes to Enable Silicon and Non-Silicon Logic Nanotechnology", *Microelectronic Engineering*, Vol.80, pp. 1-6, 2005.

[4] G. D.Wilk, R. M.Wallace, and J. M. Anthony, "High-k Gate Dielectrics: Current Status and Materials Properties Considerations," *J. Appl. Phys.*, Vol. 89, pp. 5243–5275, 2001.

[5] M. Houssa, ed., "*High-k Gate Dielectrics*", Institute of Physics Publishing, Bristol and Philadelphia, 2004. ISBN 0-7503-0906-7.

[6] E. Atanassova and A. Paskaleva, "Challenges of Ta_2O_5 as high-k dielectric for nanoscale DRAMs", *Microelectronics Reliability* 47(6), pp. 913-923, 2007.

[7] E. Atanassova, M. Georgieva, D. Spassov, and A. Paskaleva, "High-k HfO_2-Ta_2O_5 mixed layers: Electrical characteristics and mechanisms of conductivity", *Microel. Engin*. **87**, pp. 668-676, 2010.

[8] G. Angelov, T. Takov, and St. Ristic "MOSFET Models at the Edge of 100-nm Sizes", *Proc. 24th Intl. Conf. on Microelectronics (MIEL)*, Niš, Serbia & Montenegro, Vol. 1, pp. 295-298, May 2004.

[9] M. Mierzwinski, P. O'Halloran, B. Troyanovsky, R. Dutton, "Changing the paradigm for compact model integration in circuit simulators using Verilog-A", *Technical Proceedings of the 2003 Nanotechnology Conference and Trade Show (Nanotech 2003)*, Vol. 2, February 2003, pp. 376–379.

[10] J. R. Brews, "Physics of the MOS transistor," in *Silicon Integrated Circuits*, D. Kahng, Ed. New York: Academic Press, 1981, vol. Supplement 2A, pp. 1-120, Applied Solid-state Science Series.S.M. Sze, "*Physics of Semiconductor Devices*", Wiley, 1981.

[11] A. R. Boothroyd, S. W. Tarasewicz, and C. Slaby, "MISNAN-A physically basedcontinuous MOSFET model for CAD applications," *IEEE Trans. Compter-Aided Design*, vol. CAD-10, pp. 1512-1529, 1991.

[12] P. Antognetti and G. Massobrio, *Semiconductor Device Modeling with SPICE*. New York: McGraw-Hill Book Company, 1988.

[13] H. C. de Graaff and F. M. Klaassen, *Compact Transistor Modelling for Circuit Design*. Wien, New York: Springer-Verlag, 1990.

[14] G. Angelov, N. Bonev, R. Rusev, M. Hristov, A. Paskaleva, D. Spassov, "Verilog-A Model of a High-k HfO_2-Ta_2O_5 Capacitor", *Proc. of 18th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES2011)*, pp. 470-475, Gliwice, Poland, June 16-18, 2011. ISBN 978-83-932075-0-3.

[15] K. J. Yang, C. Hu, "MOS Capacitance Measurements for High-Leakage Thin Dielectrics", *IEEE Transactions on Electron Devices*, Vol. 46, No. 7, July 1999.

[16] G. Gildenblat, X. Li, W.Wu, H. Wang, A. Jha, R. van Langevelde, G.D.J. Smit, A.J. Scholten and D.B.M. Klaassen, "PSP: An Advanced Surface-Potential-Based MOSFET Model for Circuit Simulation ", *IEEE Transactions on Electron Devices*, Vol. 53, No. 9, pp. 1979-1993, September 2006.

[17] 2Li X. Li, W. Wu, G. Gildenblat, G.D.J. Smit, A.J. Scholten, and D.B.M. Klaassen, "PSP 103.0", NXP Semiconductors and Arizona State University 2009

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