FMC Video Acquisition Module with Camera Link Interface

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***Abstract*—The paper describes an universal module for video stream acquisition from fast cameras with Camera Link interface. The first version of the referenced standard defines three configurations: Base, Medium and Full. The developed module supports all of them achieving transmission speeds up to 5.44 Gb/s for raw image data in the Full configuration.**

The module is designed according to FPGA Mezzanine Card (FMC) standard and can cooperate with carrier boards containing High-Pin Count (HPC) version of the connector. The module was tested with the TEWS TAMC-641 module.

***Index Terms*—frame grabber, fast camera, Camera Link, image acquisition, video acquisition, FMC module**

I. Introduction

A. Motivation

THE authors have in the past developed system for video acquisition in the μTCA architecture [1]. The earlier solution was assembled using only COTS (Commercial Off-The-Shelf) components, including dedicated frame grabber (FG) module with Camera Link interface. The chosen frame grabber, shown in the Figure 1, was built with use of a single FPGA circuit.

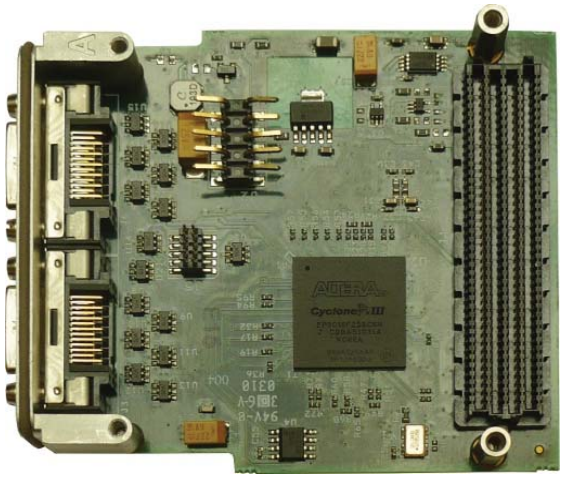

Figure 1. The original frame grabber module

The data were first deserialized, then synchronized to locally generated 86 MHz clock, next the channels were aligned and finally serialized again to fit the capabilities of FMC Low-Pin Count connector. The evaluation indicated that the FG module is unable to operate properly with pixel clock above 70 MHz while the requirement was to acquire data at 85 MHz. The errors introduced by the faulty module were much darker pixels (with the most significant bit cleared) occurring after transition from pixel intensity below 0x40 to intensity over the level of 0x40. The distortions are best illustrated with the camera test image shown in Figure 2. The analogous problems were also visible when the camera displayed images acquired from its sensor.

Figure 2. Camera test image with errors

The problems are also plainly visible in the waveforms captured using ChipScope Pro analyzer, illustrated in Figure 3 on the following page. Moreover, the module again provides the serialized data and receiving them requires similar firmware complexity as deserializing the original Camera Link stream. To receive the data from the mentioned FG module the module is required to have 8:1 deserializers running at the 688 MHz clock. This renders popular Virtex-5 family of FPGA devices not suitable for this task – newer, and more expensive, FPGAs are required. Finally, the module were equipped with programming connector for IDC cable, that was so high that it made dents in the carrier board.

To resolve these issues the new, much simpler, FMC frame grabber module was developed.

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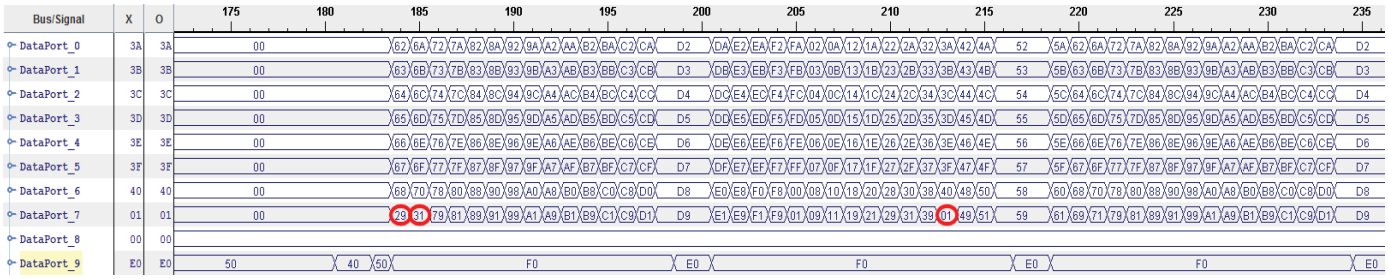

Figure 3. ChipScope window with transmission errors marked

B. High-Speed Video Acquisition

Two types of high-speed cameras are currently in popular use. First type captures the image stream to a local RAM memory and then provides the data over common interfaces, like Gigabit Ethernet or USB. This type of camera is generally easy to connect to a computing system because the standard communication interfaces are usually sufficient.

The second type of high-speed cameras stream the video live using continuous high throughput transmission. In these devices a strong emphasis is placed on achieving the smallest possible latency. This case of video acquisition is much more challenging as the single camera can easily generate several gigabits of image data per second. Such cameras are well suited for real-time applications and are often used in machine vision systems. The most popular communication standards for real-time raw video streaming are:

- GigE Vision (up to 1 Gb/s)
- IEEE 1394 (up to 3.4 Gb/s)
- USB 3.0 (up to 5 Gb/s)
- Camera Link (up to 6.8 Gb/s)

There is also an emerging competing standard, named CoaXPress [2], allowing for transmissions up to 25 Gb/s. Although the specification is very promising, its adoption is still at a very early stage. The Camera Link standard is hence the common choice for the top-notch video cameras.

C. Camera Link Standard

What differentiates the Camera Link standard from the others listed is the extremely simple protocol encapsulating the legacy parallel data channels. The Camera Link Standard Specification 1.0 defines up to three serial data channels (Channel Link interfaces) composed of reference clock signal and four data signals, all in the LVDS standard.

The large number of communication lines required to implement this standard is probably its most important drawback. Connecting the Medium or Full speed camera requires two thick cables, see Figure 4. Moreover the cables are identical and may be swapped easily.

The data serialization ratio is 1:7 hence one channel can carry up to 2.38 Gb/s at reference clock of 85 MHz. The theoretical bandwidth of the full interface, composed of three channels, is then 7.12 Gb/s [3]. Accounting for unused and synchronization signals, the full link can reach up to 5.44 Gb/s for plain pixel data (6.8 Gb/s when counting also the synchronization flags). Proper clock recovery, deserialization and synchronization of channels are not very complicated but challenging tasks. Fortunately the first two operations can be performed easily and reliably using a dedicated chipset. The only task that remains to be done in the data receiver is to synchronize data from three Channel Link lanes.

Figure 4. Camera Link to Mini Camera Link cable

II. Hardware Design

Each of the data transmission lines carries data with bit rate reaching almost 600 Mb/s. Twelve such a lines have to be routed to the dedicated deserializer circuits. The tracks have to be well equalized and tuned to avoid the phase skew. The low-noise continuous reference planes for the data signals and clocks are required. The DS90CR288A form Texas Instruments is a single-chip Channel Link receiver. It provides the module with the most important components: the PLL and deserializer block. The built-in loop attenuates the clock jitter and provides a 595 MHz clock for data deserialization. Each deserializer drives 28 LVCMOS data lines and provides a slow clock signal for synchronization (up to 85 MHz). The recovered signals are converted to LVDS and provided to the FMC connector.

The FMC-HPC connector offers 80 differential pairs for general purpose use, four pairs dedicated for associated clocks and a number of gigabit links with reference clock [4]. Passing just the data lines from all three deserializers would require 84 differential pairs, hence signals defined by the Camera Link standard as unused were stripped. A total number of 76 data pairs are implemented. The remaining 4 pairs of the connector are used for serial communication with the camera, driving four Camera Control signals and two LEDs. The 3 out of 4 general purpose clock lines were also used, one for every deserializer. The module block diagram is depicted in the Figure 5.

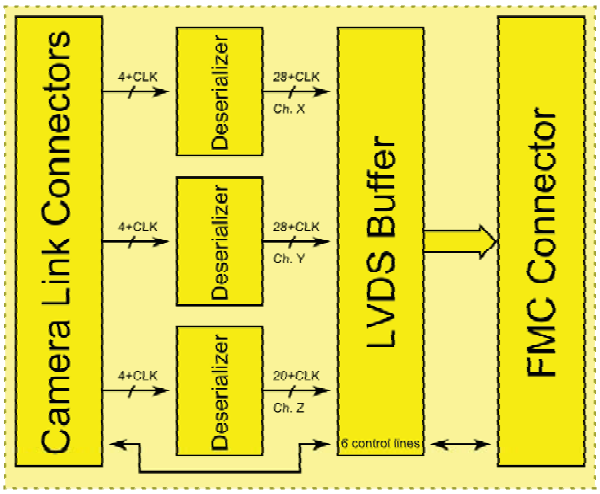

Figure 5. Device block diagram

Although the module is rather simple, the PCB layout makes use of 6 conductive layers. The number of layers is determined mainly by the cautious escape routing provided for differential pairs near the Mini Camera Link connectors. Three of layers are dedicated for 100 Ω differential pairs routing and another three layers are used for power supply and reference planes for the high-speed signals.

The only difficult process in manufacturing of the module was proper soldering of the large FMC connector. The assembled module is shown in the Figure 6.

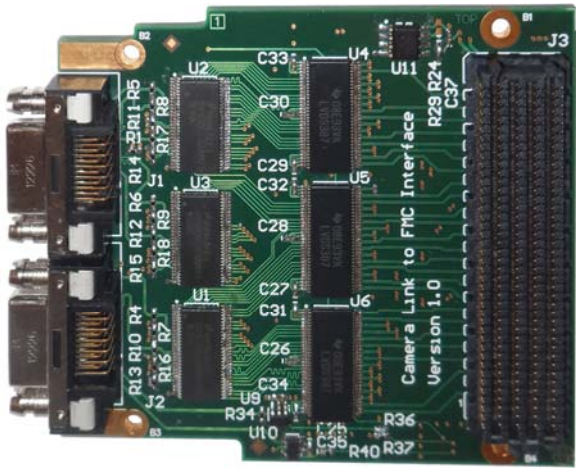

Figure 6. The developed frame grabber module

III. Receiving Firmware

All the three Channel Links are feed from the same data source and are using the same clock, nevertheless at the receiver side large phase differences between channels may occur. The data sink has to ensure proper synchronization between channels. This may be accomplished by aligning the start of frame markers of each channel.

In the proposed implementation, see Figure 7, the data from the deserializers are first stored in short FIFO queues for synchronization with local 100 MHz clock. When the queue reports new data available it is immediately read and provided to Start Of Frame (SOF) detector (labeled 'Det'). As the maximum clock frequency originating from the deserializers is 85 MHz, hence the first stage FIFO queues are required to have the depth of just a few words. If the flags indicate that the data are valid, the payload bytes together with SOF mark are stored in the second stage FIFO queues.

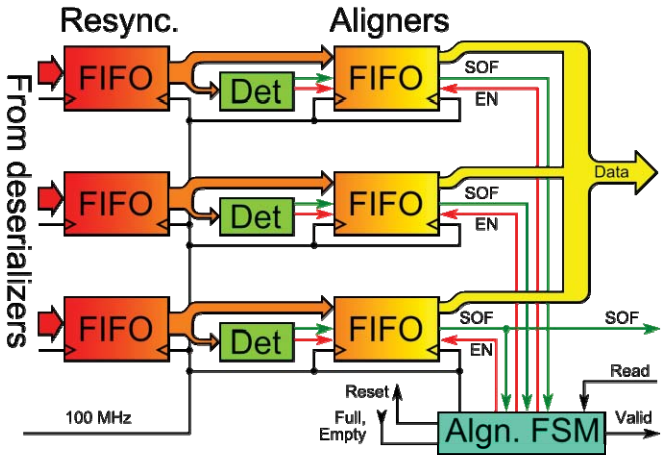

Figure 7. The FPGA interface to frame grabber module

After successful synchronization, when all the queues outputted SOF marker, the validity flag is asserted and the data is provided for higher-level firmware. From now all the queues are read simultaneously. The valid flag is deasserted if any of the FIFOs is empty. The arrival of further SOF markers is monitored. In case of alignment failure the synchronization process is repeated.

To achieve proper clock-to-data relation an input delay blocks (IDELAY) were instantiated. Moreover, to ensure predictable timing, the registers were packed into the I/O Blocks of the FPGA device.

IV. Module Evaluation

For evaluation purposes the developed Camera Link to FMC interface was hosted by the commercial AMC carrier module from TEWS Technologies, the TAMC-641. The module has the High-Pin Count FMC connector, Virtex-5 FPGA, a set of memories, clocking circuit and a number of communication links.

During the initial module startup attempts the carrier board was not activating the FMC module. The problem was found to be related to the power good (PG) signaling. The FMC module waited for PG signal from carrier and the carrier waited for the PG signal from FMC. Reconfiguration of resistor jumpers on the daughter module solved the problem.

The output from the described synchronizer was first observed using ChipScope Pro analyzer to prove its correct operation at the lowest level. No errors were observed even for pixel clock up to the maximum of 85 MHz. The captured waveforms are illustrated in Figure 8. The differences between both screenshots are expected and are caused by using different synchronization method and other ratio of readout frequency to pixel clock frequency.

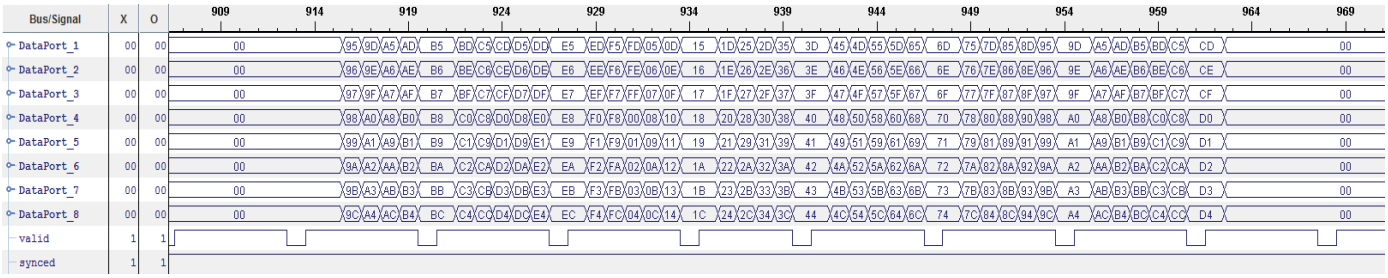

Figure 8. Data acquisition with no errors present

The authors are now working on prototype of Image Acquisition System utilizing the described module. The first video sequences captured indicate that both the module and synchronizer IP-core acquire the video data properly. The camera test images collected using new module, shown in Figure 9, contain no errors. The actual video stream is now also received correctly.

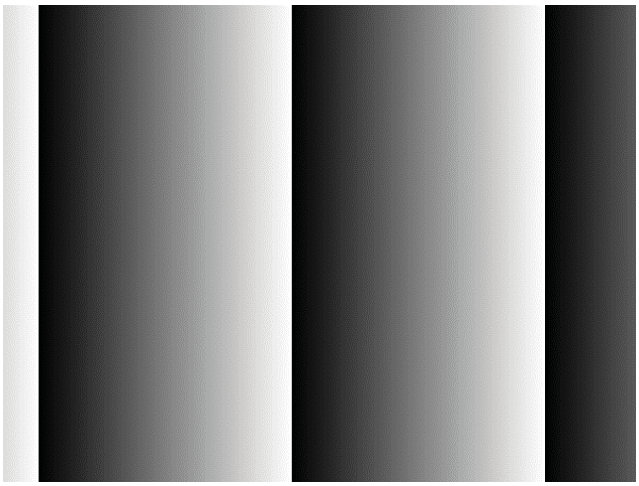

Figure 9. The camera test image captured with new module

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