Analysis of a Simple Method of CMOS IC Design for Yield Optimization

Daniel Tomaszewski, and Marat Yakupov

Abstract—**A simple approach for CMOS integrated circuit (IC) design taking into account a process variability and oriented towards optimization of a parametric yield has been presented. Its concept is based on cumulative distribution functions of random variables representing IC performances subject to process variations. In the method it has been assumed that CMOS process statistical data are expressed in terms of so-called process parameter distributions. Thus the design centering is done via layout parameter tuning. The approach relies on maximizing the probability that random variables corresponding to IC performances remain within the performance boundaries. Also, a methodology for statistical characterization of CMOS process has been briefly described. Finally, the method operation has been illustrated using analytical and SPICE models of CMOS inverter, operational amplifier and ring oscillator**

Index Terms—**CMOS, design centering, design for yield, probability density function, cumulative distribution function, statistical modeling, BPV method, SPICE simulation**

I. Introduction

INTEGRATED circuit (IC) design oriented towards optimization of yield becomes a very important task due to increasing CMOS process variability. The variability results from continuous scaling of CMOS device dimensions, from introducing new materials and solutions into MOSFET channels, gate stacks and source/drain junctions, and from introducing new fabrication methods (e.g. in photolithography). These variabilities degrade the IC fabrication outcome and should be taken into account in the design phase to minimize their effect.

There are different approaches addressing this task. The most commonly used is a worst-case (WC), or corner method. It is based on evaluation of the circuit performances for extreme variations expected in a process, bias and temperature values (the corners) [1]. It requires simulation at each corner defined by the set of constraints. For digital CMOS ICs typically it implies setting the model parameters to their min/max values. In the case of a small set of performances the number of corners is low, and the WC method is cost-effective. For increasing complexity of the circuits (case of CMOS analog blocks) the number of corners and simulations significantly increases. But more important is that in general, if parameter correlations are not considered, or unrealistic corners are analyzed, the WC method gives a too pessimistic estimation of the circuit performances. A Monte-Carlo (MC) method is an opposite approach. It consists in evaluation of the circuit performance distributions resulting from statistical distributions of non-correlated model/device parameter subset. The method is considered as reliable, though there is a possibility of a so-called sampling error, which may distort a reasoning. The method is time-consuming. It requires prior determination of parameter statistical distributions. For this purpose e.g. a backward propagation of variance (BPV) method [2, 3] may be used. A common feature of the WC and MC approaches is that they do not directly manipulate IC design parameters. They are used rather to verify correctness of the proposed design, or estimate an expected yield [4].

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II. Cumulative-Distribution Function-Based Approach

The idea standing behind this approach is very simple and may be outlined as follows. A given integrated circuit or block is characterized via its performances. Depending on the circuit design the performances may vary from very simple (e.g. a maximum DC current of a CMOS inverter) to more complicated ones (e.g. open-loop gain of an opamp). Obviously, the circuit performances $\mathbf{X}$ are determined by design parameters $\mathbf{D}$ and by building block/device model parameters $\mathbf{M}$, i.e. $\mathbf{X}=f(\mathbf{D},\mathbf{M})$. Parameter $\mathbf{M}$ variations are the main source of performance $\mathbf{X}$ variations. They result from a clean-room status and technology maturity. They exist always, independently from designer preferences, and should be considered in the design development phase. An appropriate specification of design parameters $\mathbf{D}$ seems to be the only way to do accomplish this task.

In accordance with the presented approach for the given manufacturing process uncertainty the set of design parameters $\mathbf{D}$ should maximize a probability P that the given design performances $\mathbf{X}$ remain within the specification limits $\mathbf{S}$. This approach differs from a standard one, in which a design is made based on nominal model parameters $\mathbf{M_{nom}}$ and eventually on so-called corners.

The optimum design $\mathbf{D_{opt}}$ is determined by (1).

$$\mathbf{D}_{\mathrm{opt}} = \arg\max_{\mathbf{D}} \mathrm{P}\left(\mathbf{X}(\mathbf{D},\mathbf{M}) \in \mathbf{S} \right) \quad (1)$$

Mostly, a condition $\mathbf{X}\in\mathbf{S}$ can be rewritten as a set of N_X inequalities (2). Obviously N_X is a number of circuit performances, considered in the design.

$$\begin{cases} X_{1,min} \le X_1(\mathbf{D},\mathbf{M}) \le X_{1,max} \\ X_{2,min} \le X_2(\mathbf{D},\mathbf{M}) \le X_{2,max} \\ \dots \\ X_{N_X,min} \le X_{N_X}(\mathbf{D},\mathbf{M}) \le X_{N_X,max} \end{cases} \quad (2)$$

The model parameters may be divided into two groups. The first one contains so-called process parameters, which directly reflect real process variability. Thus their variability induces model response spread. A doping concentration, a gate equivalent oxide thickness (EOT), or a carrier mobility are good examples of this class of parameters. The second category comprises parameters which are correlated to the process parameters, or are expected to be less responsible for model characteristics variability. A flat-band voltage, or a number of correction parameters belong to this category. In the following part of the work only variations of the process parameters will be considered.

If a i-th performance X_i (i=1,…,N_X) in (2) is expanded in a surrounding of the model nominal parameter set $\mathbf{M_{nom}}$, then the formula (3) is obtained.

$$X_i(\mathbf{D},\mathbf{M}) = X_i(\mathbf{D},\mathbf{M}_{nom}+\delta\mathbf{M}) \approx \approx X_i(\mathbf{D},\mathbf{M}_{nom}) + \sum_{j=1}^{N_P} \left.\frac{\partial X_i(\mathbf{D},\mathbf{M}_{nom})}{\partial M_j}\right|_{\mathbf{M}_{nom}} \cdot \delta M_j \quad (3)$$

where δM_j (j=1,…,N_P) denote mentioned above statistical variations of process parameters. Mostly, they may be considered as random variables of gaussian probability density function with zero mean values (4).

$$\delta M_j = N(0, \sigma_{M_j}) \quad (4)$$

While the i-th performance is a sum of non-correlated random variables it becomes a random variable with first two moments given by (5a), (5b).

$$E(X_i(\mathbf{D},\mathbf{M})) = X_i(\mathbf{D},\mathbf{M}_{nom}) \quad (5a)$$

$$V(X_i(\mathbf{D},\mathbf{M})) = \sum_{j=1}^{N_P} \left(\left.\frac{\partial X_i(\mathbf{D},\mathbf{M})}{\partial M_j}\right|_{\mathbf{M}_{nom}} \right)^2 \cdot \sigma_{M_j}^2 = \sum_{j=1}^{N_P} S_{ij}^2 \cdot \sigma_{M_j}^2 \quad (5b)$$

S_{ij} coefficients in (5b) are so-called sensitivities of the i-th performances to the j-th process parameter. They are identical in form to the process control monitor (PCM) sensitivities in the backward propagation of variance (BPV) method used for statistical modeling and described briefly further. The mean values $E(X_i)$ and variances $V(X_i)$ depend on design parameters $\mathbf{D}$.

If only a single performance is considered (univariate distribution), then the proposed approach reveals a nice property. The condition (2) may be easily transformed to equivalent form (6).

$$X_{min} - X(\mathbf{D},\mathbf{M}_{nom}) \le \sum_{j=1}^{N_P} \left.\frac{\partial X(\mathbf{D},\mathbf{M})}{\partial M_j}\right|_{\mathbf{M}_{nom}} \cdot \delta M_j \le X_{max} - X(\mathbf{D},\mathbf{M}_{nom}) \quad (6)$$

A sum in (6) is a normally distributed random variable of zero mean value and variance given by (5b). So a probability of (2) may be calculated with (7) based on a cumulative distribution function (cdf) F(·) of a normal distribution f(·).

$$P(X_{min} \le X(\mathbf{D},\mathbf{M}) \le X_{max}) = \int_{X_{min}-X(\mathbf{D},\mathbf{M}_{nom})}^{X_{max}-X(\mathbf{D},\mathbf{M}_{nom})} f(x)\,dx = F(X_{max} - X(\mathbf{D},\mathbf{M}_{nom})) - F(X_{min} - X(\mathbf{D},\mathbf{M}_{nom})) \quad (7)$$

Thus the design optimization task consists in this case in a simultaneous variation of the standard deviation (5b) and integration boundaries in (7) to maximize the area below f(·) and between the boundaries. This approach is illustrated in Fig. 1.

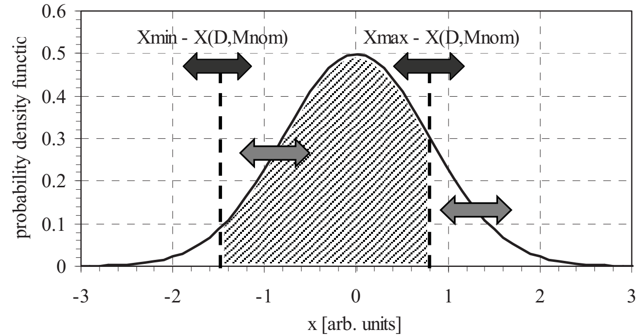

Fig. 1. Graphical representation of design optimization in the case of a single performance; integration boundaries and width of distribution are varied simultaneously via changing the design parameters.

Usually the design is determined by a number of performances. It is particularly the case of analog ICs. Then an additional problem arises. The performances are correlated, because they depend on the same set of process parameters. Thus the probability that the performances remain simultaneously within the corresponding constraint limits, i.e. joint yield, cannot be expressed in general as a product the probabilities for individual performances, i.e. partial yields (8). This issue will be considered in sections V, VI where inverter, opamp, and ring oscillator design examples are discussed.

$$P\left(\bigcap_{i=1}^{n} (X_{i,min} \le X_i(\mathbf{D},\mathbf{M}) \le X_{i,max}) \right) \ne \prod_{i=1}^{n} P(X_{i,min} \le X_i(\mathbf{D},\mathbf{M}) \le X_{i,max}) \quad (8)$$

III. Statistical Modeling Method

An important issue for the design optimization, which accounts for the process variability is a statistical modeling, i.e. determination of the statistical distributions of process (model) parameters. They, together with the design parameters according to (1) describe the circuit behavior. There is a number of methods for statistical parameter extraction. The backward propagation of variance (BPV) method mentioned in section I, seems to be a very efficient approach. This method is based on the idea of the circuit performance-to-process parameter sensitivities, the same which has been used for out cdf-based method for design optimization described in section II. Hence, the basic assumption is a linear dependence of the performance variations on the variations of the process (model) parameters. In the BPV method the statistical distributions of the process parameters are extracted based on experimentally determined statistical distributions of known performances of the test devices or IC blocks.

The BPV method has been extensively developed to take into account the process parameter correlations, which appear to be stronger for scaled technologies and corresponding device models. Also the nonlinearities between performance and parameter variations have been taken into account.

IV. Application of the cdf Method-for CMOS Block Design Based on Analytical Approximations

In order to illustrate the proposed design-for-yield methodology the performances of CMOS inverter and two-stage op-amp are considered. Their definitions are given later, but it is worthwhile to discuss here briefly the correlations between them. They have been calculated using a Monte-Carlo method and a simple MOSFET model [5] for the 0.8 μm CMOS technology. These technology parameters, and the model will be used in the course of further analysis. In the experiment a number of samples was 1000, and the following process parameters have been varied: gate oxide thickness t_{ox}, substrate doping concentrations for both devices N_{subn}, N_{subp}, carrier mobilities μ_{on}, μ_{on}, and fixed charge densities N_{ssn}, N_{ssp}. In Fig. 2 strong dependences between four performances: inverter maximum DC current, and propagation delay, and op-amp low-frequency gain, and phase margin are shown. They result from the fact, that they have been evaluated based on the same set of randomly generated process parameters. This result illustrates a need for careful treatment of performance correlations in the design for yield methodology.

A. CMOS inverter design case

For the analysis purpose, it has been assumed, that the CMOS inverter (Fig. 3) design is evaluated via two performances, namely maximum static current I_{DDmax}, and propagation delay t_P [6]. The maximum DC current I_{DDmax} is calculated for inverter input voltage V_{in} equal to the inverter threshold voltage V_I given by (11).

$$V_I = \frac{V_{DD} - |V_{T,p}| + \sqrt{\beta_n/\beta_p} \cdot V_{T,n}}{1 + \sqrt{\beta_n/\beta_p}} \qquad (11)$$

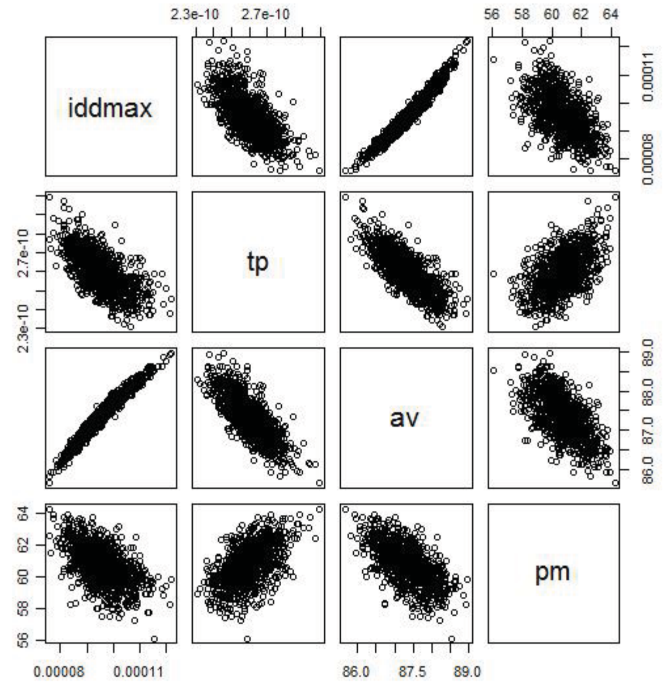

Fig. 2. Correlations between performances of two blocks in 0.8 μm CMOS process: maximum DC drain current I_{DDmax}, and propagation delay t_P of the inverter, and low-frequency gain A_v and phase margin PM of the two-stage op-amp; results have been obtained by 1000 sample MC simulation.

The propagation delay t_P is given be (12).

$$t_{P,HL} = \left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(4\frac{V_{DD} - V_{T,n}}{V_{DD}} - 1\right)\right] R_n C_{out}$$
$$t_{P,LH} = \left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(4\frac{V_{DD} - |V_{T,p}|}{V_{DD}} - 1\right)\right] R_p C_{out} \qquad (12)$$
$$t_P = 0.5 \cdot (t_{P,HL} + t_{P,LH})$$

R_n, R_p terms denote n- and p-channel MOSFET output resistances, whereas common C_{out} term is an average value of the total capacitance load at the inverter output. C_{out} consists of the inverter output capacitance determined by gate-drain and drain-substrate capacitances of both MOSFETs and of the next stage input capacitance determined by gate capacitances of that stage MOSFETs.

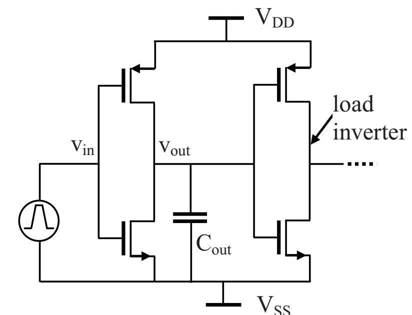

Fig. 3. CMOS inverter; C_{out} comprises output capacitances of the considered inverter and input capacitances of the load inverter.

I_{DDmax}, and t_P performances have been used for evaluation of inverter design taking into account the given process nominal parameters and their variabilities. The performances have been used with the cdf-based method to determine. the n- and p-channel MOSFET widths. The common channel length has been set to the nominal one, i.e. 0.8 μm. In Fig. 4 the contours of the inverter parametric yield obtained (i) by cdf method, as a product of partial yields calculated also by cdf methods, (ii) as product of partial yields calculated by MC method, and (iii) as joined yield calculated by MC method are shown. A good agreement between the three methods may be noticed. Hence it may be stated, that calculation of the total yield in the cdf method as a product of partial yields is accurate enough. This is an important step in overcoming the issue raised by (8). Next, based on Fig. 4 it may be easily seen, how different constraints determine the parametric yield. In order to emphasize this observation, contours for the total and partial yields have been plotted in Fig. 5. The method gives the following optimum (in terms of yield) design of the inverter Wn=3.1 μm, Wp=10.5 μm. It is worthwhile to comment "bi-modal" distribution of the yield. A "valley" in the contour map results from the specification of the minimum t_P constrain. If this condition is neglected the yield contour map becomes "uni-modal" one.

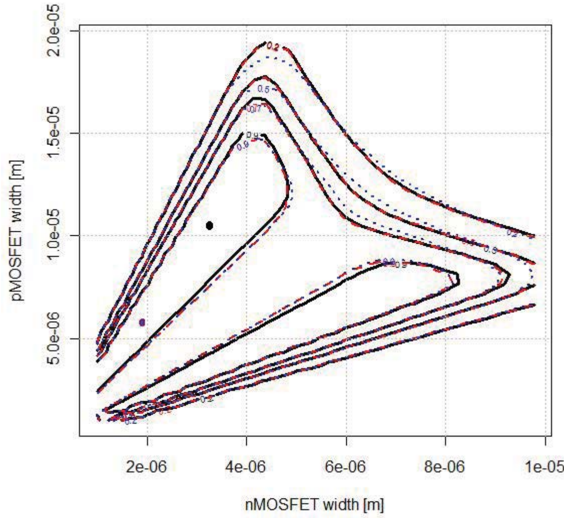

Fig. 4. Contours of the inverter parametric yield obtained by cdf method; solid line - product of partial yields calculated by cdf method, dashed line – product of partial yields calculated by MC method, dotted line – joined yield calculated by MC method.

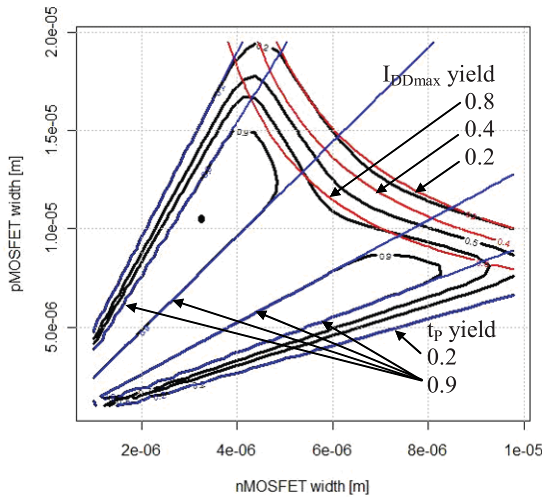

Fig. 5. Contours of the inverter parametric yield obtained by cdf method; closed contiours correspond to the product of partial yields; open contours correspond to partial yields mentioned in the chart area.

B. Two-stage op-amp design case

A general-purpose two-stage operational amplifier has been considered (Fig. 6). It consists of an input stage (M_1, M_2) with active load and the second stage (M_6) in a common-source configuration also with the active load. The circuit contains a compensation circuit (R_c, C_c). The op-amp is biased by the voltage source V_{DD} and current source I_{bias}. At the op-amp output the load capacitance C_L is connected. Operation and design issues of this circuit have been discussed in [7]. The analysis of the op-amp operation is based on an assumption that the transistors remain in a saturation range.

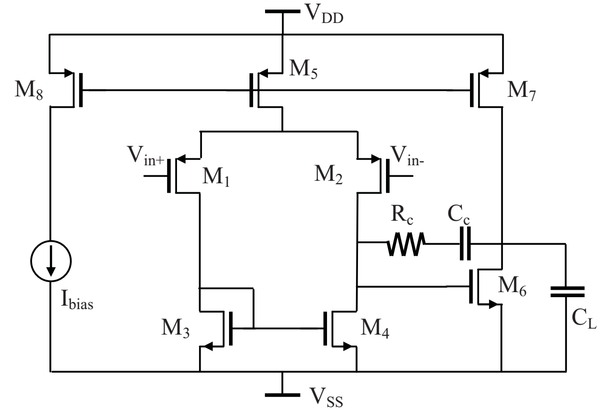

Fig. 6. Two-stage operational amplifier with active load [7]

In our analysis the following op-amp performances specified in [7] have beet taken into account:

- Low-frequency gain: A_v

$$A_V = \left(\frac{g_{m2}}{g_{o2}+g_{o4}}\right)\cdot\left(\frac{g_{m6}}{g_{o6}+g_{o7}}\right) \quad (13)$$

- Phase-margin: PM

$$PM = \Pi - \sum_{j=1}^{4} \operatorname{arc\,tg}\left(\frac{\omega_c}{p_j}\right) \quad (14)$$

- Common-Mode rejection ratio: CMRR

$$CMRR = \frac{2\cdot g_{m1}\cdot g_{m3}}{\left(g_{o3}+g_{o1}\right)\cdot g_{o5}} \quad (15)$$

- Positive Power-Supply Rejection Ratio: PSRR

$$PSRR = \frac{2\cdot g_{m2}\cdot g_{m3}\cdot g_{m6}}{\left(g_{o2}+g_{o4}\right)\cdot\left(2\cdot g_{m3}\cdot g_{o7}-g_{m6}\cdot g_{o5}\right)} \quad (16)$$

- Equivalent input-referred noise power spectral density: S_{in}^2

$$S_{in}^2 = S_1^2 + S_2^2 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \cdot \left(S_3^2 + S_4^2\right) \quad (17)$$

In these equations g_{mi}, g_{oi} denote input and output conductances of i-th transistor, ω_c is a unity-gain bandwidth, p_j denote j-th poles of the circuit, and S_k are the input-referred noise power spectral densities, consisting of thermal and 1/f components.

Similarly to the inverter case the amplifier has been analyzed using the cdf-based method. In Fig. 7, 8 closed contours of parametric yield calculated based on the cdf method are plotted in the (W_{p1}/L_{p1}, L_{p1}) space. Again, a good agreement between the cdf and MC method results may be noticed. The influence of different constraints, namely minimum gain, minimum phase margin and maximum noise spectral density may be easily identified. The corresponding curves are shown in Fig. 8. In Fig. 7 the unique optimum design parameter sets in the (Wp1/Lp1, Lp1) space, obtained for cdf and MC methods are also shown. The agreement between them is satisfactory.

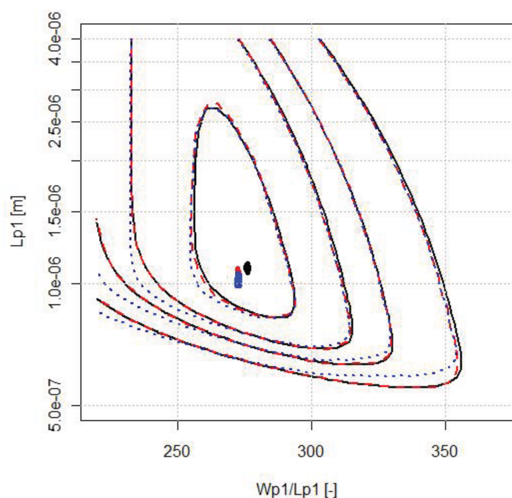

Fig. 7. Contours of the op-amp parametric yield obtained by cdf method; solid line - product of partial yields calculated by cdf method, dashed line – product of partial yields calculated by MC method, dotted line – joined yield calculated by MC method.

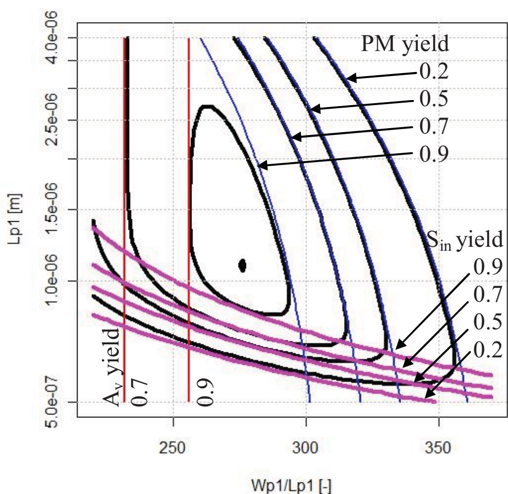

Fig. 8. Contours of the op-amp parametric yield obtained by cdf method; closed contours correspond to the product of partial yields; open contours correspond to partial yields mentioned in the chart area.

V. Application of the cdf Method for CMOS Block Design Based on SPICE Simulations

In the previous section the task of yield evaluation towards design optimization has been accomplished using the analytical formulae for CMOS cell performances. Obviously this approach is efficient in terms of time and memory effort, but is not accurate. However the proposed cdf-based methodology allows also for use of SPICE simulations for calculation of performances of the block under design. Such an approach is much more accurate and is described in this section based on a five-stage CMOS ring oscillator case shown in Fig. 9.

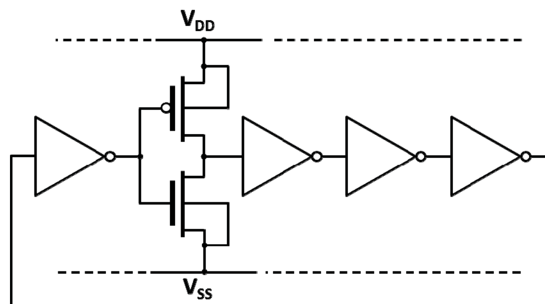

Fig. 9. Five-stage CMOS ring oscillator

The devices in the circuit are represented by BSIM3v3 models of MOS transistors [8] corresponding to the 0.6 µm CMOS technology. The circuit is represented by a netlist stored in a *.cir file. The circuit simulations specified in this file and described below have been done using ngspice program, which is one of the open-source EDA tools (e.g. [9, 10]) offering a full range functionality in terms of IC simulation.

The oscillator supply biased is 3.3 V. The MOSFET channel lengths are 0.6 µm Two oscillator performances have been considered, namely oscillation frequency f_{osc} and power consumption P. It has been assumed, that these performances should meet the following constraints:400 MHz $\leq f_{osc} \leq$ 800 MHz, P $\leq$ 0.9 mW. The oscillation frequency tolerance is intentionally large in order to have in the design space solutions corresponding to a full scale of parametric yield from very low up to very high values.

It has been assumed that the performance variability, limiting the yield, results from the spread of the following BSIM3v3 model parameters: flat band voltage VFB, gate oxide thickness TOX, substrate doping NSUB, channel doping NCH, junction depth XJ, low field mobility U0, length reduction parameter LINT, width reduction parameter WINT. These parameters establish the so-called process parameter set, defined in section II.

The simulations require random sampling of the process parameters, updating model cards, SPICE simulations for each parameter set, and finally output data storage and postprocessing. These functions have been implemented in Octave [11] script.

Variability of the process parameters has a strong impact on device and ring oscillator performances. In Fig. 10 a spread of transfer I-V characteristics of the MOSFETs is shown. The

curves have been evaluated for 1000 samples of independently generated process parameters. It is worthwhile to mention, that in spread of the I_D-V_{GS} curves a variability of a drain-induced barrier lowering (DIBL) effect has not been taken into account, which has been recently strongly recommended (e.g. [12]).

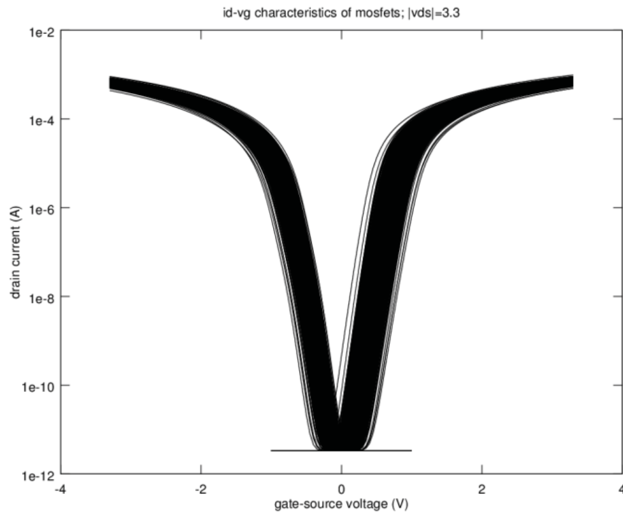

Fig. 10. Transfer characteristics of n- and p-channel MOSFETs calculated for 1000 samples of randomly distributed proces parameters

In Fig. 11 a set of ten waveforms of the ring oscillator for randomly generated process parameters is shown. Again, a strong effect of process variability may be stated.

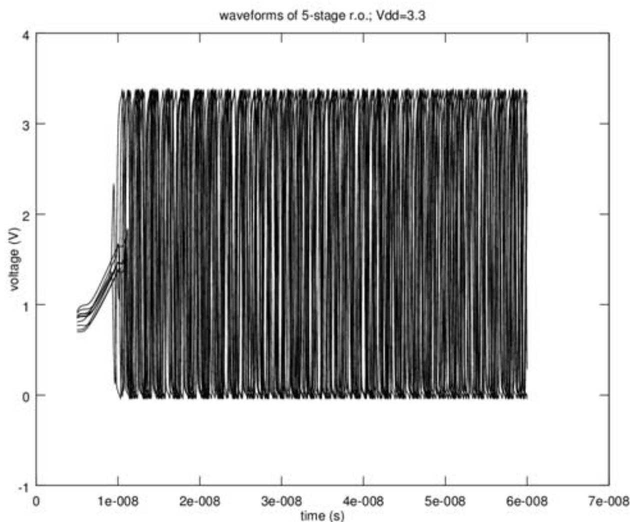

Fig. 11. CMOS ring oscillator wavefporms calculated for 10 samples of randomly distributed proces parameters

In Fig. 12 histograms of the circuit performances are shown. They have been computed for the n- and p-channel MOSFET widths equal to 3 μm, and 7.5 μm respectively. It may be stated (without appropriate testing), that the performances are approximately normally distributed around their mean values $f_{osc,mean}$≈422 MHz, and P_{mean}≈1.43 mW. Additionally these mean values are very close to the respective mediana values. It should be also mentioned, that the mean values, which correspond to the circuit performance nominal values, in particular the consumed power P_{mean} do not meet constraints mentioned above. Thus it may be expected, that the proposed design optimization method should lead to another design, which satisfies acceptable performances.

In Fig. 13 a scatterplot is shown, which illustrates, as expected, a strong between oscillation frequency and power consumption. Thus this example seems to be a severe test for overcoming in cdf-based method the inequality (8), and calculating the total yield as a product of partial yields.

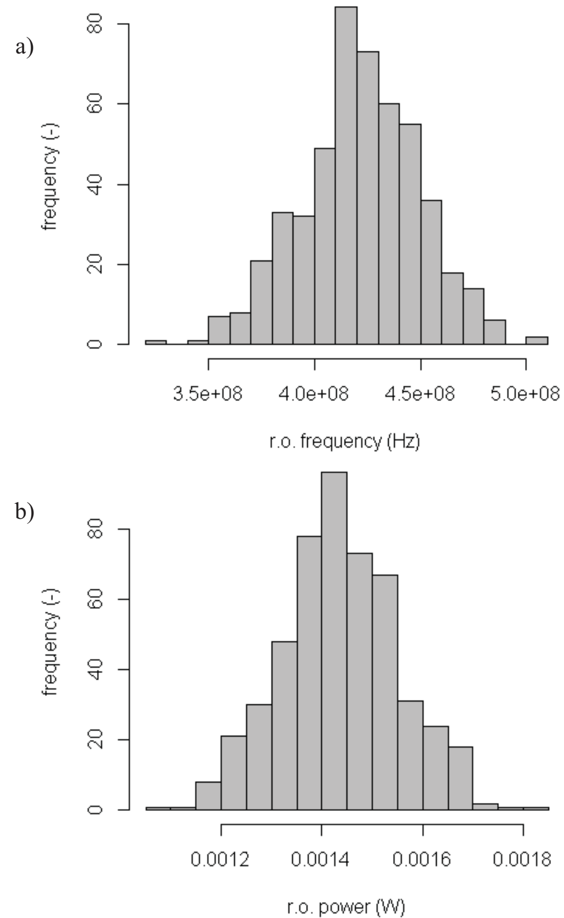

Fig. 12. A histogram of CMOS ring oscillator performances a) frequency, b) power consumed; number of samples=500

The partial and total parametric yields of CMOS ring oscillator vs widths of n- and p-channel MOSFETs have been calculated using the MC method, and the proposed cdf-based method. The results are shown in Fig. 14 in the same manner as in section IV.

A reasonably good agreement between the MC and cdf-based methods may be noticed. Both methods lead to a unique solution which is approximately: $W_{n,opt}$≈1.3 μm, $W_{p,opt}$≈4.5 μm. A small discrepancy between contours of the partial yield coming from the frequency constraint and the total yield, both calculated with the cdf-based approach results probably from a strong correlation between both performances. Thus a violation of the inequality (8) is reflected in the yield simulation results.

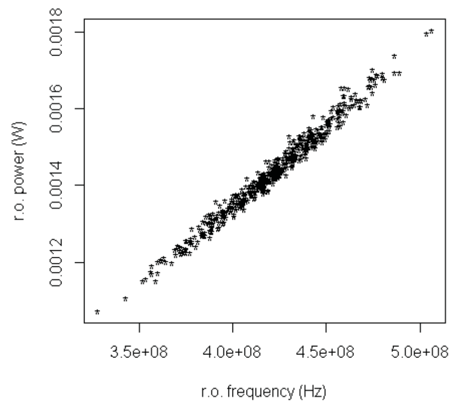

Fig. 13. A correlation between frequency and power of the ring oscillator; number of samples=500

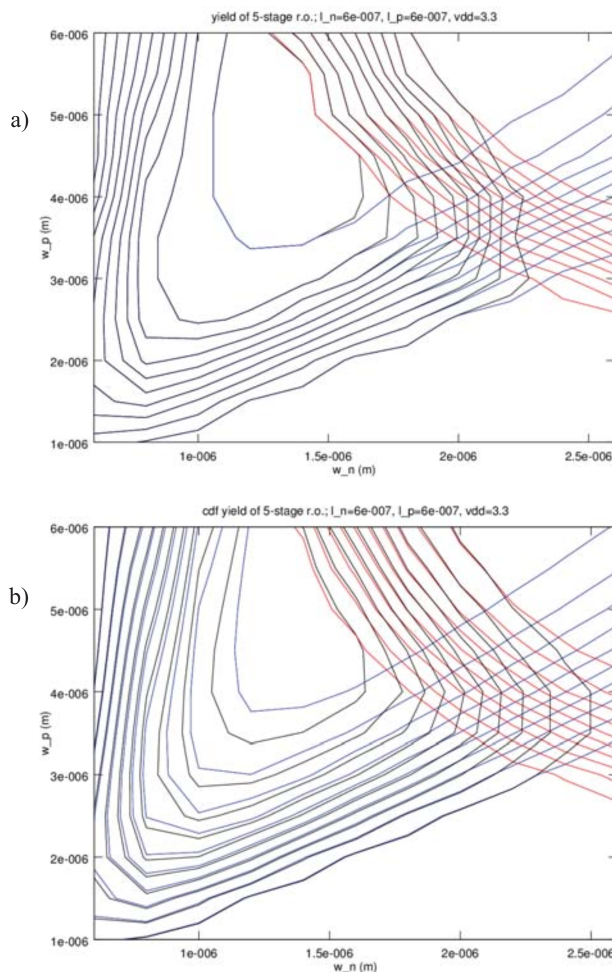

Fig. 14. Contours of partial and total yield of CMOS ring oscillator vs widths of n- and p-channel MOSFETs calculated using a) MC method, b) cdf-based method; red lines - power limit-induced yield, blue lines - frequency limit-induced yield, black lines - joined/total yield

VI. Summary

In the presented work a method for IC design aiming at maximization of the parametric yield has been presented. It has been illustrated based on simple CMOS inverter, two-stage op-amp, and ring oscillator cases.

The cdf-based method gives results very close to the time consuming Monte Carlo method. It is very fast and intuitive. It is worthwhile to mention, that in the case of very mild performance constraints X_{min}, X_{max} the method leads to continuous set of design parameters, for which the yield close to 100% is expected. On the other hand, if the constraints are very severe with respect to process variability the method leads to unique solution, for which the parametric yield below 100% is expected. Thus it may easily give information, whether the considered design class is eligible for the technology in use.

The cdf-based method has also another advantage. The design rules of the given IP may be directly used and shown in the yield plots in the design parameter space.

The presented work has been prepared using Perl scripting language, Octave environment [11], ngspice open source IC simulator, and R statistical package [13]. Hence it may be stated that the results of this work are to some extent a testimony that such tools may helpful in everyday IC design work.

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