Low Noise Micro-Power Chopper Amplifier for MEMS Gas Sensor

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***Abstract*—In this paper, a low-noise, low-power and low voltage Chopper Stabilized CMOS Amplifier (CHS-A) is presented and simulated using transistor model parameters of the AMS 0.35 µm CMOS process. This CHS-A is dedicated to high resistive gas sensor detection. The proposed CHS-A using Chopper Stabilization technique (CHS) exhibits an equivalent input referred noise of only 0.194 $nV/\sqrt{Hz}$ for a chopping frequency of 210 kHz under ±1.25 V supply voltage and 26.5 dB voltage gain. The inband PSRR is above 90 and the CMRR exceeds 120 dB. At the same simulation condition, the total power consumption is 5 µW only.**

***Index Terms*—Gas sensor, low-noise, low-power, chopper modulation, analog integrated circuits**

I. Introduction

A mobile sensor system for very low level signals such as gas spikes detection is required to implement with a scaled CMOS technology. The development of metal oxides gas sensors has experienced a considerable growth because of an interest more and more important in the protection of environment and people safety. Thanks to technological advances in microelectronics that promote better performances, low costs in terms of consumption and production, these sensors can be used for monitoring air quality in many fields such as transport, industry or housing environment. Optical sensors are generally well adapted with good accuracy but to much bulky and expansive. At the opposite, semiconducting gas sensors are more and more attractive.

It is clear that metal oxide sensors sold today present mixed performances. Indeed, despite an interesting sensitivity with a detection threshold around the ppm, those sensors also have low selectivity and significant drift, which limit their use to simple detectors. For a key circuit of these systems, a Chopper Stabilization Amplifier (CHS) which suppresses DC offset and 1/f noise figure of MOS devices is commonly used [1]. Typical sensor output signals are in the microvolt range and have bandwidths ranging from DC up to a few kilohertz [2]. One of the main challenges in weak sensor signals data acquisition systems are low-frequency 1/f noise and DC-offset [3]. To achieve the sub-microvolt level both for offset and noise, the CHS has been found a prime candidate to meet these requirements [4][5]. CHS is employed in the amplification stage to eliminate the non-ideal low frequency effects, such as the flicker noise and DC-offset voltage [6][7].

The signal pickup of the device only provides a very weak signal, i.e. on the order of a few µV, which necessitates preamplification prior to any further processing. The main signal energy of gas sensor signals lies in a frequency band of a few kHz. Due to the weak signal, low-noise operation of the preamplifier is crucial in order to retain a sufficient signal to noise ratio (SNR) for gas sensor signal extraction. To ensure the best possible signal recovery and to enable gas sensor response while ensuring skin continuity, fully implantable electronic interfacing solutions are required.

This paper reports on the design of a fully integrated and simple chopper stabilized amplifier suitable for MEMS gas sensor. This CHS contains classic analog structures like a passive modulator/demodulator, a 2nd order selective BP-filter with a simple OTA-Miller core, a gain stage with a simple OTA-Miller core and a 1st order passive LP-filter in the output. We show that this CHS rejects DC-offset and offer very good performances like power consumption and equivalent input referred noise over a wide number of

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previously published CHS-A [1][2][3][4].

This paper is organized as follows. Section II describes the gas sensor. Section III describes the basic principle of the proposed CHS-A. Section IV presents an analysis of CMRR improvement. Section V describes the circuit design. Section VI presents simulations. Section VII presents design comparison and finally, in section VIII a conclusion is given.

II. Single Gas Sensor Description

Gas sensor presently used can be decomposed in two parts: a metal oxide sensitive layer and a silicon microhotplate. A first generation of microhotplate has been initially developed by LAAS-CNRS in collaboration with MOTOROLA, and currently exploited by MicroChemical Systems S.A [8]. This structure which includes polysilicon heater and thin insulated membranes, allows low power consumption (can reach 600°C with less than 100mW) and very low thermal inertia (minor than 25 ms from ambient to 500°C).

Nowadays, LAAS-CNRS and IM2NP develop conjointly this kind of structure with a polycrystalline silicon heater and WO_3 thin sensitive layer. Even if this technology has already presented good results and is relatively well controlled, it is not free of defaults.

Some studies show that polysilicon heater drifts significantly [9]. Indeed there is a not reversible resistance drift. That needs more power to reach the same temperature. However the more important power is, the more heater resistor degrades…Moreover the heater aging acts on the gas sensitivity: thermal conditioning of sensitive layer is directly bounded to detection phenomenon. However optimum sensitivity for one gas presents generally a restricted spectrum of operating temperature. In addition, if the sensor is used with pulsed operating mode, temperature variations can have a negative effect on kinetic response of sensitive layer (or if the temperature is not well controlled).

To free itself of this major drawback, it is very important to obtain a good stability of the heater resistor. For that, two choices are considered:

- To develop a power control unit eventually in pulsed mode but it reduces significantly the sensor life time without solving the heater drift problem.
- To design a new more stable microhotplate.

A new generation of microhotplate was conceived without any polysilicon resistor. This structure is detailed on Fig. 1. It consists of a platinum resistor. The use of this material would have advantage to reach high level of temperature (around 600°C compare to 450°C with polycrystalline silicon). Finally, Pt-heater can be use such as a metallic thermistor in aimed to control more accurately sensitive layer temperature.

The micromachined hotplate is realized on double side polish silicon substrate. Membrane with low residual stress is constituted by LPCVD deposit of SiO_2/SiN_X (1.4/0.6µm) bi-layer. Heater consists of Ti/Pt (0.01/0.15µm) deposited with electron beam evaporation. Then its geometry is obtained by lift-off process [10]. The heater is then insulated by a PECVD deposit of SiO_2 layer. Then, interdigitated electrodes are realized by similar metallization of the heater using the Ti/Pt layer. The sensitive layer of WO_3 (0.03µm) is deposit by RF magnetron sputtering [11]. Finally the membrane is released on the backside by DRIE (Deep Reactive Ion Etching).

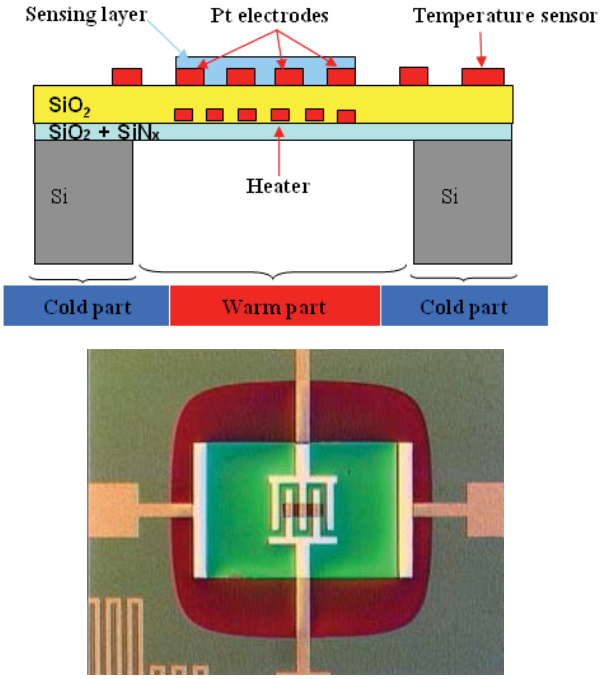


Fig. 1. Schematic and top of view of gas sensor with platinum heater

III. Basic Principle of the CHS-A

Chopper Stabilized Amplifiers are low-noise continuous-time amplifiers useful for amplifying DC and very low frequency signals. CHS-A is used for instrumentation application such as Gas sensor detection [12][13]. Often the design objective is to reach the microvolt level for both offset and noise, with a bandwidth limited to a few hundred Hz while maintaining the low power consumption. CHSs are best suited for low-power, very low-noise, very small offset and offset drift. They are needed for gas sensors applications.

The CHS technique uses an AC carrier to transpose the input signal to higher frequency. The principle of chopper amplification is illustrated in Fig. 2 [14] with input V_{in}, output V_{out}, and A is the gain of a linear amplifier. The signal $m_1(t)$ and $m_2(t)$ are modulating and demodulating carriers with period $T=1/f_{chop}$ where f_{chop} is the chopper frequency. Also, V_{OS} and V_n denote deterministic DC-offset and 1/f noise. It is assumed that the input signal is band limited to half of the chopper frequency f_{chop} so no signal aliasing occurs [2]. Basically, amplitude modulation using a square-wave carrier transposes the signal to higher frequencies where there is no 1/f noise, and then the modulated signal is demodulated back to the base band after amplification [2].

For the periodic carrier with a period of T and 50% duty

cycle, its Fourier representation is:

$$m(t) = 2\sum_{k=1}^{\infty} \frac{\sin(\frac{k\pi}{2})}{(\frac{k\pi}{2})}\cos(2\pi f_{chop} kt) \quad (1)$$

Its k-th Fourier-coefficients, Mk, have the property:

$$M_0 = M_{\pm 2} = M_{\pm 4} \ldots = 0 \quad (2)$$

The modulated signal is the product of the initial signal and equation (1). The spectrum of the product $V_{in} \cdot m_1(t)$ in Fig. 2 shows that the signal is transposed to the odd harmonic frequencies of the modulating signal. After amplification, the modulated signal is then demodulated by multiplying $m_2(t)$ to obtain:

$$V_d(t) = 4AV_{in}(t)\left[\sum_{k=1}^{\infty} \frac{\sin\left(\frac{k\pi}{2}\right)}{\left(\frac{k\pi}{2}\right)}\cos(2\pi f_{chop} kt)\right] * \left[\sum_{l=1}^{\infty} \frac{\sin\left(\frac{l\pi}{2}\right)}{\left(\frac{l\pi}{2}\right)}\cos(2\pi f_{chop} lt)\right] \quad (3)$$

To recover the original signal in amplified form at the output, the demodulated signal must be applied to a low-pass filter with a cut-off frequency slightly above the input signal bandwidth. In this case, we choosed a half of the chopper frequency. Noise and offset are modulated only once [3].

A typical noise power spectrum for CMOS amplifiers is shown in Fig. 3(a). For low frequencies, the noise spectrum is dominated by flicker (1/f) noise. At higher frequencies, the noise spectrum is determined by the thermal noise of the transistors. The frequency at which the 1/f noise is equal to the thermal noise is denoted the corner frequency f_c. The input referred noise spectral density for a MOS transistor is given by [15]:

$$v_{ni}^2(f) = \underbrace{4kT\frac{2}{3}\frac{1}{g_m}}_{thermal} + \underbrace{\frac{k_f}{WLC_{ox}f}}_{flicker} \quad (4)$$

Where k is the Boltzmann's constant, T is the absolute temperature, g_m is the transconductance of MOS transistor, W and L are the channel width and length of MOS transistor, C_{ox} is the physical gate oxide thickness and k_f is the flicker noise coefficient of MOS transistor. From Eq. (4), we see that the thermal noise contribution is inversely proportional to the MOS transistor transconductance g_m. Using the EKV model [16], the transconductance normalized to the drain current for MOS transistors working in weak and strong inversion respectively can be found.

$$\frac{g_{m\ weak}}{I_{DS}} = \frac{1}{nV_T} \quad (5)$$

$$\frac{g_{m\ strong}}{I_{DS}} = \frac{2}{V_{eff}} \quad (6)$$

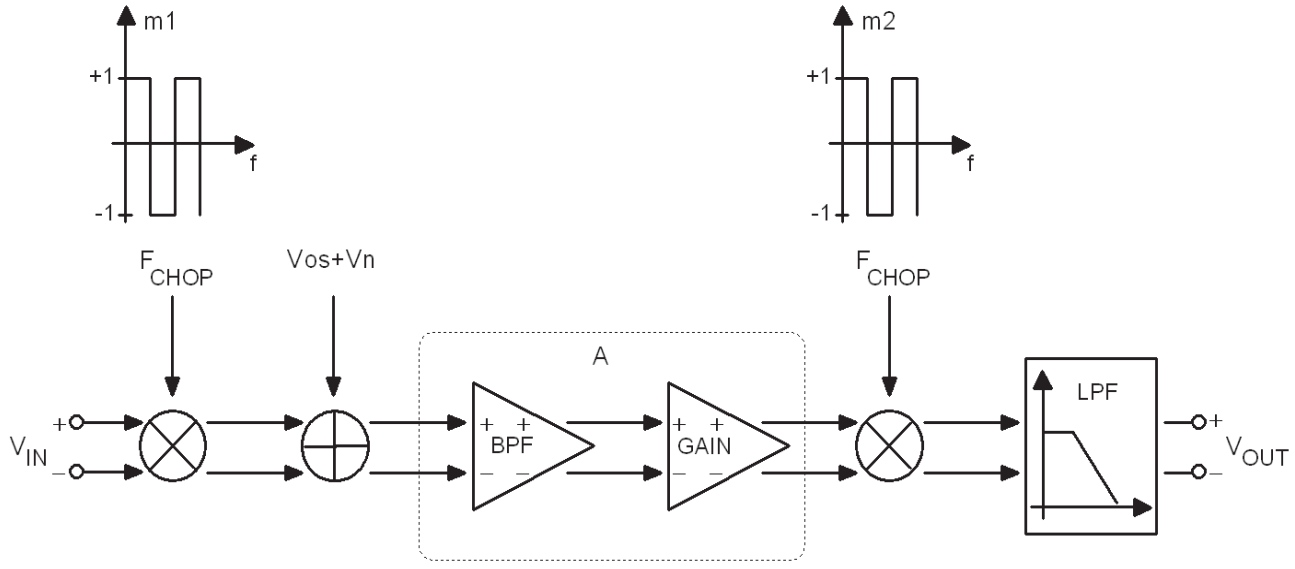
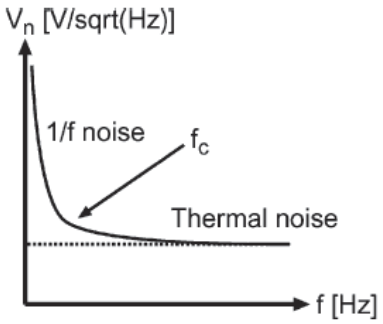


Fig. 2. Chopper stabilization amplifier principle [14]

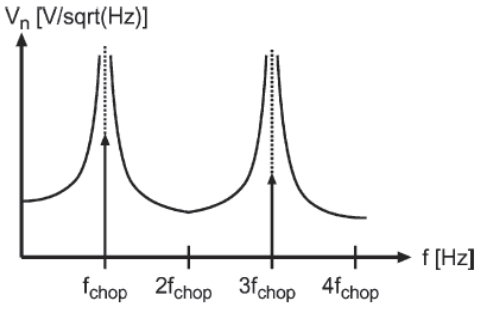
Where V_T is the thermal voltage and $V_{eff} = V_G - V_{th} - nV_S$ is the effective voltage. V_{th} is the threshold voltage and n is the slope factor. All terminal voltages are referred to the bulk. Hence the thermal noise suppression is maximized by increasing the drain current I_{DS}, and biasing the MOS transistor in the weak inversion region of operation.

The noise corner for MOS transistor can be located at several kHz. Thus, the 1/f noise dominates in the frequency range of interest for gas signals. Equation (4) shows that the 1/f noise level can be minimized by maximizing the MOS transistor area, however for the low noise levels necessitated by the weak input signal, the device dimensions become very large [17], implying poor PSRR at higher frequencies due to parasitic feedthrough.

By employing the CHS, the impact of 1/f noise can be drastically reduced. In Fig. 2, the input signal V_{in}, is chopped prior and after amplification, thus shifting the input frequency to the chopping frequency during amplification and then shifting it back to the baseband.



(a) CMOS noise spectrum



(b) CMOS chopped noise spectrum

Fig. 3. CMOS amplifier noise spectra. (a) No chopping. (b) Chopped.

The amplifier noise is however only chopped once, which will shift the 1/f - noise to the odd multiples of the chopping frequency as illustrated in Fig. 3(b), leaving the thermal noise as the main inband noise contributor.

The 1/f noise power spectral density (PSD) can be referred to the wideband thermal noise floor S_0, and the noise corner f_c by [2]:

$$S_{1/f}(f) = S_0 \frac{f_c}{|f|} \tag{7}$$

Let Sn denotes the noise PSD of the amplifier. For an amplifier with a DC-gain A_0, it can be shown that the output noise PSD for the CHS is given by [2]:

$$S_y(f) = A_0^2 \left(\frac{2}{\pi}\right)^2 \sum_{\substack{n=-\infty \\ nodd}}^{n=+\infty} \frac{1}{n^2} S_n\left(f - nf_{chop}\right) \tag{8}$$

Where, the summation indicates the spectrum foldover components. Inserting Eq. (7) in Eq. (8), results in the following expression for the CHS output 1/f noise:

$$S_{y.1/f}(f) = \left(\frac{2A_0}{\pi}\right)^2 \sum_{\substack{n=-\infty \\ nodd}}^{n=+\infty} \frac{1}{n^2} \frac{S_0 f_c}{\left|f - nf_{chop}\right|} \tag{9}$$

Numerical analysis of Eq. (9) reveals that the first order aliased components $n = \pm 1$ are responsible for more than 95% of the aliased noise [7]. For our simulation of the modulator/demodulator, the noise corner was observed to be located at approximately 2 kHz, and typically a chopping frequency of 210 kHz was employed. A good approximation of the resulting effective thermal noise floor can be extracted by adding only the first order terms to the thermal noise. Assuming a flat inband 1/f noise contribution and taking the magnitude at DC, an approximate expression for the effective thermal noise can be found [2]:

$$S_{th.eff}(f) \approx A_0^2 S_0 \left(1 + \frac{8}{\pi^2} \frac{f_c}{f_{chop}}\right) \tag{10}$$

Equation (10) reveals that less than 10% increase in effective thermal noise can be expected for chopping frequencies f_{chop} up to $10 f_c$.

I. CMRR in Chopper Amplifiers

High common-mode rejection ratio (CMRR), typically 110–120 dB [18][19], is usually observed in trimmed or stabilized continuous-time microvolt offset amplifiers. Both offset and CMRR are due to the same mismatch effects, and their product is to a first order equal to the Early voltage of the bias current source transistor of the input differential pair [20].

Less well appreciated is the CMRR and offset suppression in chopper modulated amplifiers. Instead of trimming or regulating the offset to zero and simultaneously increasing the CMRR, the operation in the chopper amplifier is more complex. The elementary operation of the chopper amplifier for a differential signal, noise, and offset has been extensively discussed in [1][2][3][4]. In the strict sense of the term, CMRR (as well as power-supply rejection ratio (PSRR)) is the ratio of two transfer functions at the same frequency, which are

defined in a linear time-invariant system. Since the chopper amplifier is a time-variant system, it is inherently nonlinear. However, with regard to a bandwidth limitation of the input signal $f_{sig}<f_{chop}$, the amplifier behaves as a quasi-linear system in the frequency range considered. This band-limitation requirement is usually satisfied in low-frequency sensor applications, and f_{chop} can be chosen accordingly (by taking into account that the residual offset increases proportionally as f_{chop} increases). In contrast to the signal, spurious signals such as common mode interference may not be band limited and will be aliased to the baseband. A similar situation has been observed in switched-capacitor networks [3]. It is therefore important to have an estimate of the amount of out-of-band common-mode interference that will be aliased to the baseband.

Since the fully differential input modulator consists of four cross-coupled switches, it is completely transparent to any common-mode signal. For this reason, the common-mode signal V_{cm} appears directly at the input of the amplifier. A differential signal is then formed according to the amplifier's common-mode transfer function $A_{cm}(f)$ and multiplied by the second chopping signal $m_2(t)$ which shifts it to the odd harmonics of the chopping frequency. This can be described by the following equation:

$$\left|V_{out}(f)\right| = \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{1}{n} * \left|A_{cm}(f-\frac{n}{T}) * V_{cm}(f-\frac{n}{T})\right| \qquad (11)$$

Where $(1/T)=f_{chop}$.

Hence, a low-frequency common-mode signal V_{cm} ($f<(f_{chop}/2)$), such as spurious interference of the mains, will be mixed to out-of-band frequencies. In this sense, its suppression is similar to the original offset and low-frequency noise. Similar to the residual offset due to clock-feedthrough spikes, a residual differential signal due to common-mode modulated charge-injection spikes of the input modulator persists, which limits the CMRR. Thus, the BP filter not only improves the achievable residual offset but also further enhances the CMRR performance.

Aliasing of common-mode signals V_{cm} ($f > (f_{chop}/2)$), as predicted by Eq. (11), depends on the original common-mode transfer function $A_{cm}(f)$, which is essentially determined by the first gain stage. In our case, this is a fixed-gain wide-band preamplifier. It is well known that $A_{cm}(f)$ is affected by a zero f_z due to the input stage bias current source [2]. This zero causes the CMRR to roll off by -6dB/oct at f_z. However, this degradation of CMRR at higher frequencies actually does not increase the portion of common-mode signal that will be downconverted to the baseband provided that $f_z>f_{chop}$. By the careful design of a wide-band CMRR preamplifier, such that $f_z>>f_{chop}$, an effective attenuation of out-of-band interferences can be obtained. Moreover, a subsequent BP filter will further improve this attenuation. A worst case frequency range for aliasing of common-mode interferences is therefore the bandwith of the BP filter.

II. Circuit Design

A. Chopper modulator/demodulator

Passive chopper modulator/demodulator circuits can be easily implemented in MOS technology as only four switches are needed for a fully differential chopper implementation as shown in Fig. 4.

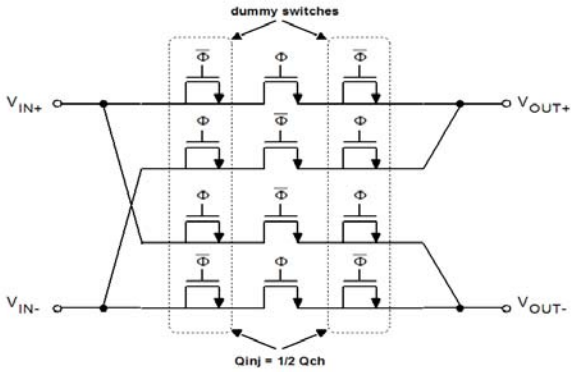


Fig. 4. Chopper modulator/demodulator

Here, the sign inversion is accomplished simply by alternating the signal path using a clock Φ , and its counter phase $\overline{\Phi}$. The charge injection q_{inj}, as the switch MOS changes state, is a major contributor to dynamic offset [2][14]. For fast switch clock waveforms, the channel charge will split equally to the source and drain terminals [2], hence to compensate for the charge injection, half sized dummy MOS with shorted drain-source are inserted in the signal path. By using the clock counterphase for the dummy switches, the dummy MOS charge will cancel the main switch charge to a first order approximation.

As the input chopper circuit receives the input signal directly from the gas sensor, this circuit is noise critical. The thermal current noise spectral density due to the resistive channel in the MOS is given by [14]:

$$i_n^2(f) = 4kT\underbrace{K'(W/L)V_{eff}}_{g_{ds}} \qquad (12)$$

In Eq. (12), the maximum V_{eff}, is given by the available supply voltage. As NMOS transistors have a higher K compared to their PMOS transistors counterparts, these are an appropriate choice for the switches.

The output chopper is not noise critical as the output signal has gained 40 dB in magnitude. Hence, minimum sized NMOS transistors can be used for the output chopper. In order to be able to employ dummy switches, larger than minimum sized switches were employed.

B. Amplifier design

For achieving the necessary high overall gain in a controlled manner, two amplifying stages are used. Most of the gain is achieved in the first stage as this stage is noise critical,

whereas the second stage brings the signal to the desired final level.

1) First stage

The architecture that has been used to implement the first stage 2nd order band-pass filter is Sallen-Key Topology as shown in Fig. 7. This was chosen thanks of its simplicity. The Active-RC Sallen-Key filters have a range of advantages when used for lower order of the filter: have excellent linearity, have low power dissipation and are easy to design and analyze. The schematic of a classical OTA-Miller integrated circuit implemented with CMOS transistors is illustrated in Fig. 8 [21]. It consists of a basic differential pair implemented with PMOS transistors (M_1 and M_2), which has a single-ended current source as active load implemented with NMOS transistors (M_3 and M_4). This stage is biased with the current mirror formed with PMOS transistors M_5 and M_6, whose reference current source is I_{REF}=200 nA. The second stage is a basic common source amplifier with an NMOS transistor (M_7) acting as amplifier and a PMOS transistor (M_8) acting as a current source load. We assign the values indicated in Table I to the transistor sizes such as length L and width W. This OTA-Miller is designed to drive a load capacitor, C_L, of 5pF. It is biased with voltage sources V_{DD} = -V_{SS} = 1.25 V. The process parameters for the transistors used in this work correspond to the AMS 0.35µm Technology. All the design specifications for the OTA-Miller were optimized while the sizes of CMOS transistors remain in the valid range for the selected technology. The design of our CMOS OTA-Miller integrated circuit starts by defining the design specifications in terms of the performance parameters of interest, such that a high open lop voltage gain, |Av|, a high phase margin, PM, a low slew rate, SR, and a low power dissipation, PD.

TABLE I
TRANSISTOR SIZES OF THE OTA-MILLER

Transistors	Type	Size W/L (µm/µm)
M_1-M_2	pmos	30.5/0.5
M_3-M_4	nmos	0.5/1
M_7	nmos	4.5/1
M_5-M_6-M_8	pmos	3/1

The results of circuit simulation for the OTA-Miller are shown in Fig.5. We simulate an initial |Av| of 26.5 dB at low frequencies, a 1.208 MHz frequency at unity DC-gain and 159 kHz for a -3dB cut off frequency. On the other hand, the Phase Margin in Fig.6, PM, is approximately PM = 46°. The simulated positive Slew Rate, SR+, is 0.822mA/µs, while the SR- is -0.383mA/µs.

The results of circuit maker simulation for the 2nd order Active-RC Sallen-Key band-pass filter are shown in Fig. 9. The filter design has passband frequency of 40 kHz, a center frequency of about 203 kHz, a passband gain of about 12.2, a quality factor Q of 5, a low cut-off frequency of 185 kHz, a high cut-off frequency of 225 kHz, a Total Power Dissipation, TPD, at the starting point is 1.28 µW.

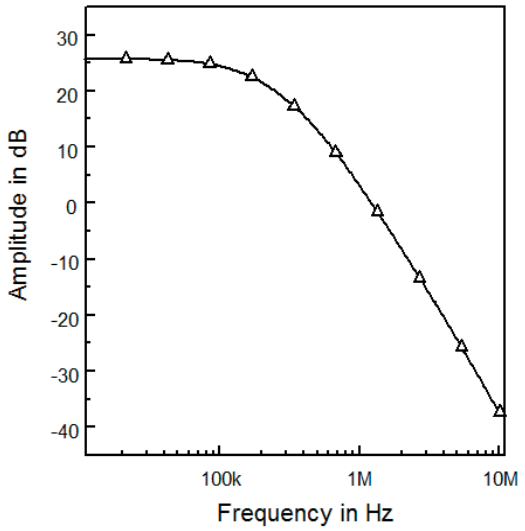


Fig. 5. DC gain

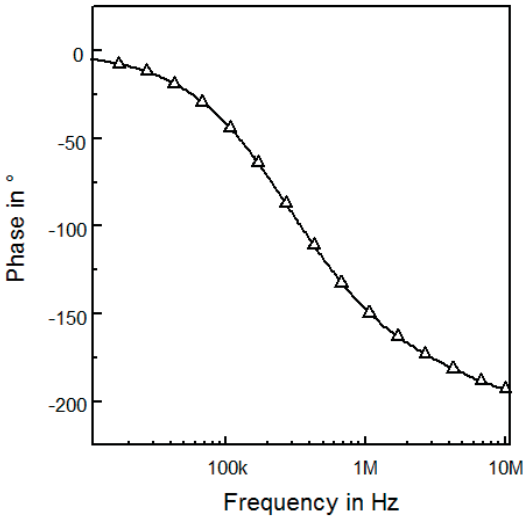


Fig. 6. Phase margin

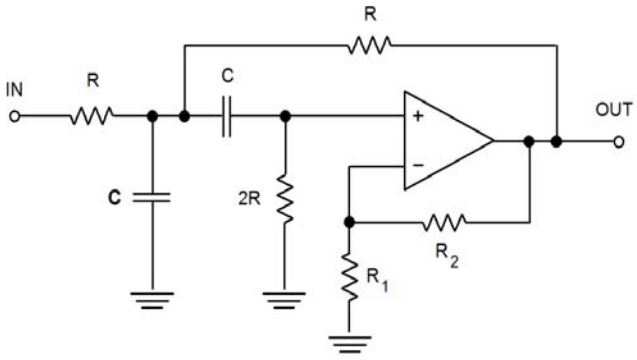


Fig. 7. Second order Sallen-Key band-pass filter

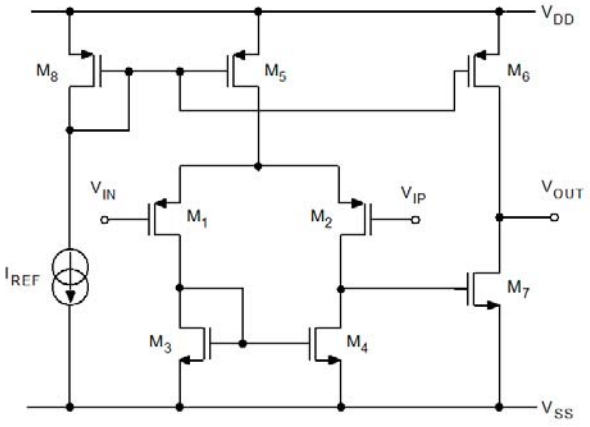


Fig. 8. Schematic of a classical CMOS OTA-Miller

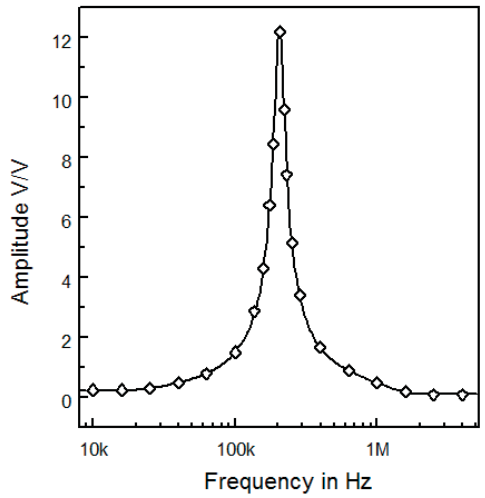


Fig. 9. Response of the second order Sallen-Key band-pass filter

2) Second stage and low pass filter

The CMOS OTA-Miller is used in the first stage bloc and in the second amplifier gain stage simultaneously to obtain a good trade-off between power consumption and input noise. The schematic of the second stage is illustrated in Fig. 10. The gain of the second stage is about 40 dB.

The low-pass filter is implemented with a simple R-C cell. The 3-dB cut-off frequency of the filter is chosen to be 10 kHz.

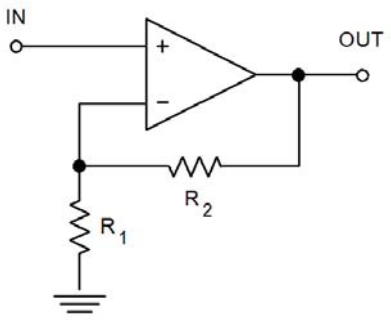


Fig. 10. Second gain stage schematic

III. Simulations

The chopper amplifier was simulated in the AMS 0.35 µm Technology. The magnitude frequency response of the CHS is shown in Fig. 11. The input signal has 100 µV amplitude and 10 kHz frequency. The chopping frequency has been set to 210 kHz. The output signal has 2.1 mV amplitude and 10 kHz frequency. Thus, a gain of 26.5 dB is achieved from the CHS. The output noise PSD of the CHS is depicted in Fig. 12. The effective noise floor referred to the input is 0.194 $nV/\sqrt{Hz}$.

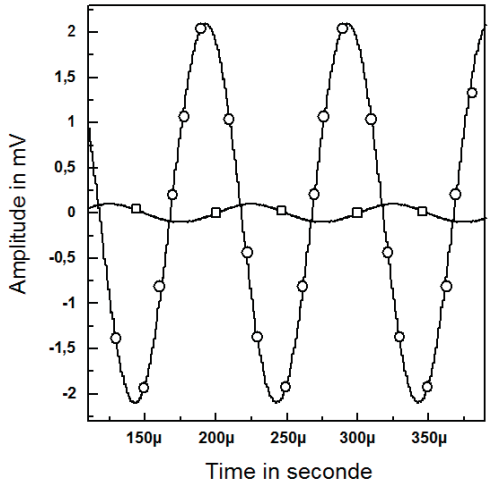


Fig. 11. Input and Output waveforms for the CHS

The consumption current of the circuit was 4 µA. For a supply voltage of ± 1.25 V, this yields a power consumption of 5 µW. A summary of the measured CHS performance is given in Table II.

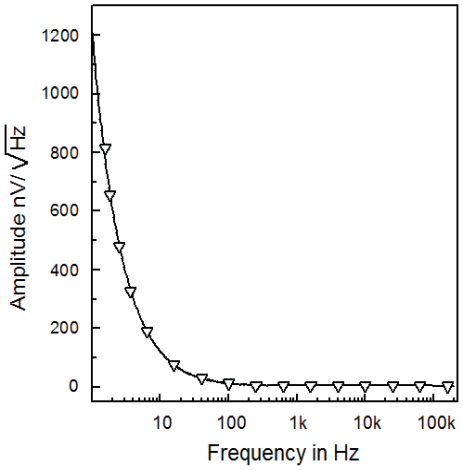


Fig. 12. Input-referred voltage noise spectrum

The PSRR and CMRR of the amplifier was simulated with enabling chopper modulation by sweeping an input voltage V_{in} = 100µV_{pp}. By enabling the chopper modulation scheme, a significant performance improvement is observed resulting in an inband PSRR above 90 dB and a CMRR greater than 120 dB inband. This is due to the fact that any signal that will

couple through the power supply, or the common-mode input to the differential outputs, will only be modulated by the output chopper. Hence these signals will be shifted upwards in frequency to the chopper frequency and its harmonics, where they can be removed by low pass post filtering.

IV. Design Comparison

In this section, we compared a CMOS front-end amplifier dedicated to monitor very low amplitude signal from implantable sensors [5], a low-power low-noise CMOS amplifier for neural recording applications [22] and a 2 µW 100 $nV/\sqrt{Hz}$ chopper stabilized instrumentation amplifier for chronic measurement of neural field potentials [23] to our low noise micro-power chopper amplifier for high resistive MEMS gas sensor. The performance comparison between the proposed CHS and published CHSs is summarized in Table II.

In the proposed CHS, the low power consumption and the low equivalent input referred noise are considered. From the table II we can see the proposed CHS achieved relatively low equivalent input referred noise compared to published CHS in[5], in [22] and in [23]. It has a supply voltage lower than the referred CHS [22] but a little high power consumption than the referred CHS [23]. In both published CHSs, if the power consumption decreases the equivalent input referred noise increase. The contrary is true. The power consumption is inversely proportional to the equivalent input referred noise. However, This CHS achieves a good trade-off between power consumption and input noise.

Compared to the published CHSs, this CHS contains a classic analog CMOS structures like a passive modulator/demodulator, a 2nd order selective Band-Pass-filter with a simple OTA-Miller core, a gain stage with a simple OTA-Miller core and a 1st order passive Low-Pass-filter in the output. Instead of the make of complex analog structures to the published CHSs, we have make a simple CHS containing a classic analog structures that offering very good performances like power consumption and equivalent input referred noise.

TABLE II
COMPARISON OF THE REFERENCE AMPLIFIER AND THIS WORK

	This work	Ref. [5]	Ref. [22]	Ref. [23]
Supply voltage (V)	2.5	1.8	5	1.8 to 3.3
Chopping frequency (kHz)	210	37.6	-	16
Amplifier voltage gain (dB)	26.5	51	40	41
Equivalent input referred noise ($nV/\sqrt{Hz}$)	0.194	56	21	100
Power consumption (µW)	5	775	80	2
Application	MEMS gas sensor	Biomedical sensor	EEG amplifier	EEG amplifier

V. Conclusion

A fully integrated low voltage analog front-end preamplifier dedicated to gas sensors is presented. The chopper modulation technique was chosen to reduce the 1/f noise and DC-offset. It is an efficient way to implement sensors that transduce very weak input signals. The CHS is simulated using transistor model parameters of the AMS 0.35 µm CMOS technology at a ±1.25 V power supply voltage and 26.5 dB voltage gain. At the same simulation condition, the total power consumption is 5 µW only. It achieves a noise floor of 0.194 $nV/\sqrt{Hz}$ within the frequency range from 1 kHz to 10 kHz. Excellent CMRR, greater than 120 dB, and PSRR, about 90 dB, are demonstrated as a consequence of the chopping scheme. This CHS achieves a good trade-off between power consumption and input noise. The circuit features very low offset, low noise, and low power consumption.

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