# Voltage Reference with Programmable Temperature Coefficient and Offset Voltage Compensation

Dominik Gruber, *Student Member, IEEE,* Gerald Hilber, and Timm Ostermann, *Member, IEEE*

***Abstract*—This paper demonstrates an integrated circuit for compensation of errors in voltage references, that not only is able to compensate first order changes of the temperature coefficient, but can also correct for the offset error that is unavoidable in production due to variations in process conditions and mismatches.**

**The temperature compensation circuit is programmable via three control bits, the remaining offset error is compensated by setting eight control bits and an external provided reference voltage. The compensation procedure can be controlled by an internal digital block or via external signals.**

**The actual calibration data can then be saved in several possible ways (EPROM, laser fuses, external Memory, ...).**

**Extensive simulations and measurements show that the described circuit reduces the average temperature error by more than 40% and the overall absolute error by more than 90% wth regards to the uncalibrated reference voltage.**

***Index Terms*—voltage reference, bandgap, temperature coefficient, offset voltage, trimmable, programmable, calibration.**

## I. Introduction

VOLTAGE references act as important buildings blocks in many of today's electronic circuits, like analog-to-digital converters, radio transceivers or generally in any application where a reliable and stable reference voltage is mandatory.

Usually, the voltage drop $V_D$ over a diode or diode-connected bipolar transistor is used to generate a more or less stable reference [1], [2], [3]. Recently, considerate effort was put into finding new circuit design approaches that minimize the existing temperature dependency of these so-called bandgap voltage references (BGR).

First proposals to correct the non-linearity of $V_D$ [4], [5] made it possible to counterbalance the nonlinearities so that the temperature coefficient was lowered to a few $ppm/K$. Since then, more sophisticated methods were developed to further improve the situation [6], [7], [8], [9], [10], [11].

Fig. 1 shows that the temperature characteristics of the diode voltage $V_D$ is manifold and subject to considerable fluctuations of any kind. Changes of the temperature dependency first, second and even third order can be observed due to process variations as shown in Fig. 1. The above mentioned methods are more or less concepts without respect to process variations and mismatch. It is not clear, based on these concepts, how to deal with this influences in mass production.

The situation is made worse due to the fact that there are no real bipolar junction transistors (BJT) available in modern CMOS processes. Instead, BJTs are substituted by using parasitic lateral bipolar transistors [12] which tend to have lower performance [13].

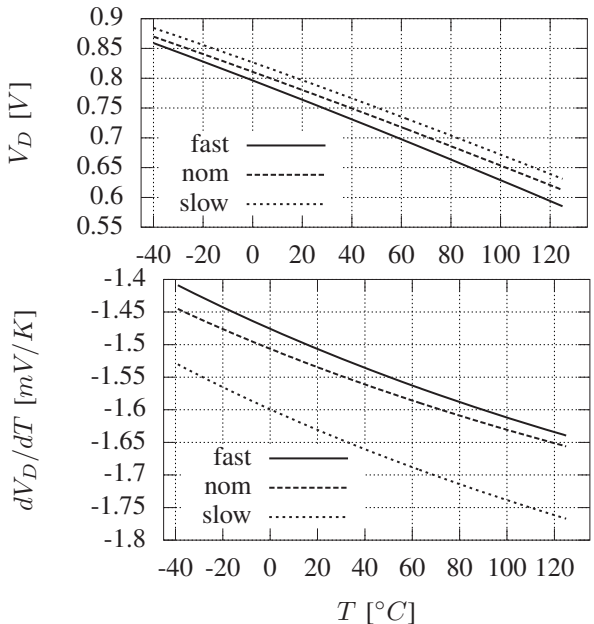


Fig. 1. Temperature characteristics of the diodeconnected BJT due to process variations

In addition to the variations of the voltage $V_D$, mismatch- and process variations (resistor mismatch, offset voltages in operational amplifiers etc.) cause unavoidable offset variations of the output voltage ($V_{\mathrm{BG}}$) of the BGR. In order to keep the initial error of the voltage reference as low as possible, several options are available, e.g. low offset operational amplifiers or chopper op-amps [14], [15]. There is also the possibility to calibrate this error as well.

To keep the cost of such a calibration as low as possible, different methods were proposed to make the output voltage of a voltage reference on-chip trimmable/programmable [16], [17]. We decided to realize a calibration method which is independent to the available options to save the calibration data (internal or external memory, fuses, laser fuses etc).

In this paper we present a new design for a voltage reference with on-chip trimmable temperature coefficient as well as on-chip trimmable offset voltage (Fig. 2) and appropriate simulation and measurement data. The temperature coefficient is trimmable over a wide range via three control bits, the offset of the output voltage is trimmable over the range of more than 250mV via eight control bits.

The circuit was realized in a $3.3V$, $0.25\mu m$ CMOS process. The offset calibration circuit was manufactured and successfully tested in a $0.35\mu m$ (by the authors of [16]) as well as

D. Gruber, G. Hilber and T. Ostermann are with the Institute for Integrated Circuits, JKU - Johannes Kepler University Linz, Austria, e-mail: {gruber, hilber, oster}@riic.at.

in a $0.25\mu m$ process.

This paper is organised in the following way: Section II describes the circuit, section III shows the results from simulations, section IV the measurement results are discussed and section V finally summarizes the findings.

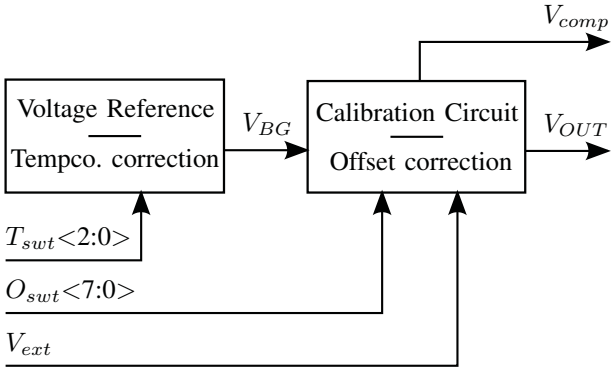


Fig. 2. Block diagramm of the trimmable voltage reference

## II. Circuit Description

In this section the two main building blocks (see Fig. 2) of the voltage reference, the temperature coefficient trimmable bandgap reference (TBGR) and the offset voltage trimmable calibration circuit (OCC) are described in detail.

### A. Trimmable Bandgap Reference - TBGR

Figure 3 shows the implemented bandgap reference with trimmable temperature coefficient, which is based on a concept by Karel Kuijk [2]. The output voltage $V_{\text{BG}}$ can be described by

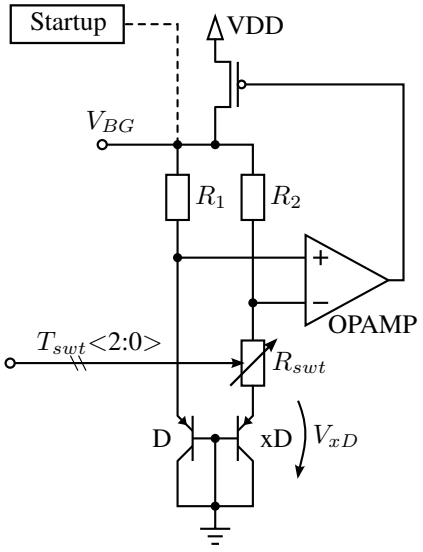


Fig. 3. Schematic of the trimmable bandgap reference

$$V_{BG} = \underbrace{V_{xD}}_{\text{neg. Tempco}} + \underbrace{V_T \cdot \ln(x)\,(1 + R_2/R_{swt})}_{\text{pos. Tempco}} \qquad (1)$$

$V_{\text{xD}}$ is the voltage-drop over the diode-connected bipolar transistors $xD$ and $x$ is the number of bipolar transistors in parallel. $V_T = kT/q$ is the temperature voltage, with $k$ the Boltzmann constant, $T$ the absolute temperature in Kelvin and $q$ the amount of electric charge in Coulomb.

We chose $x$ as 20 for our design. A higher number of parasitic lateral bipolar transistors in parallel is preferable, but this would consume a relatively large area on the ASIC, so $x = 20$ is a good trade-off between performance and die area. Furthermore a transistor ratio of $1/20$ is sufficient to operate both bipolar transistors on different current densities.

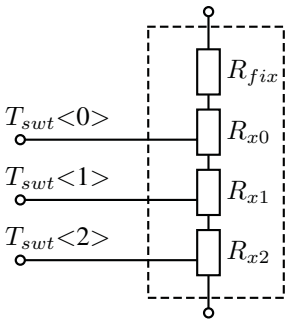


Fig. 4. Block diagram of $R_{swt}$

The resistor $R_{\text{swt}}$ is controlled by three control bits. It consists of one high-value fixed ($R_{fix} \approx 8k\Omega$) and three binary weighted smaller-value resistors (Fig. 4). These are used to change the resistor ratio $R_2/R_{\text{swt}}$ in a sufficiently wide range. The possible range of trimmable temperature coefficients is shown in Fig. 5.

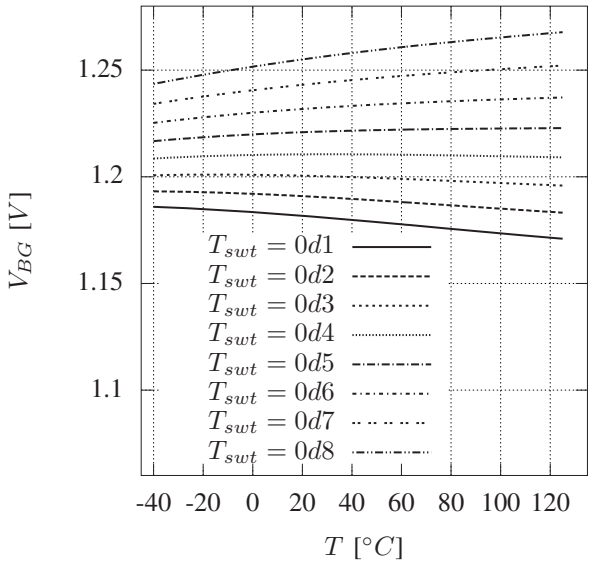


Fig. 5. Simulated range of the calibratable temperature coefficient of output voltage $V_{BG}$ of the TBGR

Depending on the adjusted compensation, the resistors $R_x$ are either bypassed by low resistor transmission gates, or not (see Fig. 6). In each case a transmission gate (T-gate) is in the current path. The T-gate in the resistor branch is used as a dummy device. We chose this concept, because there

are always three T-gates connected in series. Therefore the temperature behavior is almost independent to the control bits $T_{swt}$<2:0>.

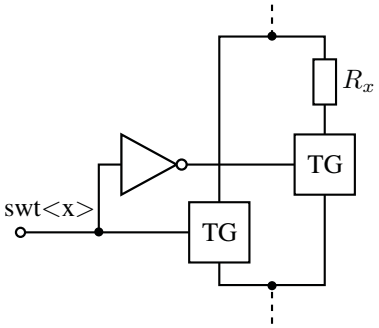


Fig. 6. Block diagram of a single resistor element of $R_{swt}$

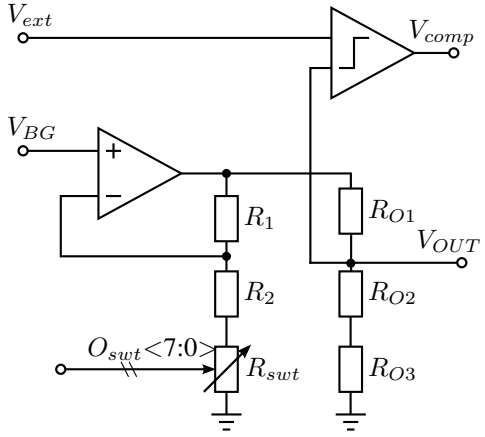


Fig. 7. Schematic of the offset calibration circuit

To circumvent BGRs to get "stuck" in the stable state $V_{\text{BG}} = 0V$, additional startup circuits are commonly used. We decided to use a simple continuous-conduction method as proposed in [7]. This kind of startup is very small (one transistor is enough), and is reliable. Simulations showed stable startup with minimal supply voltage and temperatures down to $-40°C$.

### *B. Offset Calibration Circuit - OCC*

The offset calibration circuit is shown in Fig. 7. It utilizes a non-inverting amplifier with on-chip trimmable amplification factor. By default the gain of the amplifier is set to approximately 2, so the output voltage of the bandgap reference $V_{\text{BG}}$ is amplified to $2.5V$. With an corresponding voltage divider (resistors $R_{\text{Oi}}$ in figure 7), the output of the overall voltage reference (TBGR + OCC) $V_{\text{OUT}}$ can be set to any voltage value between $2.5V$ an $0V$. This concept is chosen to decouple the influence of the load on the calibration and feedback mechanism. Another advantage of this concept is the possibility to optimize each resistance ladder of different voltage references due to their different requirements (resistance step size, crowbar current, ...). For example, if one needs a voltage reference with $V'_{\text{OUT}} = 1.6V$, only the resistor ladder consisting of the resistors $R_{\text{Oi}}$ needs to be changed. The most critical parts of the voltage reference can be easily reused.

The output voltage is set to $2.0V$ in our circuit. The resistor $R_{\text{swt}}$ is programmable via eight control lines. The calibration range of the OCC is big enough to compensate for offset variations of the TBGR and offset errors introduced by the resistors in the output voltage dividers ($R_1$, $R_2$, $R_{\text{swt}}$, $R_{\text{Oi}}$) due to local (mismatch) and global process variations.

The main principle of the calibration resistors $R_{\text{swt}}$ in Fig. 7 is the same as in the trimmable bandgap voltage reference (TBGR) (Fig. 3). It consists of eight binary incremented resistors, which can be bypassed by a low resistance transmission gate. The concept of T-gates and dummy-T-gates is the same as explained in section II-A (Fig. 6).

This arrangement allows to change the output voltage in the range of approximately $235mV$ around the nominal value. Eight control bits (256 different calibration states) theoretically imply an offset error of the output voltage at the calibration temperature of approximately $\pm 0.5mV$. Due to process and mismatch variations in the resistor $R_{\text{swt}}$ some calibration states overlap. The effective offset error of the offset calibration circuit is approximately $\pm 0.5mV \ldots \pm 1.5mV$.

In order to calibrate the offset, a comparator is included to the OCC. It compares the output voltage of the reference circuit ($V_{\text{OUT}}$) with a stable externally provided voltage ($V_{\text{ext}}$). As soon as the automatic calibration procedure is started, an internal digital block increases the output voltage, through the digital input $O_{swt}$<7:0>, as long as the comparator output is low. As the voltage $V_{\text{OUT}}$ rises above $V_{\text{ext}}$, the comparator output also switches to high level and the calibration procedure stops [16]. The actual value of $O_{swt}$<7:0> can then be saved in several possible ways (EPROM, laser fuses, external Memory, ...).

In addition to this automatic calibration process the voltage VREF can be directly controlled by a Three-Wire-Interface (TWI). This feature is included for test purposes to directly set every calibration state without having to wait for the automatic calibration to finish. The advantage of this method is the direct and fast adjustability of the reference output voltage VREF, although a communication protocol has to be implemented for the calibration process.

## III. Simulation Results

### *A. Trimmable Bangap Reference*

Figure 8 shows the dependency of the bandgap output voltage $V_{BG}$ (default calibration state $T_{swt}$<2:0>$= 0b001$) on different process corner. According to Fig. 1 the fast corner has the lowest temperature coefficient, the slow corner the highest.

In order to determine the behavior of $V_{\text{BG}}$ according to process and mismatch variations, a Monto-Carlo analysis was performed. Fig. 9 shows the results of an untrimmed TBGR (or rather a bandgap reference circuit in default calibration state). The offset voltage varies up to $\pm 50mV$, the temperature coefficient between 10 to $117ppm$. The error of the tempco is [18]

$$E_{\text{ppm}} = \left( \frac{V_{\text{max}} - V_{\text{min}}}{V_{\text{nom}} \cdot (T_{\text{max}} - T_{\text{min}})} \right) \cdot 1x10^6 \qquad (2)$$

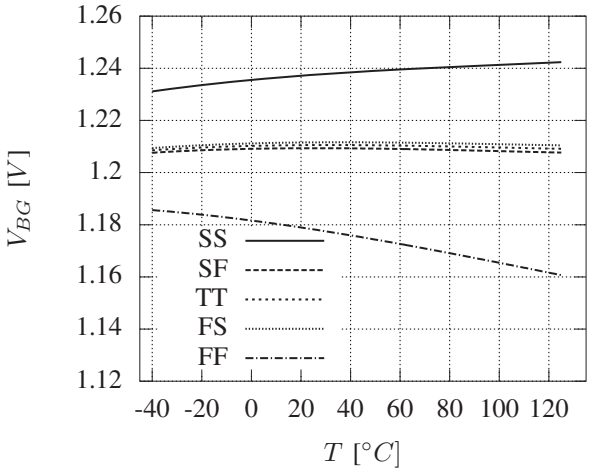


Fig. 8. Change of the temperature coefficient of TBGR due to process variations

$V_{\text{nom}}$ is the value of $V_{\text{BG}}$ at $27°C$.

Figure 10 shows the same simulation with a temperature coefficient trimmed TBGR. The offset still varies up to $\pm 40mV$, but the temperature stability is increased. The resulting error $E_{\text{ppm}}$ is between 6 and $42ppm$. The average error improves by more than 40%.

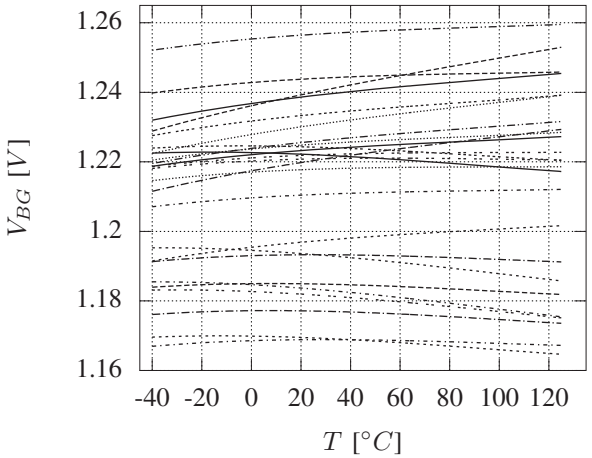


Fig. 9. Monte-Carlo analysis of a untrimmed TBGR output voltage

Figure 11 compares the two approaches: The untrimmed error is pictured in gray, the error of the trimmed TBGR is black. Run number 11 depicts a simulation run which could not be optimally compensated.

### *B. Offset Calibration Circuit*

Figure 7 describes the offset calibration circuit (OCC) that is used to compensate the remaining offset error. In order to characterize only the OCC, the trimmable bandgap voltage reference is replaced by an ideal voltage source with $V_{\text{OUT}} = 1.21V$.

Figure 12 shows some examples of the output voltage $V_{\text{OUT}}$ over a temperature range of $165°K$. The curves for the calibration states for minimum, maximum output voltage and some states in between are shown.

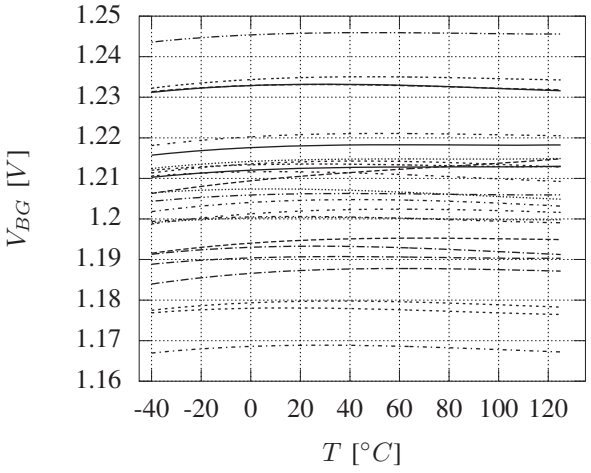


Fig. 10. Monte-Carlo analysis of a trimmed TBGR output voltage

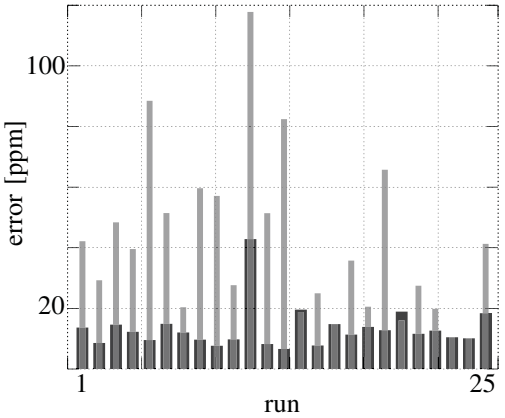


Fig. 11. Tempco of TBGR in ppm, befor (gray) and after trimming (black)

The overall calibration range of the OCC is about $235mV$. Given an amplification factor of $\approx 2$, an offset variation of about $\pm 55mV$ of the TBGR can be successfully compensated.

It is noteworthy that the curvature regarding temperature is inverse proportional to the bangap reference. This improves the curvature of the overall circuit to a certain extent.

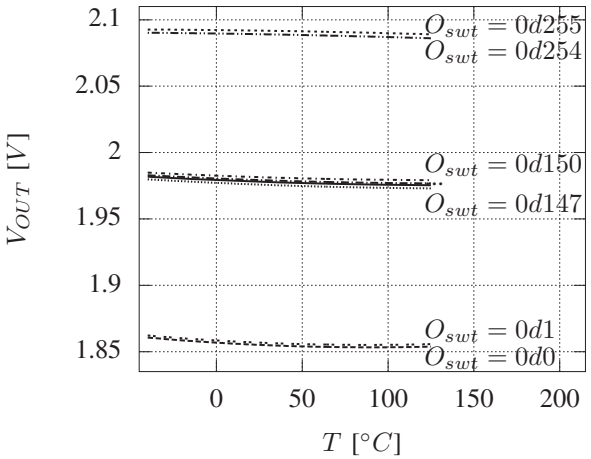


Fig. 12. Simulated offset calibration range ($O_{swt}$=0 (min), $O_{swt}$=255 (max) and some sample values in between ($O_{swt}$=1, 147, 148, 149, 150, 254))

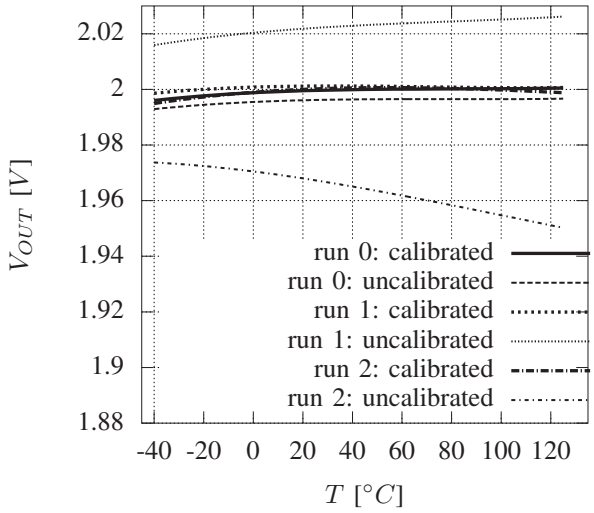


Fig. 13. Three simulation examples for offset and tempco calibration (uncalibrated curves are slashed, calibrated curves solid)

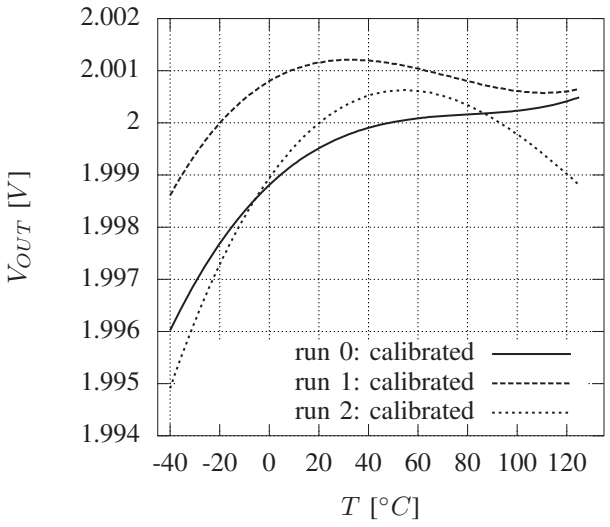


Fig. 14. Detailed view of the three examples for offset and tempco calibration (calibrated curves only)

### C. Overall Reference Circuit

Figure 13 demonstrates three examples of the overall output voltage $V_{\mathrm{OUT}}$ of the whole circuit, combining the trimmable bandgap voltage reference (TBGR) and the offset calibration circuit (OCC). The temperature coefficient and the offset of the untrimmed output voltage vary considerably.

In the next step, the compensation procedure was performed by compensating the temperature coefficient, followed by reducing the remaining offset. Corresponding curves are shown in Fig. 13. Figure 14 shows the calibrated curves in detail.

The uncalibrated output voltage varies from $+26mV$ to $-50mV$. The calibration reduces the error to $+1mV$ to $-5mV$ over the temperature range from $-40°C$ to $+125°C$, therefore reducing the absolute error to 8% of the original value.

Figure 15 shows the implemented layout.

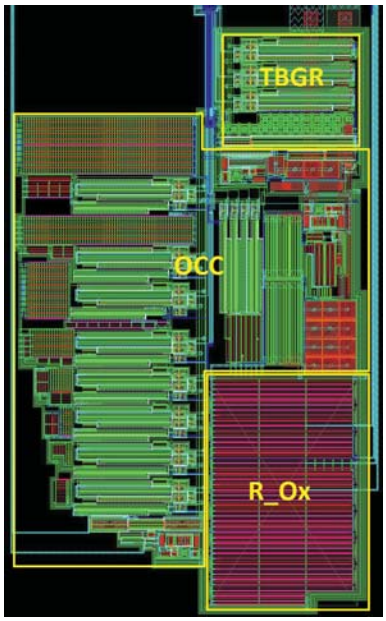


Fig. 15. Layout of the proposed voltage reference

## IV. Measurement Results

To assess the overall performance of the proposed programmable voltage reference circuit a corner lot of nine wafers was manufactured. One wafer is manufactured at nominal process conditions, the remaining eight wafers are intentionally produced at selected process corners:

- TT: typical case
- FF: all MOSFET have minimal threshold voltages
- SF: all n-type MOSFET have maximal and all p-type MOSFET have minimal threshold voltages
- FS: all n-type MOSFET have minimal and all p-type MOSFET have maximal threshold voltages
- SS: all MOSFET have maximal threshold voltages
- HRES: all used resistors have maximum values
- LRES: all used resistors have minimum values
- LGL: gate length larger than nominal value
- SGL: gate length smaller than nominal value

All measurements were done using a nominal supply voltage $V_{DD} = 3.3V$.

### A. Trimmable Bandgap Reference - TBGR

Fig. 16 shows a typical measurement of the trimmable temperature coefficient. The offset compensation was set to default ($O_{swt}$<7:0>= $0d124$). A proper temperature compensation for the example in Fig. 16 is Tswt = 0d2. As a consequence the temperature coefficient is calibrated to approximately $\pm 4mV$ over a temperature range of $165°C$.

### B. Offset Calibration Circuit

Fig. 17 demonstrates the offset calibration capabilities of the circuit. All combinations of the switch settings of the offset calibration circuit were triggered. Temperature compensation was set to a default value ($T_{swt}$<2:0>= $0d4$). The offset

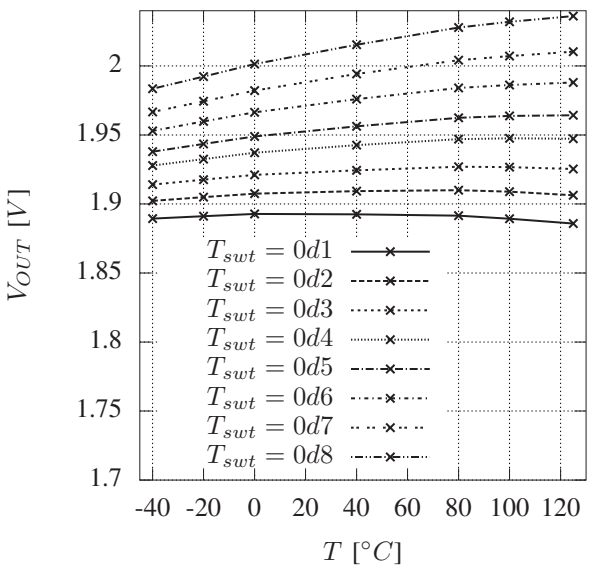


Fig. 16. Measurement of the trimmable temperature coefficient of the overall circuit (with untrimmed offset)

can therefore be corrected over approximately $215mV$ accordingly.

The larger steps in the data shown in Fig. 17 occur if larger MSB values are switched (e.g. from value 0d127 (0b0011 1111) to 0d128 (0b0100 0000)). Although the layout uses unit cell resistors for $R_x$, mismatch effects due to other parasitic resistances (e.g. metal interconnects) exist. Because of the fact that the voltage drop is always negative at this larger steps, no missing calibration code occurs.

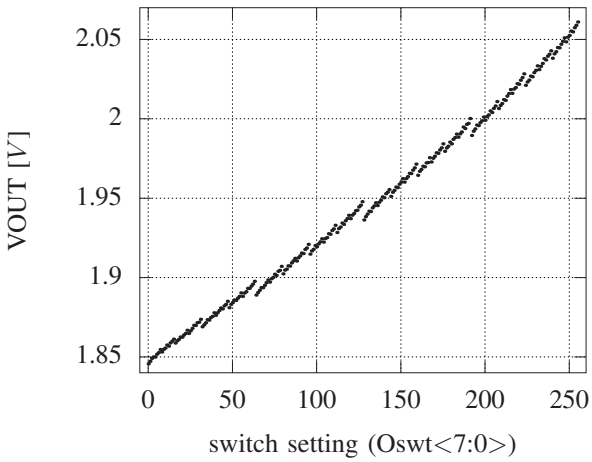


Fig. 17. Measurement of the offset calibration of the overall circuit (with untrimmed temperature coefficient)

Fig. 18 shows how accurate the offset calibration can be. It displays 38 single measurements of the offset calibrated output voltage $V_{OUT}$ at room temperature. Measurement 1-4 and 35-38 are from a typical (TT) wafer, 5-8 from a fast (FF) wafer, 9-12 from a SF wafer, 13-16 from a FS wafer, 17 and 18 from a HRES wafer, 19-22 from a LRES wafer, 23-26 from a SGL wafer, 27-30 from a LGL wafer and measurements 31-34 are from a slow (SS) wafer. This optimal calibration states are found via the Three-Wire Interface, because the simple automatic calibration process used here not always gives the optimal value, but only the first value which is bigger than the value of $V_{ext}$, which is not always the best value due to mismatch.

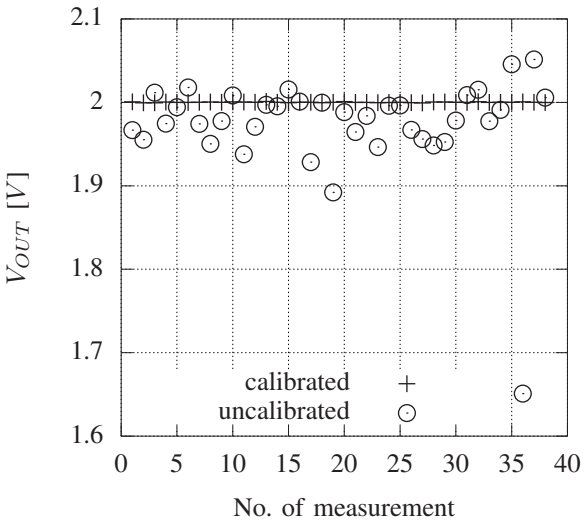


Fig. 18. Measurement of 38 different corner chips: Comparison between uncalibrated and optimally offset calibrated output voltages at $V_{DD} = 3.3V$ and $T = 25°C$.

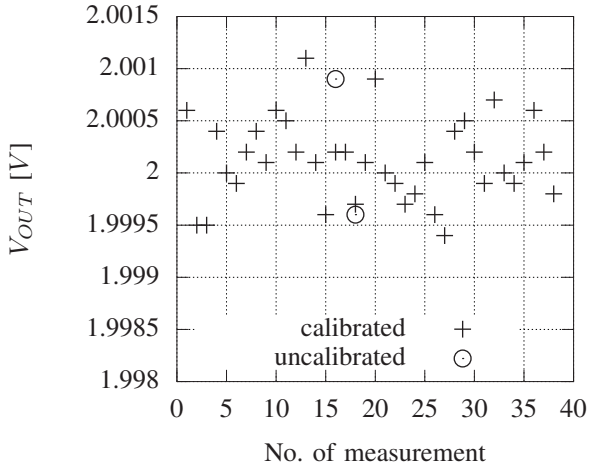


Fig. 19. Measurement of 38 different corner chips: Comparison between uncalibrated and optimally offset calibrated output voltages at $V_{DD} = 3.3V$ and $T = 25°C$.

Fig. 19 shows a more detailed view of Fig. 18. The reference output voltage $V_{OUT}$ can be set to values from $+1.1mV$ to $-0.6mV$ around the desired $2V$.

### C. Overall Reference Circuit

The temperature and offset calibration is accomplished by following three steps:

1) measurement of $V_{OUT}$ with all possible switch settings of $T_{swt}$<2:0> at an ambient temperature of $\approx 80°C$ and a default offset compensation $O_{swt}$<7:0>$= 0d124$: $V_{OUT}|_{T=80°C,Tswt=0...7}$

2) measurement of $V_{OUT}$ with all possible switch settings of $T_{swt}$<2:0> at an ambient temperature of $\approx 40°C$ and a default offset compensation $O_{swt}$<7:0>$= 0d124$: $V_{OUT}|_{T=40°C,Tswt=0...7}$
3) calculation the optimal switch setting for $T_{swt,opt}$<2:0> by selecting the one with the smallest delta.
4) calibrating for the offset error with the calculated $T_{swt,opt}$<2:0> set.

Fig. 20 shows five measurements of the temperature and offset calibrated output voltage $V_{OUT}$. The curves marked with 'O' are the uncalibrated, the curves marked with '+' are the calibrated reference voltages. The offset calibration was carried out with the automatic calibration process (see section II-B).

The overall accuracy of the reference circuit can be reduced from $-12mV \ldots -78mV$ to $+4mV \ldots -6mV$ around the desired $2.000V$ over a temperature range of $165°K$.

Fig. 21 shows a photograph of the manufactured die with the voltage reference.

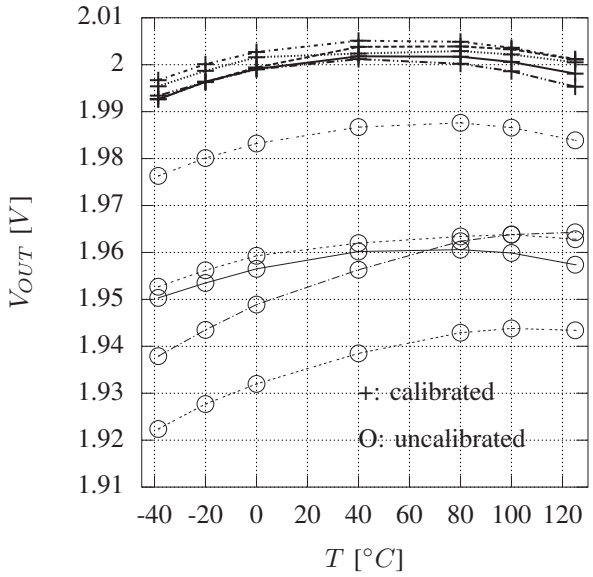


Fig. 20. Measurement of five different typical chips: Comparison between uncalibrated and calibrated output voltages at $V_{DD} = 3.3V$ and $T = 25°C$. Both temperature coefficient and offset were compensated.

## V. Conclusion

This paper demonstrates a circuit for compensation of the temperature errors in voltage references, that not only is able to compensate gradient changes of the temperature coefficient, but can also correct for the offset error that is unavoidable in production due to variations in process conditions and mismatches.

We show that the proposed calibration circuit is able to counterbalance changes in the temperature coefficient and appearing offset errors accordingly.

Extensive simulations and measurements demonstrate that the performance of the proposed circuit is superior to untrimmed alternatives.

Further work will concentrate on increasing the range and accuracy of temperature coefficients that can be compensated and on the ease of the calibration procedure.

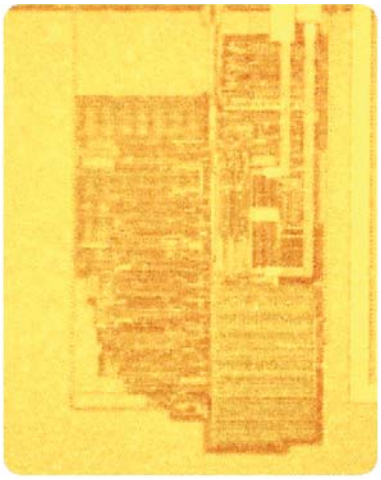

Fig. 21. Chip photo of the proposed voltage reference

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**Dominik Gruber** was born in Linz, Austria in 1980. He received the Dipl.-Ing. (Graduate Engineer) degree in Mechatronics from the Johannes Kepler University of Linz, Linz, Austria, in 2007, and is currently working toward the Doctoral degree (Ph.D.) at the Johannes Kepler University of Linz. In 2007, he joined the Institute for Integrated Circuits, Johannes Kepler University of Linz. His research interests concern the field of temperature sensors and integrated references with a focus on programmable voltage references.

**Gerald Hilber** was born in Linz, Austria in 1978. He received the Dipl.-Ing. degree in mechatronics from the Johannes Kepler University of Linz in 2008. He is currently a Ph.D. candidate at the Johannes Kepler University. In 2005 he joined the Institute for Integrated Circuits at the Johannes Kepler University in Linz. His research interests include the design and testing of analog and mixed-signal integrated circuits.

**Timm Ostermann** received the Dipl.-Ing. degree in Electrical Engineering from the Technical University of Hamburg-Harburg, Germany, in 1993, the Dr. techn. (Ph.D) degree and the Univ.-Doz. (Habilitation) degree both from the Johannes Kepler University Linz (JKU), Austria, in 1999 and 2004, respectively. From 1994 to 2000 he was with the Department of Microelectronic Systems, Institute of Systems Science and from 2000 he is with the Institute of Integrated Circuits both at the University of Linz. He is currently Assoc. Professor at the JKU and deputy head of the Institute for Integrated Circuits. His research work includes the modelling and characterisation of SiGe-MODFETs and organic transistors as well as organic solar cells for circuit design and the design of, analog, RF and mixed analog digital integrated circuits. His current research interests are robust CMOS design aspects as well as design methods for analog/mixed-mode and RF circuit synthesis.