Towards a g_m/I_D Design Methodology for Polymer-based Organic Thin Film Transistors

Frédéric Zanella, Adrian von Mühlenen, Zbigniew Szamel, Giovanni Nisato, Christian Enz, and Jean-Michel Sallese

Abstract—In this paper we show based on experiments that an invariant representation exists for various polymer-based solution processable organic thin film transistors (OTFTs). Despite the fact that this technology suffers from a non-negligible spread of parameters, all experimental data exhibit low dispersion when represented in a g_m/I_D versus I_D diagram. This result is important for circuit design strategy based on the g_m/I_D representation, giving more insight into analogue design methodology. In addition, the g_m/I_D invariant can also be used to extract the gate voltage mobility dependence that is inherent to organic field effect transistor.

Index Terms—OFET, OTFT, g_m/I_D , P3HT, PTAA.

I. INTRODUCTION

 $\bf E$ VER since the first organic field-effect transistors (OFETs) were reported, the interest in this field has steadily risen, especially for solution processable polymer semiconductors. Indeed this technology allows producing low-cost and flexible circuits through the combination of low temperature processing ($T<200\,^{\rm o}{\rm C}$ in this work) - thus compatible with flexible substrates - and high-throughput fabrication techniques such as roll-to-roll.

Among the applications embedding OTFTs reported so far, three main areas stick out: active matrix as backplane in flexible displays, disposable flexible RFID tags and more recently A/D and D/A converters opening the way to front-end signal processing e.g. for sensors. More details can be found in these recent reviews [1]–[7].

Performance-wise, OFETs, and more especially the polymer-based TFTs, exhibit field-effect mobility at minimum three orders of magnitude lower than inorganic crystalline silicon-based MOSFETs, but nowadays they can compete with amorphous hydrogenated (a-Si:H) TFTs [3]. Compared to MOSFETs, OFET operates in accumulation only. Similarly, the threshold voltage becomes meaningless and a turn-on voltage V_{to} (also called switch-on voltage) is preferred instead. It can be defined as the voltage where the channel conduction starts rapidly increasing over the off-current [8]. However, off-currents in OFET are mainly due to bulk current and gate

F. Zanella and C. Enz are with Centre Suisse d'Electronique et de Microtechnique, CSEM SA, Mattenstrasse 22, 4016 Basel, Switzerland and School of Electrical Engineering, Swiss Federal Institute of Technology, EPFL, Station 11, 1015 Lausanne, Switzerland (email: frederic.zanella@csem.ch).

A. von Mühlenen, Z. Szamel and G. Nisato are with Centre Suisse d'Electronique et de Microtechnique, CSEM SA, Mattenstrasse 22, 4016 Basel, Switzerland.

J.-M. Sallese is with School of Electrical Engineering, Swiss Federal Institute of Technology, EPFL, Station 11, 1015 Lausanne, Switzerland.

leakage current [9]. Nevertheless, V_T is still a benchmark through the classical Extrapolation in the Linear Region (ELR) or Extrapolation in the Saturation Region (ESR) methods.

The field-effect mobility in OTFTs is not constant and strongly depends on the gate voltage [10]. However, as for V_T , the constant linear and saturation field-effect mobilities - μ_{lin} and μ_{sat} , respectively - are commonly used as benchmarks. The contact resistance is also an inherent limitation to OFETs performances due to the energy level mismatch between the organic semiconductor band and the work function of the contact metal. There is indeed for example a potential contact resistance due to the P3HT-Au Schottky barrier of 0.3 eV, in the best case [11].

One of the reasons why OFETs are not yet widely used in working circuits is their large spread of performance parameters such as threshold voltage and mobility. Indeed, a large variability occurs in both batch-to-batch and device-to-device scales. This makes the design of analogue/digital blocks particularly challenging. Therefore, a different approach is needed for the designer in order to compete with the before mentionned variability issues. In the following sections, we propose to investigate this aspect and set the basis for a g_m/I_D design methodology for organic electronics.

II. THE g_m/I_D DESIGN METHODOLOGY FOR OFETS

The g_m/I_D ratio characterizes the transconductance of a transconductor obtained for a given current level [12]. It can hence be used as a figure-of-merit (FoM) to compare the current-efficiency of different transconductors. Together with the inversion coefficient I_C defining the state of inversion of the channel, it can also be used to properly size transistors according to initial specifications such as gain, bandwidth, noise, etc. [12]–[14]. For silicon MOSFETS, the g_m/I_D characteristic versus the inversion coefficient has this unique property to remain invariant to process parameters (for long-channel devices).

This paper investigate whether such an invariant property also exists for polymer-based OFETs, despite their different current transport mechanism. A few attempts have been done to analyze the g_m/I_D characteristics for small molecules OTFTs. In Ref. [6], Murmann et al. attempted a comparison of DNTT [15] OFETs with simulated 0.35 μ m MOSFETs. But these did not bring a strong evidence for any kind of FoM that would deserve design in a large sense. To this purpose, we

have extracted the g_m/I_D from measurements and tried to find a proper normalization current similar to the specific current used for silicon MOSFETs [12]. As will be shown later, this will also allow characterizing the mobility bias dependence.

A. Sample fabrication

In order to cover a broad range of organic devices, 70 OTFTs based on both standard bottom-gate bottom-contacts and top-gate bottom-contacts architectures - see insets in Fig. 1 and Fig. 2, respectively - have been fabricated using two polymer semiconductors and four inorganic/organic gate dielectrics as summarized in Table I.

TABLE I Description of the used stacks. * (C): common, (P): patterned

Designation	BG1	BG2	BG3	TG1	TG2
Architecture	BG-BC	BG-BC	BG-BC	TG-BC	TG-BC
Gate contact*	Al/n-Si	n-Si	ITO	Al	Al
	(C)	(C)	(P)	(P)	(P)
(nm)	-	-	75	70	70
Dielectric	SiO2	SiO2	PVP	Cytop	D139
$C_i \; (\mathbf{nF/cm}^2)$	33	15	13	7	6
Surface	OTS	HMDS	-	-	-
treatment					
S/D contacts	Ti/Au	TiW/Au	Au	Ti/Au	Ti/Au
(nm)	5/60	5/30	60	5/50	5/50
Semiconductor	P3HT	PTAA	P3HT	P3HT	P3HT

The chosen organic semiconductors are regioregular poly(3-hexylthiophene) (P3HT) and polytriarylamine (PTAA) because of their well-known p-type properties, [16] and [17], respectively. PTAA displays a lower mobility compared to P3HT, however it is air-stable. P3HT has been supplied by Merck[®] (LisiconTMSP001, 10mg/mL in anhydrous chloroform) as well as PTAA (LisiconTMSP006, 7mg/mL in toluene). PTAA was annealed 2 min at 100 °C but not P3HT.

For samples BG1 and BG2, highly phosphorus doped silicon wafers with thermally grown silicon dioxide (SiO2) are used as both substrate and gate dielectric. Self-assembled monolayers are used to passivate the oxide surface [18]: octadecyltrichlorosilane (OTS) and hexamethyldisilazane (HMDS). OTS is deposited by dip-coating and HMDS by vapor deposition.

For all the other samples, glass substrates and three commercially available polymer dielectrics are used: cross-linked poly(4-vinyl phenol) (PVP, Aldrich® 436224) [19], diluted Cytop® CTL 809A and Merck® LisiconTMD139-FC43-045 (D139). Each polymer layer - PVP, Cytop, D139, P3HT and PTAA - is deposited by spin-coating in inert (N₂) atmosphere, or in air for PVP, without any further patterning process.

Source and drain contacts are patterned via photolithography. The bottom gate electrode of BG3 is a solid solution of indium(III) oxide and tin(IV) oxide (ITO) which is also photolithography patterned. Aluminum top gate electrodes are defined by shadow mask technique.

The transistors reported here are part of different layouts and topologies e.g. finger transistors and interdigitated transistors.

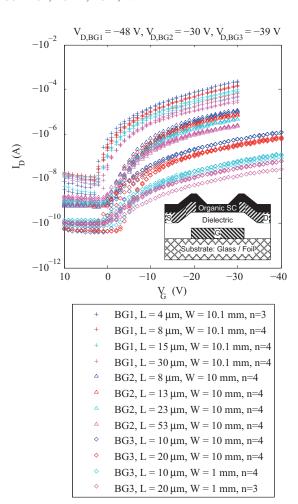


Fig. 1. Transfer characteristics in saturation regime (bottom-gate). L: channel length. W: channel width. n: number of OTFTs plotted.

B. Electrical characterization

A fully automated setup designed by CSEM including an Agilent 4155C was used to measure, in inert atmosphere, the transfer and output characteristics and to extract the performance parameters according to the IEEE 1620 standard [20]. The different insulator capacitances C_i were measured using an HP 4192 and the values are listed in Table I.

III. RESULTS AND DISCUSSION

The transfer characteristics in saturation regime are plotted for the transistors used in this work. They are divided in two groups for readability reasons: bottom-gate and top-gate transistors are plotted in Fig. 1 and Fig. 2, respectively.

The transfer curves show that the studied samples exhibit distinct characteristics in terms of performances and V_{to} , although four samples are made from the same semiconductor. Secondly the off-current does not scale in W/L and this has to be kept in mind for the normalized g_m/I_D plots addressed in the next section. For bottom-gate transistors, e.g. BG1 and BG2, the off-current is one order of magnitude higher than for BG3 (see Fig. 1). This can be attributed to the patterned gate electrode that limits current leakages. Note that patterning

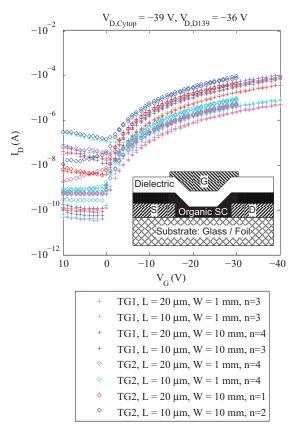


Fig. 2. Transfer characteristics in saturation regime (top-gate)

the gate dielectric and the semiconductor also help to further reduce these leakages, although this it is not the point of this paper.

Thirdly, for a given set of identical transistors, e.g. "BG1, L=30um, W=10.1mm, n=4", Fig. 1 reveals a spread of performance parameters on the very same substrate which is very problematic for circuit design using OTFTs. Performancewise, transistors from sample BG1 are better than those from sample BG3, but also have broader statistical distributions for maximal drain current and saturation mobility, see Fig. 3. This can be attributed to variations of surface modification using silanes.

The $g_m/|I_D|$ versus I_D characteristics are plotted in Fig. 4. Each curve can be clearly decomposed in two asymptotes: one vertical dealing with off-currents, and one showing a slope close to the theoretical limit calculated in silicon MOSFETs, $\propto 1/\sqrt{|I_D|}$. This last point will be discussed in the next section.

A. Normalization of the g_m/I_D versus I_D characteristics

The classical silicon approach has been used to start normalizing the g_m/I_D characteristics using W/L which gathers and sorts group of curves per sample. Then C_i and a constant μ_{FE} have been added to compare samples together [12]. As a first step, the sample scale was considered saying that the mean measured value of μ_{sat} was used as μ_{FE} for each sample which forms already a common group of curves. Finally each

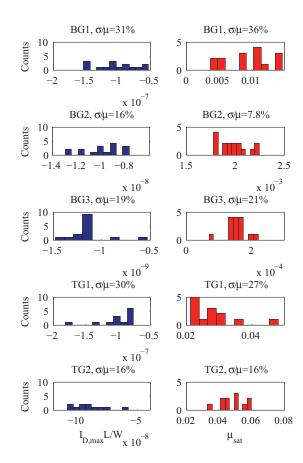


Fig. 3. Distribution of (left) maximal normalized drain current $\frac{L}{W}I_D(V_{GS,max},V_{DS,max})$ (A) and (right) saturation mobility μ_{sat} (cm²/Vs)

value of μ_{sat} has been applied on the respective transistor and the results of this last step are plotted in Fig. 5.

B. Analytical discussion

As visible in Fig. 5, some transistors and especially the TFTs on BG2 follow the ideal $|I_D|^{-0.5}$ asymptote accurately, however the asymptote of the majority of OTFTS tends to $|I_D|^{-0.4}$. At this point, we assume that this might be attributed to the gate-voltage dependence of the mobility, since this is indeed very peculiar to organic FETs. We will now discuss this point using a commonly used power law description of the gate voltage dependency of the mobility i.e. the variable range hopping (VRH) model [21], [22] where x is the position considered along the channel from drain to source and where we set $V_{AA} = 1V$ for sake of simplicity.

$$\mu_{VRH}\left(V_{GS}, x\right) = \mu_0 \left(\frac{V_{GS} - V_{to} - V(x)}{V_{AA}}\right)^{\gamma} \tag{1}$$

We are now going to extract the parameters μ_0 and γ for the VRH approach using the asymptotic behavior of the normalized g_m/I_D representation in Fig. 5. Therefore we write:

$$\frac{g_m}{|I_D|} = 0.79 \left[I_D \frac{L}{WC_i \mu_{sat}} \right]^{-0.4}$$
 (2)

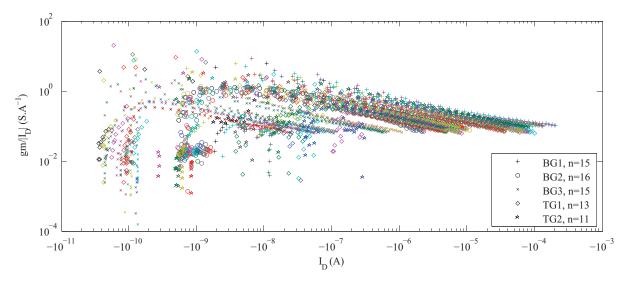


Fig. 4. g_m/I_D versus I_D characteristics

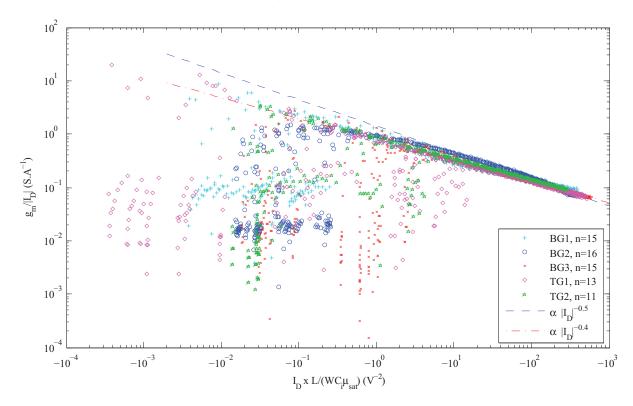


Fig. 5. Normalized g_m/I_D versus I_D characteristics

Even though OFETs operation is quite different from MOS-FET principles, it is quite common to rely on the classical MOSFET equations (in strong inversion). As a starting point, the absolute drain current in saturation regime using (1) writes:

$$|I_D| = \frac{W}{L(\gamma + 2)} C_i \mu_0 |V_{GS} - V_{to}|^{\gamma + 2}$$
 (3)

In other words, $g_m/|I_D|$ generally writes:

$$\frac{g_m}{|I_D|} = (\gamma + 2) \left(\frac{W}{L(\gamma + 2)} C_i \mu_0 \right)^{\frac{1}{\gamma + 2}} |I_D|^{\frac{-1}{\gamma + 2}}$$
 (4)

$$= (\gamma + 2) \left(\frac{\mu_0}{(\gamma + 2)\mu_{sat}}\right)^{\frac{1}{\gamma + 2}} \left[|I_D| \frac{L}{WC_i\mu_{sat}}\right]^{\frac{-1}{\gamma + 2}}$$
(5)

Comparing with (2), we deduce the VRH parameters: $\gamma=0.5$ and $\mu_0=0.14\mu_{sat}.$

IV. CONCLUSION

In this paper we show experimentally that a quasi-invariant g_m/I_D characteristic exists for solution processable organic transistors based on both regioregular P3HT and PTAA polymer semiconductors. Not only, this observation is very interesting from a designer point of view, but we found that it could also be used to extract the VRH model coefficients of the gate voltage-dependent mobility.

ACKNOWLEDGMENT

The authors wish to thank Neeraj Adsul and all people at CSEM who contributed in the lab. This work was partially supported by European Community's Seventh Framework Programme (FP7/2007-2013) under grant agreements n°247978 and n°247745.

REFERENCES

- G. Gelinck, P. Heremans, K. Nomoto, and T. D. Anthopoulos, "Organic transistors in optical displays and microelectronic applications," *Advanced Materials*, vol. 22, no. 34, p. 37783798, sept 2010.
- [2] H. Sirringhaus, "Materials and applications for solution-processed organic field-effect transistors," *Proceedings of the IEEE*, vol. 97, no. 9, pp. 1570–1579, sept 2009.
- [3] R. A. Street, "Thin-film transistors," Advanced Materials, vol. 21, no. 20, pp. 2007–2022, may 2009.
- [4] A. Dodabalapur, "Organic and polymer transistors for electronics," *Materials Today*, vol. 9, no. 4, pp. 24–30, april 2006.
- [5] D. de Leeuw and E. Cantatore, "Organic electronics: Materials, technology and circuit design developments enabling new applications," *Materials Science in Semiconductor Processing*, vol. 11, no. 5, pp. 199–204, oct 2008.
- [6] B. Murmann and W. Xiong, "Design of analog circuits using organic field-effect transistors," in *IEEE/ACM International Conference* on Computer-Aided Design (ICCAD), San Jose, CA, USA, 2010, pp. 504–507
- [7] M. E. Roberts, A. N. Sokolov, and Z. Bao, "Material and device considerations for organic thin-film transistor sensors," *Journal of Materials Chemistry*, vol. 19, no. 21, pp. 3351–3363, sept 2009.
- [8] E. J. Meijer, C. Tanase, P. W. M. Blom, E. van Veenendaal, B.-H. Huisman, D. M. de Leeuw, and T. M. Klapwijk, "Switch-on voltage in disordered organic field-effect transistors," *Applied Physics Letters*, vol. 80, no. 20, p. 3838, 2002.

- [9] H. Jia, S. Gowrisanker, G. K. Pant, R. M. Wallace, and B. E. Gnadea, "Effect of poly (3-hexylthiophene) film thickness on organic thin film transistor properties," *The Journal of Vacuum Science and Technology* A, vol. 24, no. 4, p. 12281232, 2006.
- [10] J.-F. Chang, H. Sirringhaus, M. Giles, M. Heeney, and I. McCulloch, "Relative importance of polaron activation and disorder on charge transport in high-mobility conjugated polymer field-effect transistors," *Physical Review B*, vol. 76, no. 20, nov 2007.
- [11] L. Bürgi, T. J. Richards, R. H. Friend, and H. Sirringhaus, "Close look at charge carrier injection in polymer field-effect transistors," *Journal of Applied Physics*, vol. 94, no. 9, p. 61296137, nov 2003.
- [12] C. C. Enz and E. A. Vittoz, Charge-Based MOS Transistor Modeling -The EKV Model for Low-Power and RF IC Design, 1st ed. John Wiley, aug 2006.
- [13] D. Binkley, Tradeoffs and Optimization in Analog CMOS Design, 1st ed. John Wiley, jun 2008.
- [14] M. Kayal and M. Blagojevic, "Design methodology based on the analog blocks retargeting from bulk to FD SOI using EKV model," in *International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)*, Gdynia, Poland, 2006, pp. 131–135.
- [15] H. Klauk, U. Zschieschang, and M. Halik, "Low-voltage organic thinfilm transistors with large transconductance," *Journal of Applied Physics*, vol. 102, no. 7, p. 074514, 2007.
- [16] H. Sirringhaus, P. J. Brown, R. H. Friend, M. M. Nielsen, K. Bechgaard, B. M. W. Langeveld-Voss, A. J. H. Spiering, R. A. J. Janssen, E. W. Meijer, P. Herwig, and D. M. de Leeuw, "Two-dimensional charge transport in self-organized, high-mobility conjugated polymers," *Nature*, vol. 401, no. 20, pp. 685–688, oct 1999.
- [17] J. Veres, S. D. Ogier, S. W. Leeming, D. C. Cupertino, and S. M. Khaffaf, "Low-k insulators as the choice of dielectrics in organic field-effect transistors," *Advanced Functional Materials*, vol. 13, no. 3, pp. 199–204, mar 2003.
- [18] H. Sirringhaus, N. Tessler, and R. H. Friend, "Integrated optoelectronic devices based on conjugated polymers," *Science*, vol. 280, p. 17411744, jun 1998.
- [19] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, and W. Radlik, "High-mobility polymer gate dielectric pentacene thin film transistors," *Journal of Applied Physics*, vol. 92, p. 5259, 2002.
- [20] I. C. Society, Ed., 1620 IEEE Standard Test Methods for the Characterization of Organic Transistors and Materials. Institute of Electrical and Electronics Engineers, apr 2004.
- [21] M. C. J. M. Vissenberg and M. Matters, "Theory of the field-effect mobility in amorphous organic transistors," *Physical Review B Condensed Matter*, vol. 57, no. 20, pp. 12964–12967, may 1998.
- [22] C. Detcheverry and M. Matters, "Device simulation of all-polymer thinfilm transistors," in *Proceeding of the 30th European Solid-State Device Research Conference (ESSDERC)*, 2000, pp. 328–330.