Reduced Stress and Fluctuation for the Integrated α-Si TFT Gate Driver on the LCD

Nan Xiong Huang, Miin Shyue Shiau, Hong-Chong Wu, Rui Chen Sun, and Don-Gey Liu

Abstract—**In this paper, an integrated TFT gate driver was designed on the glass substrate not only to decrease the fluctuation at the output, but also to reduce the stress effect on the pull-down branches. The fluctuation in the voltage at the output transistor was attributed to the coupled clocks through the parasitic capacitors in the TFTs. In this study, the voltage gating the pull-down braches was reduced for longer operational lifetime. This scheme was investigated by simulation by Smart-SPICE with an α-Si TFT model from Wintek Inc. at level 35.**

***Index Terms*—gate driver; fluctuation noise; stress effect; system on panel (SoP)**

I. Introduction

THE amorphous silicon (α-Si) thin-film transistor (TFT) has been widely used for mobile and portable display applications with their advantages in lower fabrication cost, simpler process steps, and higher yield. With the demands of higher resolution in displays, the interconnection becomes a key issue in the back-end package technology. Recently, more complex circuits can be implemented by the mature TFT technology [1-4]. Including the external controller circuits into the panel may be a good resort to solve the bottleneck in the interconnection.

Unfortunately, some transistors in the gate driver, such as the pull-down transistors suffer a very long on-time stress that will result in a big shift in the threshold voltage [1]. In order to reduce the stress on the pull-down transistors, the concept of the dual pull-down was proposed by doubling the number of the pull-down transistors [2-6]. However, doubling the pull-down branches cannot provide enough improvements in the reliability of the transistors. In the meanwhile, the floating state at the output transistor made the output terminal suffer serious interference from the clocks. Oh et al. and Deng et al. have tried to suppress this problem by the anti-fluctuating structure [7][8]. In their studies, prominent improvement had been achieved.

In this paper, further improvements in the fluctuation and reliability will be investigated. We would like to discuss the above issues by a more practical model from the industry. In this study, the control scheme for the dual pull-down structure was redesigned with a reduced gate voltage on the pull-down transistors to relieve the stress effect. In our simulation, Smart-SPICE with an α-Si TFT model used in the industry was utilized to estimate the possible degradation effects. In our study, the output fluctuation of our gate driver was prominently reduced as compared to that of the conventional one. And the stress effect in the dual pull-down branches was also significantly reduced.

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II. A Low Noise On-Panel TFT Gate Driver

A gate driving unit provides a high pulse voltage to each row line for selecting matrix line by turns. When gate driver turns on a row of TFT, source driver provides data voltage to charge pixels. After the pixels are charged, the gate driver provides a low voltage to keep up the charge in the pixels of that line and then turns on next row line sequentially. Fig. 1 shows the block diagrams of two-phase clocks (C1 and C2) controlled gate driver comprising a series of shift register cells for selecting each row line by scanning.

In order to achieve the enough driving capability, the size of push-up TFT must be larger than that of others. As a result, the coupling effect is happened easily on the larger parasitical capacitance of push-up transistor. The output voltage and the node P1 voltage of the circuit suffer the coupling noise from the capacitance C_{gs} and C_{gd} while the clock is switching alternatively. For this reason, the output voltage is fluctuating seriously while no output pulse is shifted.

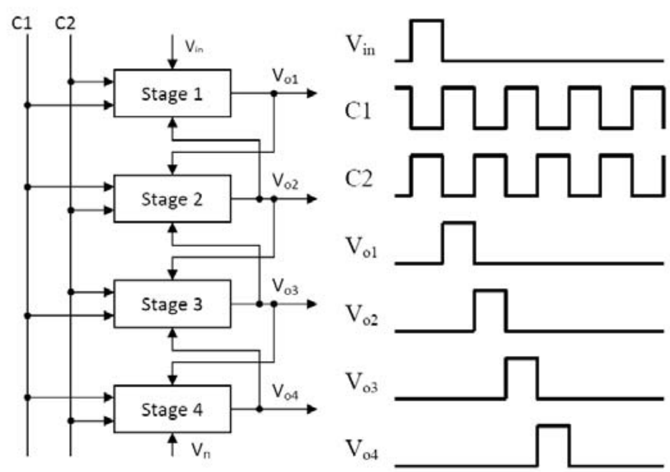

Fig. 1. The block diagram of Gate driver and its shift operation for gate scanning

Such fluctuation noise is resulted from the charge injection by means of the coupling of clock C1 to the node P1 via C_{gd}, and then to the output by C_{gs} while no output pulse is presented. Obviously, the output voltage is fluctuating seriously by this way, the node P1 is located at the key point on the fluctuating influence path.

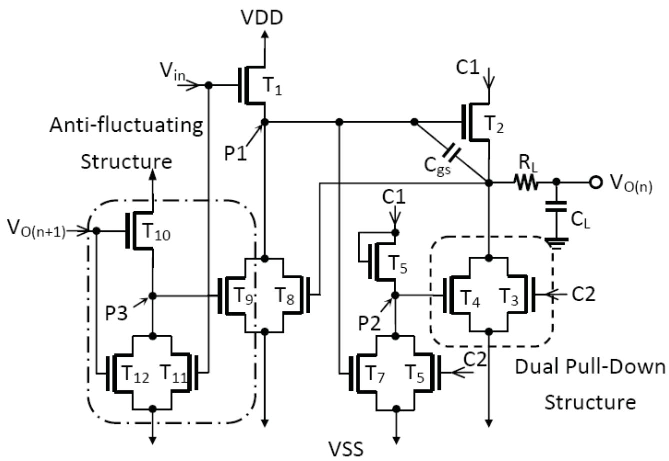

Fig. 2. A low noise on-panel TFT gate driver [8]

In the past, we proposed a modified on-panel TFT gate driver with anti-fluctuating structure in conjunction with the stress-reducing effect as shown in fig. 2 to reduce the noise coupling from C1 [6]. In order to decrease the number of TFTs, the anti-fluctuating structure is closely integrated into the on-panel TFT gate driver with dual pull-down structure as well. Keeping the output node $V_{O(n)}$ from the ac coupling of clock C1, the voltage of node-P1 must be kept constantly and low enough to avoid the stress effect. An anti-fluctuation structure (T9-T11) is added and a low stress voltage node P3 is designed for the pull-down transistor (T9) of node P1. The voltage of node P3 is reset to VSS each time when the input pulse Vin is coming in order to not affect the proper bootstrapping-up operation of node P1. But at some time late, while the output pulse Vout(n+1) of the next stage is fed back , the node P3 will be biased and held at an appropriate small voltage level which is still large enough to pull down the node P1 voltage through T9 by optimized-design of the size of T10 and T12. This situation is sustained until the coming of input pulse Vin of the next scan-turn. The connection of node P1 to a small constant voltage by a low resistance path as described above keeps it from the coupling of clock source C1 efficiently. An improved low-noise structure consists of a dual pull-down and an anti-fluctuation was designed successively. The low noise on-panel α-Si TFT-based gate driver of LCD display would be not only reduced the fluctuating noise of output but also modified the serious stress effect.

III. Improving Stress Effect of Pull-Down Transistor

Conventional gate driver circuit uses single pull-down structure. The pull down transistor undergoes almost full duty cycle to guarantee gate driver provides a low voltage output for a long time. In order to relax the serious stress effect of pull-down transistor, a dual pull-down structure are proposed [2][4][5]. When gate driver circuit requires a low voltage output, one of the two pull-down transistors is turned on alternatively after half time of clock signal.

Improving the stress effect of transistor further, two ways can be adopted, one is decreasing the turn-on time; and the other is diminishing the control voltage. Decreasing the turn-on time will become more complex circuit and more area overhead. From equation (1) we can understand to reduce the gate-voltage stress on our circuit, the lifetime of TFT-LCD driver will be increased. In this paper, a novel combined short turn-on time and well-designed low control voltage structure is proposed for reducing the stress effect of the dull pull-down transistors in advanced.

A time-dependent semiempirical description of ΔV_{th} is given by [9]

$$\Delta V_{th}(t) = A \cdot \exp\left(-\frac{E_A}{kT}\right) \cdot t^{\beta}\left(V_{GS} - \eta V_{DS} - V_{th,0}\right)^{n} \quad (1)$$

where k is the Boltzmann constant, T is the absolute temperature, t is the bias-stress time duration, E_A is the mean activation energy, A is the degradation rate, and $\eta = V_{GS}/(V_{GS}+V_{DS})$. β and n are process related constants. β is about 0.3 and n is about 1.0.

In the past, we use dual pull-down structure to extend the lifetime of pull-down transistors. From the equation (1) we can see that increasing the number of pull-down transistors is limited the increase lifetime of TFT gate driver. There, we will change the way for increasing the lifetime. Adding the number of pull-down transistors is reducing the turn on time. Now we will reduce the turn on voltage of the pull-down transistor. From equation (1), we can find that reducing the voltage is more favorable for the threshold voltage shift.

Fig. 3 shows the proposed gate driver circuit, which can be relax stress effect of dual pull-down transistor. The proposed gate driver include dual pull-down structure, anti-floating low noise structure, and two flash transistors. Transistor T_2 is the mainly responsible for pushing up the voltage, T_3 and T_4 are dual pull-down structure, T_9~T_{12} are anti-floating low noise structure, T_{13} is a reset transistor, T_8 and T_{14} are flash transistors, others transistors generate the lower voltage to control the dual pull-down structure. By cascading the TFT, the control voltages of node P2 and P4 for the dull pull-down transistors can be low down. In our design these dual pull-down transistors are only used as the auxiliary discharge switches, because the lower control voltage will result to a longer time for the output voltage discharging from VDD to VSS. Thus, it is only suitable for a low voltage swing usage. For this reason, a main flash pull-down transistor (T_{14}) is added, this transistor is designed with a little larger size and is turned on only a half period of clock C1, just likes a flash, in one whole scanning turn. So, the main switch (T_{14}) and both of the dual pull-down transistors (T_3-T_4) are benefitting of light stress effect. In addition to low stress effect design, this circuit maintained the long-term low noise design with an additional storage-capacitor C_{FS}.

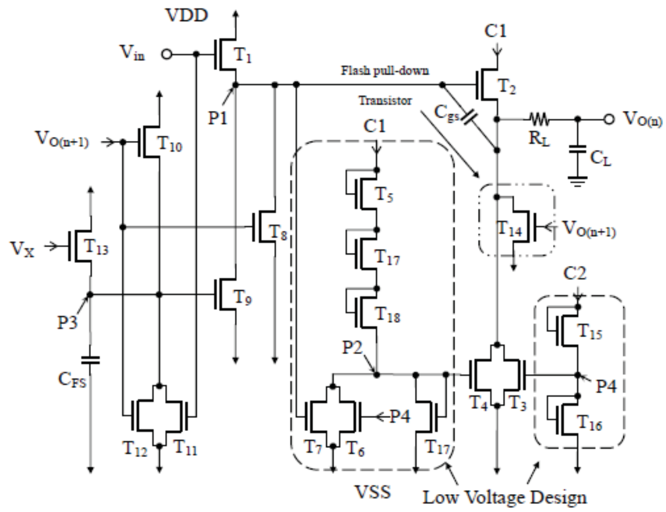

Fig. 3. Type 1 of a low voltage design on-panel TFT gate drive

Fig. 4 shows another low stress effect design. In the type 1 described above, we cascade the transistors to diminish the control voltage for dual pull-down transistors, but the threshold voltage of TFT is not necessarily the same in different factory and process. If the threshold voltage is lower, we must cascade much number of transistors. For this reason, following the idea of the node P4, we use the voltage divider by the aspect-ratios of the transistors to make up the suitable smaller voltage in P2 and P4. In the type 2 we can use less transistor and reach the same effect.

IV. Simulation Results and Discussion

In this paper, our simulation use Smart SPICE with the level=35 of α-Si TFT process Spice Model and the operation voltage is used from +15V to -10V. Fig. 5 shows the voltage of node P2 and P4 of the type 1 circuit. The P2 and P4 is the gate of dual pull-down transistors. If we reduce the gate to source voltage of pull-down transistors, we can relax the stress effect.

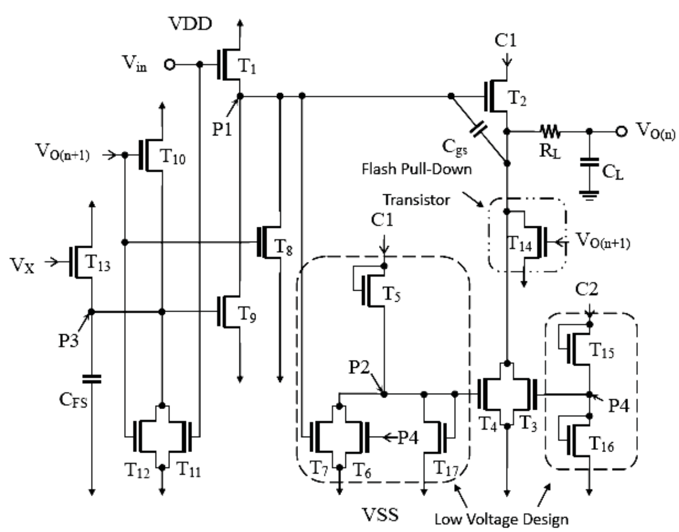

Fig. 4. Type 2 of a low voltage design on-panel TFT gate driver

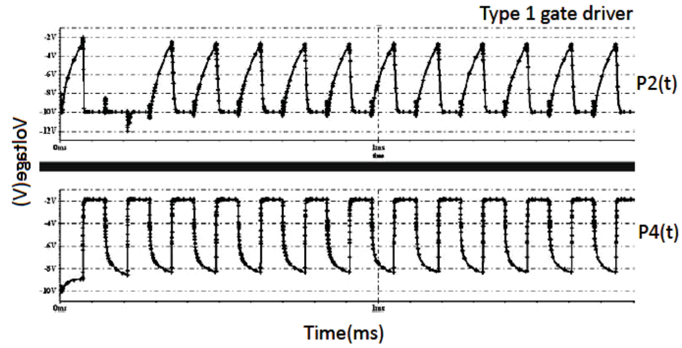

Fig. 5. The node P2 and P4 simulation results of the type 1 circuit

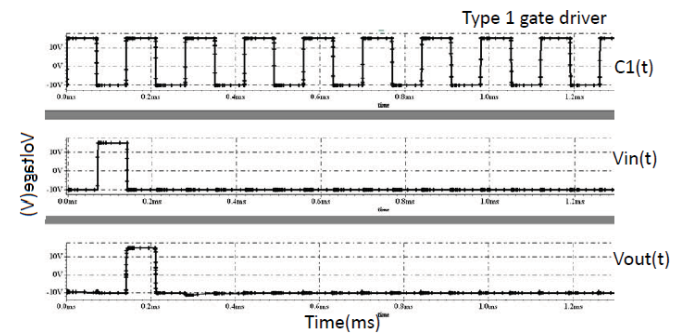

Fig. 6. The clock C1, input and the output simulation results of the type 1 circuit

In the past, the control signals of dual pull-down were clock 1 and clock 2, the voltage of these signals was about 25V and the turn-on ratio was 50%. If we use the low driver voltage design, the speed of threshold voltage shift will be slower than without using low driving voltage. The node P2 and P4 voltage will be set and held at a small voltage level (about -2 V) but large enough to turn on the T3 and T4 (V_{GST3} = V_{GST4}= 8V). From the fig. 5 we can find that the waveform of P2 presents the ramp wave. In the type 1, we would use the diode connected to reduce control voltage. But the diode connected had to endure smaller current, the voltage of P2 isn't arrived our setting level fast. Even so, the gate driver can still work correctly. Fig. 6 illustrates the waveforms of the voltages at the clock C1, the input and the output in the type 1 circuit. From this figure, the output voltage would reach 15V and the function of gate driver would be correct. In this study, we set the resolution of TFT-LCD is QVGA, so the gate driver would be 240 stages. From the fig. 6, we can see that the voltage of 240^{th} stage would reach 15V.

Fig. 8 shows the voltage of node P2 and P4 of the type 2 circuit. As the same, the control voltage is decreased from 15V to about -2V. We compare the difference fig. 5 and fig. 8 that the voltage of P2 in fig. 5 is like a ramp wave. But the voltage of P2 in fig. 8 is using the voltage divider, the waveform is like a complete clock. The type 2 gate driver could use less number of transistor and we do not consider that the differences of threshold voltage.

Fig. 9 illustrates the waveforms of the voltages at the clock C1, the input and the output in the type 2 circuit. From this figure, the output voltage would reach 15V and the function of gate driver would be correct. The fig. 7 and fig. 10 are the waveforms of the 231th to the 240th output voltage of type 1 and type 2 respectively. Both of them shows that the lower voltage of P2 and P4 would not influence the function of gate driver.

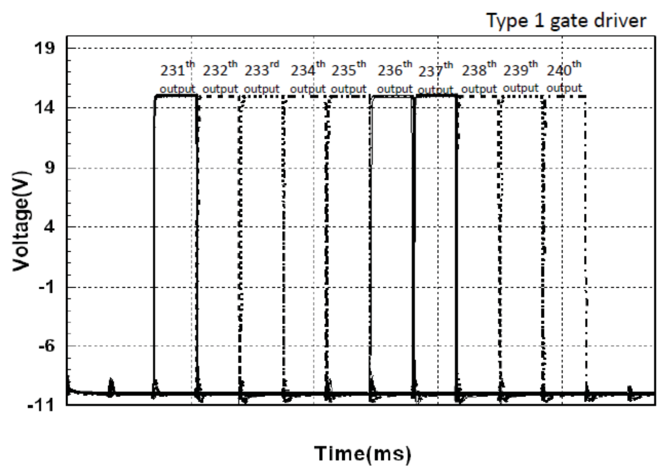

Fig. 7. The output waveform of 231th to 240th of type 1 circuit

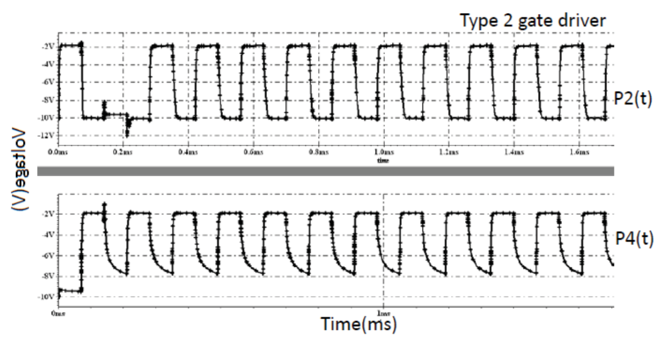

Fig. 8. The node P2 and P4 simulation results of the type 2 gate driver

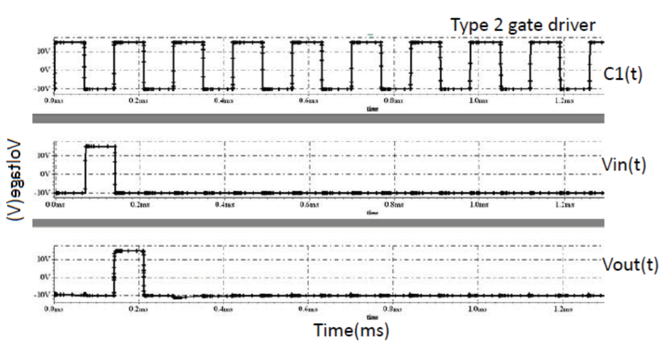

Fig. 9. The clock C1, input and the output simulation results of the type 2 circuit

The function will be correct, no matter what kinds of low driving voltage design. If we select the type 1, we have to cascade the transistor, and the numbers of cascade transistor would be decided by the threshold of TFT. If we select the type 2, we can just adjust the size of transistors of controlled signal such as T5, T15, T16 and T17.

V. Summary

In this paper, we propose a novel stress reducing solution for the on-panel α-Si TFT-based gate driver of LCD display. We modify the structure of the pull-down configuration and implement the low control signal of dual pull-down to relax the stress effect of the transistors and it keeps up a long-term low noise structure. According to the results of our simulation with the Smart-SPICE and using level-35 for α-Si TFT process model, it shows that our proposed structure works successively as expected to suppress the fluctuation noise phenomenon at the output node and to relax the high stress of the dual pull-down transistors. Thus it is a reasonable conclusion that the proposed integrated structures in this paper for an on-panel TFT gate diver can operate well with good reliability and low noise.

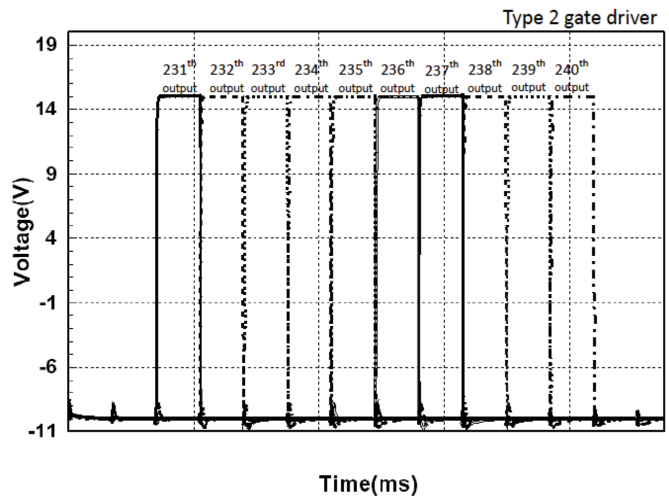

Fig. 10. The output waveform of 231th to 240th of type 2 circuit

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References

[1] H. C. Cheng, C. Y. Huang, J. W. Lin, Kung, J.J.-H., "The reliability of amorphous silicon thin film transistors for LCD under DC and AC stresses" Solid-State and Integrated Circuit Technology, 1998. Proceedings, 1998 5th International Conference on 21-23, pp. 834 – 837, Oct. 1998.

[2] S. Y. Yoon, Y. H. Jang, B. K., M. D. Chun, H. N. Cho, N. W. Cho, C. Y. Sohn, S. H. Jo, C. D. Kim and I. J. Chung, "Highly Stable Integrated Gate Driver Circuit using a-Si TFT with Dual Pull-down Structure" SID2005, Digest 172L, pp.348, 2005.

[3] H. R. Han, J. F. Tsai, W. T. Liao, and W. C. Wang, "Reliable Integrated a-Si Select Line Driver for 2.2-in. QVGA TFT-LCD" SID2005, Digest 15_3, pp.946, 2005.

[4] M. S. Shiau, M.Y. Tsao, H. C. Wu, C. H. Cheng and D. G. Liu, "Reducing the Stress on the Output Transistors of On-Panel TFT Gate Drivers", Chinese Journal of Electron Devices , vol.31 , no.1 , pp.124-129, Feb. 2008.

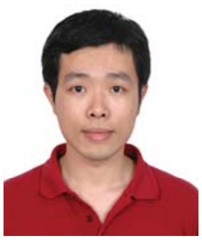
[5] M. Y. Tsao , M. S. Shiau , H. C. Wu, D. G. Liu, C. H. Cheng, "Reliable Gate Driver Circuits on Integrated TFT-LCD Panels," Conference on electronic communication and Applications, CECA2006, Kaohsiung, R.O.C., July 6, 2006.

[6] M. S. Shiau, M. Y. Tsao, H. C. Wu, D. G. Liu, C. H. Cheng, "Reduce High Voltage Stress Time on Gate Driver Circuits of Integrated TFT-LCD Panels," 2006 Taiwan Display Conference, Taipei, R.O.C., June 15-16, 2006.

[7] J. H. Oh, J. H. Hur, Y. D. Son, K. M. Kim, S. H. Kim, E. H. Kim, J. W. Choi, S. M. Hong, J. O Kim, B. S. Bae and J. J., “2.0 inch a-Si:H TFT-LCD with Low Noise Integrated Gate Driver” SID’05, Digest 15_2, 2005.

[8] E. L. Deng, M. S. Shiau, N. X. Huang, D. G. Liu. “A Novel Design of Low Noise On-panel TFT Gate Driver,” 8th International Meeting on Information Display, International Display Manufacturing Conference and Asia Display, KINTEX, Ilsan, Korea, October 13-17 2008.

[9] D. R. Allee, L. T. Clark, B. D. Vogt, R. Shringarpure, S. M. Venugopal, S. G. Uppili, K. Kaftanoglu, H. Shivalingaiah, Z. P. Li, J. J. Ravindra Fernando, E.J. Bawolek, S. M. O'Rourke, “Circuit-Level Impact of a-Si:H Thin-Film-Transistor Degradation Effects ” Electron Devices, IEEE Transactions Vol. 56, no. 6, pp. 1166-1176, Jnue 2009.



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