Multichannel Readout System for Registration of Electronic System Temperature Response with High Temporal Resolution

Marcin Janicki, Zbigniew Kulesza, Piotr Pietrzak, and Andrzej Napieralski, *Senior Member, IEEE*

***Abstract*—This paper presents the design and the practical realization of a measurement system dedicated to fast real-time multichannel registration of electronic system thermal response. The response is registered in parallel channels with a frequency up to 1 *MHz*. Such a high frequency is required for the thermal identification of electronic systems. The designed circuit is used here for the investigation of a thermal test ASIC. The presented solution can be extended for a different number of measurement channels and adapted for other types of sensors.**

***Index Terms*—Thermal characterization of electronic systems, real time parallel measurement data processing.**

I. Introduction

TEMPERATURE is the main factor, which influences the performance of modern electronic systems. Thus, thermal characterization and analysis of such systems is now one of the most important problems. For this purpose, high accuracy and high resolution temperature measurement data are required. These data can be further processed in real time to produce the hot spot temperature estimates or used off-line for the thermal characterization of electronic systems.

This paper presents such a practical solution which renders possible various thermal analyses of electronic systems. The next section of this paper presents briefly the analyzed thermal test ASIC. Then, all the design requirements and the practical realization of the measurement system are described in detail. Finally, test results of the manufactured system are presented. In particular, the problem of noise reduction is discussed.

II. Thermal Test ASIC

The detailed description of the thermal test ASIC, inspired by the earlier practical realization [1], was already presented in [2]-[3] hence here only a brief overview of the main circuit features will be provided. The internal structure of the entire ASIC is shown in Fig. 1.

This work was supported by the Polish Ministry of Science and Higher Education grant N515 008 31/0331.

The authors are with the Dept. of Microelectronics and Computer Science, Technical University of Lodz, Wólczańska 221/223, 90-924 Łódź, Poland (corresponding author phone: +48 42 6312654; fax: +48 42 6360327; e-mail: janicki@dmcs.pl).

The test ASIC was designed and manufactured in a 0.35 μm high voltage technology where logic circuits are powered with 3.3 V and high power circuits are supplied with 50 V. The analog part of the circuit consists of 2 overlaying matrices; the matrix of nine transistor heat sources, visible in Fig. 1 as large boxes, and the matrix of 25 p-n junction based temperature sensors covering the area of the heat source matrix. The logic part controls the heat sources and processes in real time sensor measurements.

The full flexibility of shaping the power dissipation pattern in the circuit is assured through the system of internal current mirrors and an external reference current source. The amount of the generated heat is controlled by digitally programmable current sources. Owing to this solution it is possible to switch individually each heat source on at one of 7 predefined power levels and at any desired time instant. The external reference current and the digital information, which controls the power dissipation in the heat sources, should be provided by the dedicated readout system described in the following sections of this paper.

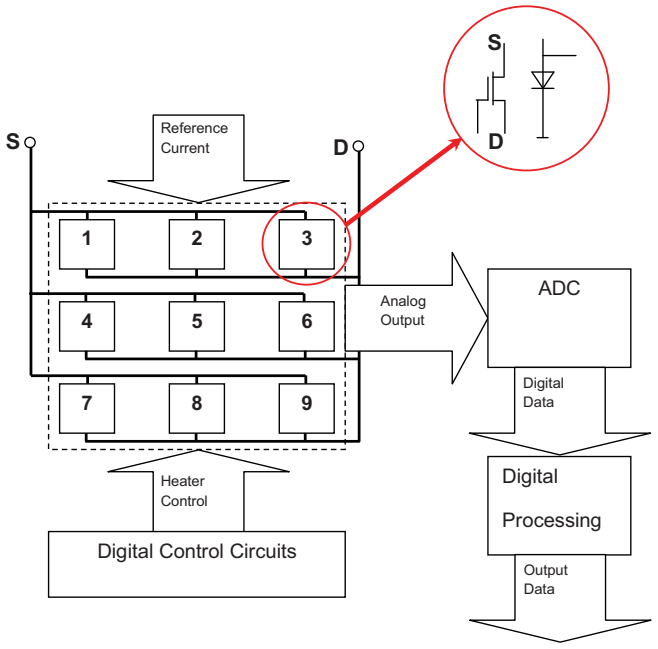

Fig. 1. Block schematics of the thermal test ASIC.

The temperature of the ASIC can be measured in real time directly with the sensors implemented inside the circuit. These sensors are not simple p-n junctions but they are composed of 3 in series connected base-emitter junction of the bipolar transistors available in the particular manufacturing technology used for the ASIC fabrication. The junction connected directly to the ground provides a voltage pedestal thus protecting from interferences propagating through this signal path whereas the useful signal is read across the two 'upper' junctions what improves the sensitivity, but requires the use of ADCs with differential inputs. The differential analog signals from each sensor are available directly at the appropriate pins of the ASIC, where they can be read and processed further by the external measurement system.

The main advantage of the differential measurement method is its higher immunity to interferences. This fact is particularly important when measurement signals are transmitted through long wires, as it is in the considered case where the system is connected to the board with the investigated circuit through a 30 cm long flexible bus.

The ASIC itself also contains 25 internal ADCs connected to the temperature sensors, but taking into account the limited chip size the internal structure of the converters had to be kept very simple. Consequently, they consist of digital counters and analog comparators which have to be supplied by an external reference saw-like waveform. The internal DAC output values can be stored in the built-in RAM memory and processed then by the on-chip digital filter to produce real time temperature estimates of hot spots located in the ASIC.

The internal logic circuits of the ASIC communicate with the readout system through a serial interface. The interface allows the control of the power dissipation in the heat sources and renders possible the configuration of the ASIC operation. Moreover, it communicates with the on-chip RAM writing the digital filter coefficient values or reading internally converted sensor voltages computed as well as the hot spot temperature estimates.

III. Design Requirements

The fundamental requirement for the measurement system was the ability to process in parallel at least 25 differential sensor inputs sampled at 1 MHz each. Moreover, the system should allow fully automatic programming of the test ASIC and the control of the temperature measurement processes, lasting even several hours. The system should also give the possibility not only to store the measured data in real time but also to process and filter them.

Another desired feature of the system is to communicate with the user allowing the visual inspection of the real time or recorded data. Finally, the system should provide the ASIC with all the necessary power supplies and reference currents. Unfortunately, currently there is no commercial measurement system available on the market able to fulfill even the first requirement alone.

Obviously, one can purchase systems with sampling rates of much more than 1 MHz, but this rate concerns only a single channel and when multiple channels are processed at the same time the sampling frequency has to be decreased because all channels share the ADCs.

The project assumed that up to 512 samples per channel can be stored in the system memory and that sensor measurements can be sampled at the maximal rate of 1 Msps with the digital resolution of at least 14 bits. Additionally, for the pre-filtering purposes, up to 4 consecutive samples from each measurement channel can be buffered and averaged.

The heat sources, as mentioned previously, can be switched on and off at any time instant and at any of 7 preset power levels. Owing to the use of current mirrors, the current in each source can be increased up to 21 mA with the step of 7 mA. This, combined with the possibility of setting the power supply voltage to any value in the range of 20÷50 V, assured the full flexibility in shaping the power dissipation pattern across the ASIC chip.

The precise triggering of the heat sources is possible owing to the use of 32/48 bit timer. The triggering time intervals can vary from 1 μs to 2 hours and they can be constant during the measurements or increased with the time base of 2 or 10. Thus the recording time of a temperature response can extend from 512 μs to almost 1 year! Additionally, before the sources are switched on, up to 16 measurements can be pre-triggered, also at any desired time interval .

Another challenge for the design of the system was to assure several different levels of power supply voltage. Namely, the system should provide 3 different voltages up to 3.3 V for the digital circuits, 3.3 V and 5.0 V for the analog circuits and 20÷50 V for the heat sources. Besides, the system should also produce the high precision saw-like reference voltage which, as described later on, is generated for the internal ASIC ADCs by a 16-bit digital current source.

IV. Practical Realization

The crucial decision to make in the system design was the choice of the main data processing and control unit. Finally, an FPGA-based solution was chosen because of its simplicity of testing combined with the large number of I/O ports offered and the freedom of configuring the internal FPGA resources. The main core of the practical realization, where all the control circuits and the memory of the system were located, was one the smallest FPGA circuits from the Xilinx® Spartan family - XC3S400. First, the functionality of the system was described in the VHDL. Then, the behavioural description was compiled and implemented in the hardware. The communication module of the system was designed as a state machine in the Xilinx® StateCAD environment. The usage of the resources available in the FPGA was: programmable blocks 2368/3584 (66 %), flip-flops 2727/7168 (38 %), LUTs 3360/7168 (46 %), 288 kb memory blocks 16/16 (100 %) and pins 94/97 (96 %).

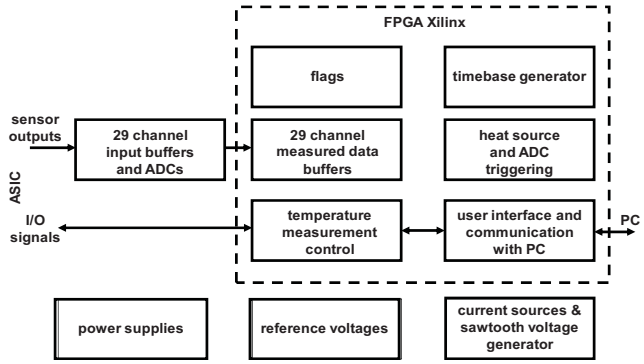

Fig. 2. Block schematics of the measurement system.

The block schematics and the photo of the finally realized system are presented in Figs. 2-3. The locations of all the most important functional block are indicated in the photo as well. The system communicates with the user through the standard EIA-RS232 serial interface at the rate of 115 kbps. The open source Tera Term terminal was used as a user interface. This software allows fully automatic control over the ASIC and the FPGA operation and reports transmission errors. The interface can be configured to read the measured values directly from the ASIC or from the RAM memory at desired time intervals. All the status registers of the FPGA can be also accessed from the terminal. Additional information provides a set of LEDs, which inform the user about the current operation of the ASIC or the FPGA, e.g. they indicate if the heat sources are switched on or if the ASIC is overheated.

The number of measurement channels implemented in the system is 29; 25 of which process the data from ASIC junction sensors, 1 is connected to the additional PTAT sensor located also in the ASIC, 2 read data from temperature sensors placed on the measurement board and finally 1 reads a high precision reference differential voltage. Here, unlike most other practical realizations, sampled values are not just buffered in ordinary FIFO registers, but they are stored in a memory, what renders possible their processing and filtering. The differential signals from all analog inputs are initially processed in high-precision amplifiers to suppress the common part of these signals and buffer them. Next, the signals are converted to the digital form in 14-bit ADCs. Because of the large number of measurement channels the ADCs have serial outputs.

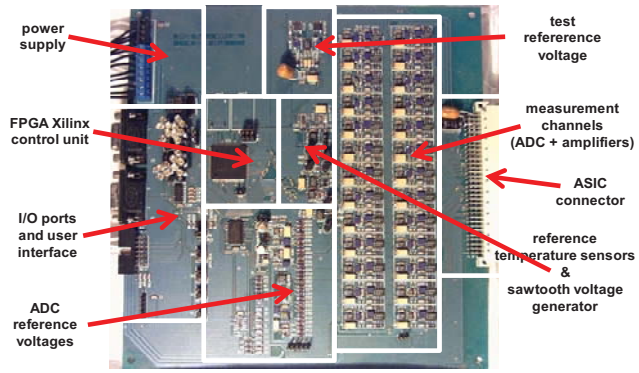

Fig. 3. Photograph of the system indicating the main functional blocks.

TABLE I
POWER SUPPLY BOARD SPECIFICATIONS

Suplied units	Voltage (V)	Power (mW)
Main digital power supply: ADCs, ASIC core, main board peripherals, EEPROM	3.3	900
Xilinx core	1.2	250
Xilinx clock and I/Os	2.5	50
Main analog power supply: input amplifiers, DACs, buffers	3.3	2125
Reference voltage units	5	255
ASIC high voltage: heaters	20-50	350-1500
	Total:	3930-5080

The constant current is delivered to the temperature sensors in the ASIC from the measurement system by a programmable current source. This source converts the digital voltage signal generated in the FPGA to an analog current signal in a simple converter consisting of a DAC, an operational amplifier and a bipolar transistor. The precise saw waveform for the ADCs contained in the ASIC is generated by a programmable current source controlled by a digital to analogue converter connected to the FPGA. Its output current is integrated in the capacitor, which is periodically discharged by an additional transistor key controlled by the FPGA. The voltage at the capacitor of the integrator forms the saw waveform. Then, this signal, buffered by another operational amplifier, is delivered to the ASIC.

The entire measurements system is powered by a relatively complex circuit, pictured in Fig. 4. This circuit provides all the power supplies essential for the proper operation of the FPGA board and the ASIC. The circuit can be supplied from a single 8÷20 V DC source. The estimated power values which should be provided by this circuit for the particular power supply voltages are given in Table 1. As can be seen, this circuit was expected to provide a relatively large variety of digital and analog voltages. For that reason, its design was divided into two separate parts; namely linear voltage regulators for the analog part and the Discontinuous Current Mode converters for the digital part. Taking into account that the total ASIC current should not exceed 0.2 A, it was estimated that the current demand of the entire system amounts to the maximal level of 1 A.

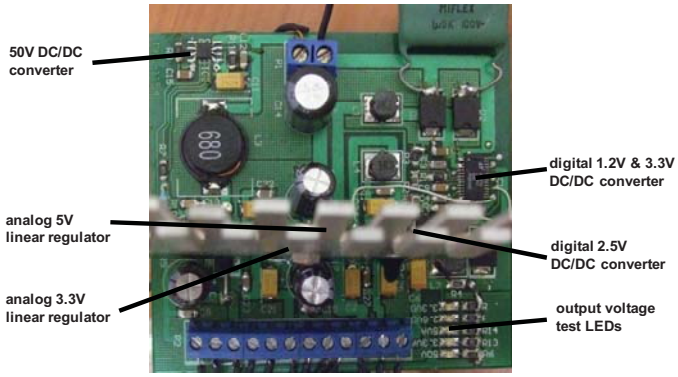

Fig. 4. Photograph of the power supply board showing its main blocks.

The main digital power supply is 3.3 V. This voltage is now very common among the integrated circuits and it was required also for powering the ASIC logic circuitry. Other components of the main board supplied by this voltage are: the ADCs, the EEPROM, as well as the I/O and interface circuits. In addition, the FPGA needs two more voltages: 1.2 V and 2.5 V. The first one is used for powering the FPGA core whereas the second one powers the Digital Clock Manager and I/O circuits. The quality of this voltage is therefore crucial from the system jitter and interference propagation point of view.

The current demand from the 2.5 V source is not significant, just a few tens of mA, therefore the simple LT1118-2.5 linear regulator was used as the power supply for this voltage. This circuit was powered through the 5 V analog voltage supplied by an additional inductor to suppress interferences between the digital and the analog parts.

For the 1.2 V and 3.3 V digital power supply, the miniature LT1941 DCM DC/DC converter was used. This circuit has the switching frequency of 1.1 MHz and it contains internal power switches, hence and it allows the use of compact inductors and there is no need to use external transistors. The circuit contains three integrated converters; two step-down ones with current efficiency of 3 A and 2 A, which were used to generate 1.2 V and 3.3 V voltages respectively, and a boost converter, which was left unused. The two step-down converters were run with opposite phase, thus reducing the ripple current.

The analog circuits, including buffers, reference voltage and current sources as well as the saw tooth wave generator have to be supplied by 5 V or 3.3 V. For this purpose, the standard integrated voltage regulators were chosen. The 7803 regulator in the TO-3 package was used to provide 5 V and the surface mounted LT-1963-3.3 for the 3.3 V voltage. These regulators were electrically connected in such a way that the output of the first one was joined to the input of the other one. Then, only the 5 V regulator requires a heat sink because it dissipates the most power. It should be also mentioned that owing to the use of linear regulators it was possible to assure lower noise level than in the case when DC-DC converters are used.

The power supply circuit provides also the 50 V voltage, which is delivered to the transistor heat sources manufactured in the ASIC. Because the input voltage of the power supply unit can be as low as 8 V, it was necessary to use a boost DC-DC converter. Taking into account that this converter is not expected to provide currents higher than 50 mA, the LM3478 low-side N-channel controller was chosen for this purpose. It is a universal IC which can work as boost, flyback or SEPIC DC/DC converter. Its output current can be limited by a proper choice of a resistor, which is an important feature from the ASIC safety point of view. The switching frequency of this converter was set to its maximal value of 1MHz, what allowed significant miniaturization of the filtering circuits. Currently, this converter is being modified by adding some microswitches so as to render possible setting the output voltage to different values in the range of 20÷50 V.

V. Testing and Measurements

The full functionality of the entire system was proved during numerous tests. The most important observation is that it was possible to attain the assumed in the project, extremely high, temperature measurement speed of 1 Msps in all the parallel channels sampled at the same time. The effective 14-bit ADC resolution at this sampling frequency was around 12 bit. This corresponds to the temperature measurement accuracy of less than 1 K. All the reference currents and voltages showed high stability and the internal data transfer rate attained within the measurement system was 60 MB/s.

The only drawback was a relatively high level of noise and interference in measurement channels. More detailed analyses, shown in Fig. 5, led to the conclusions that the signal quality is not uniform in particular channels and that in some of them the standard deviation of the noise largely exceeds the sensibly acceptable value of a few mV.

Theoretically, certain reduction of noise and interferences could be achieved by lowering the sampling frequency of the ADCs. This system was designed for the sampling frequency of 1 MHz. Such a high sampling frequency is rarely required in practice, because for the characterization of most thermal phenomena the sampling frequencies lower by two orders of magnitude are more than sufficient.

Indeed the tests carried out at the 100 times lower sampling frequency of 10 kHz and with averaging of a few consecutive samples confirmed these theoretical considerations. The new results, shown in Fig. 6, demonstrate that at the lower sampling frequency, the standard deviation of noise in all the channels dropped down significantly. The magnified view of this chart produced in Fig. 7 only for the channels in which the standard deviation does not exceed 10 mV shows that that the average standard deviation in these channels slightly exceeds 4 mV, which corresponds to around 1.5 K.

The observed phenomenon appeared with the introduction of serial ADCs and it is particularly visible when systems are operating at their nominal conditions. The cause for this is that the ADCs with serial interfaces are clocked at a relatively high frequency (in this case over 18 times higher than the sampling frequency). As a result, the signals at the series outputs of the ADCs usually contain, in spite of the use of antialiasing filters, sequences corresponding to a wide frequency range, even the low ones, comparable with the sampling frequency.

Further elimination of interferences was achieved through filtering of power supply voltages using high quality capacitors and inductors, particularly in the analog part of the system. Another effective way of improving the signal quality turned out to be the blocking of the clock signals at the time instants when measurements are taken. This could be realized directly in hardware by just changing the VHDL code and recompiling it for the FPGA. Unfortunately, this solution is not possible when some advanced features of the ASIC have to be used, such as its internal ADCs or the on-chip digital filters.

The effects of the improvements for a selected measurement channel are shown in Figs. 8-10. As can be seen, low sampling frequency combined with the efficient decoupling of individual channels can bring important noise reduction. Obviously, this solution is practical when the thermal frequency components higher than a few kilohertz are not important.

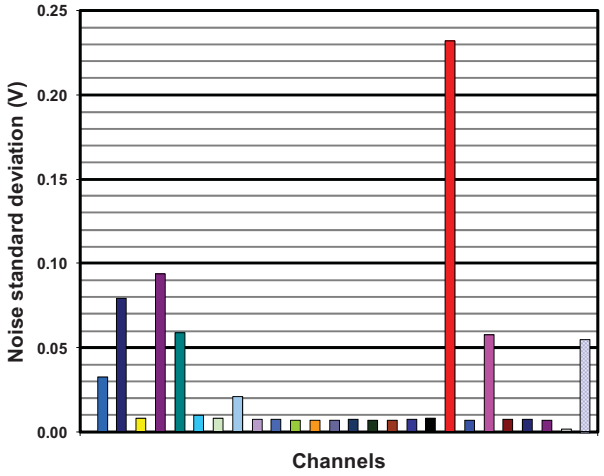

Fig. 5. Noise standard deviation in particular channels sampled at 1MHz.

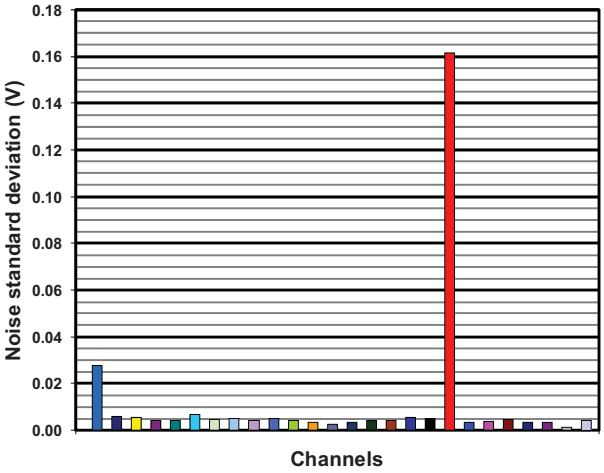

Fig. 6. Noise standard deviation in particular channels sampled at 10kHz.

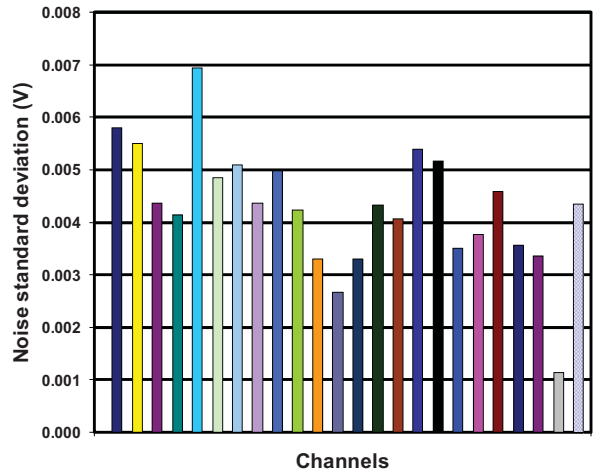

Fig. 7. Magnified view of noise standard deviation with sampling at 10kHz.

Although the current system does not have any errors in the electrical connections, however it was created with a limited budget only as a prototype. Thus, in future a better solution would be to redesign entirely the layout of the main board and integrate it with the power supply circuit. The final version of the system should have a modified topology of components and routing of signal paths, with a few blocking capacitors added. The most vulnerable areas could be screened by copper plates. The required modifications should also encompass the changes in the ASIC itself, among which the most important one is the separation of the analog and digital power supplies.

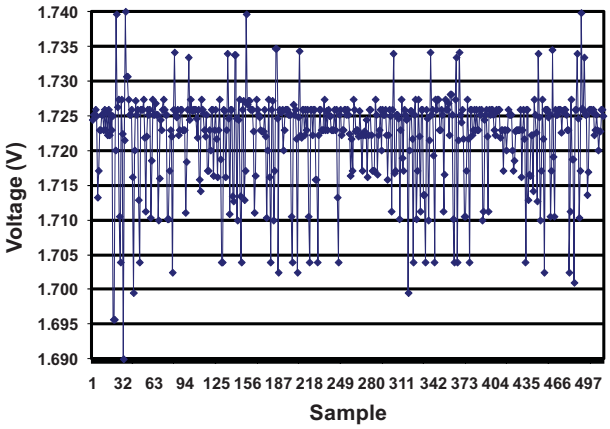

Fig. 8. Original results for a selected channel sampled at 1MHz.

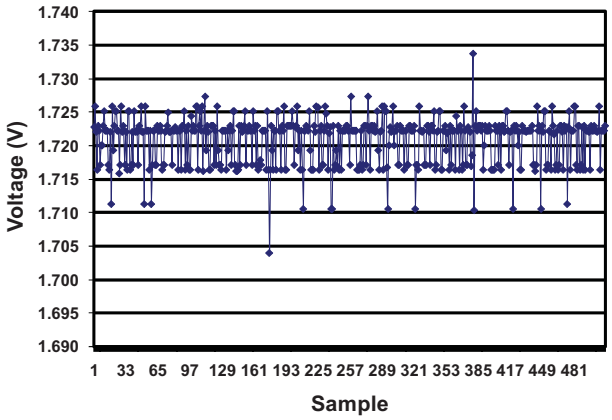

Fig. 9. Original results for a selected channel sampled at 10kHz.

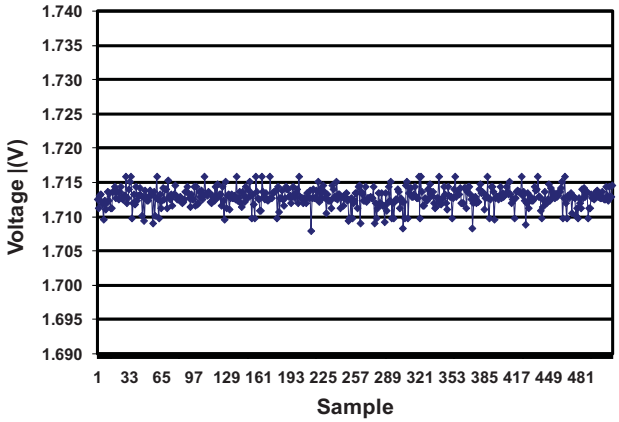

Fig. 10. Improved results for a selected channel sampled at 10kHz.

The usefulness of the measurement system has been proven in numerous experiments, described in [4], when temperature of the ASIC was measured for different configurations of heat sources and in different cooling conditions. An example of the results obtained at the 32 times reduced initial sampling rate and the sampling interval doubled with each 32 measurements are shown in Fig. 11. Figure 12 presents results for the same case but with the minimal initial sampling intervals of 1 μs doubled with every 20 measurements. The power dissipated in the heat source in both cases was round 1 W. The total time required for the acquisition of 512 samples was 20 minutes in the first case and 10 minutes in the second one. As can be seen the results are very similar, what proves the repeatability of the results and the stability of the designed system.

VI. Conclusions

This paper presented a successful realization of the system dedicated to multichannel temperature measurements carried out in multiple channels with very high sampling rates and relatively low noise level. Even better results than the hereby presented ones can be obtained averaging successive samples. Once programmed, the measurement is fully controlled by the system and does not require any human supervision.

Future modifications of the system should be aimed at the lowering of the noise and interference levels. This goal could be attained by modifying the layout of this prototype system, thus achieving higher compactness of the design and better temperature measurement accuracy.

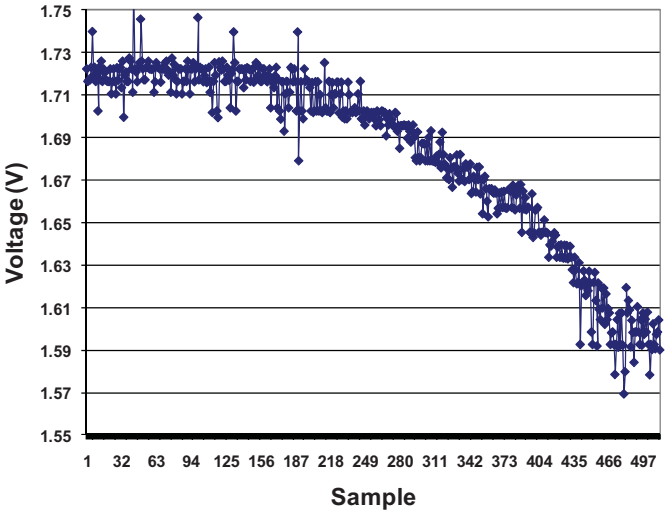

Fig. 11. Measurement results at the 32 times reduced initial sampling rate and the sampling interval doubled with each 32 measurements.

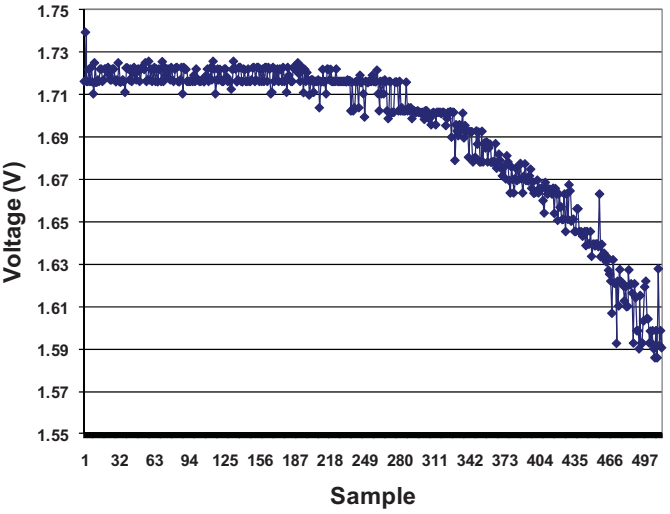

Fig. 12. Measurement result obtained with the minimal initial sampling intervals of 1 μs doubled with every 20 measurements.

References

[1] Z. Benedek, B. Courtois, G. Farkas, E. Kollár, A. Poppe, M. Rencz, V. Székely, and K. Torki, "A scalable multi-functional thermal test chip family: Design and evaluation," *ASME J. Electron. Packag.*, vol. 123, pp 323-330, Dec. 2001.

[2] M. Szermer, Z. Kulesza, M. Janicki, and A. Napieralski, "Test ASIC for real time estimation of chip temperature," in *Proc. 10th NSTI Nanotechnology Conf. Nanotech*, Boston, USA, 2008, vol. 3, pp. 529-532.

[3] M. Szermer, Z. Kulesza, M. Janicki, and A. Napieralski, "Design of the test ASIC for on-line temperature monitoring and thermal structure analysis," in *Proc. 15th Conf. Mixed Design of Integrated Circuits and Systems MIXDES*, Poznan, Poland, 2008, pp. 317-320.

[4] M. Janicki, M. Szermer, S. Klab, Z. Kulesza, A. Napieralski, "Practical study of temperature distribution in a thermal test integrated circuit," in *Proc. 15th Workshop on Thermal Investigations of ICs and Systems THERMINIC*, Leuven, Belgium, 2009, pp. 136-139.