Digitally Programmable Delay-Locked-Loop with Variable Charge Pump Current

Bruno Lopes, Nuno Paulino *Member, IEEE,* João Goes *Senior Member, IEEE*, and Adolfo Steiger-Garção

***Abstract*—This paper presents a digitally programmable delay line intended for use as timing generator in a RADAR ranging system. The architecture of the programmable delay uses a $\Sigma\Delta$ modulator to generate a reference clock with a delay unaffected by component matching. This reference clock has a large jitter noise component that is filtered by delay lock loop (DLL). The programmable delay can produce a delay ranging from 20 ns to 100 ns, because of the large delay variation, it is necessary to use a variable charge pump current in the DDL, in order to guaranty stability for all the desired delay values. The electrical design of the circuit, in a 0.13-μm 1.2-V CMOS technology, will be presented, as well as electrical simulations results of the complete system.**

***Index Terms*—Delay-Locked-Loop, digitally programmable delay, Ultra Wide Band.**

I. Introduction

USING ultra wide band signals (UWB) it is possible to build a low-cost short-range RADAR ranging systems such as the one described in [1], [2]. These systems work by measuring the travel time of a signal from the transmitter to the target and back to the receiver. In order to measure this time it is necessary to compare the received signal with a delayed version of the transmitted signal until an echo is found. The target range can be determined from this delay. In order to simplify the measurement of the delay it is convenient to use a digitally programmable delay circuit to generate the delayed version of the clock. The circuit presented in this paper is capable of generating a digitally programmable delay whose resolution is not affected by element mismatch. This paper describes the design and simulation of this circuit, using a 0.13-μm 1.2-V CMOS technology. The architecture of the digitally programmable delay is described in [3]. All of the circuits in the digitally programmable delay are fully differential, including the charge pump that has several advantages over the conventional single-ended charge pump proposed in [5], [6], [7].

II. Architecture of the Programmable DLL

In order to achieve a digitally programmable delay with a large linearity (independent from matching errors), the architecture of the system is constituted by a digital $\Sigma\Delta$ modulator that controls a 1-bit digital to time converter, whose output will be filtered by a Delay Lock Loop (DLL), thus producing the delayed clock signal [3]. This architecture is depicted in Fig. 1.

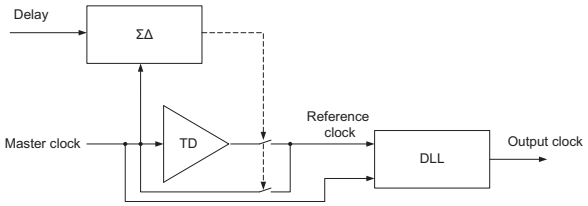

Fig. 1. Architecture of the digitally programmable delay (DLL).

The digital $\Sigma\Delta$ modulator, with a fixed input digital code, controls the switching sequence between the master clock and a delayed version of this clock, in order to produce the reference clock with an average delay value determined by the digital input code. This reference clock will have a large jitter noise caused by the high frequency quantization noise, produced by the $\Sigma\Delta$ modulator. This noise is filtered by the DLL low pass transfer function. To avoid spikes in this reference clock, the maximum delay T_D should be inferior to half period of the master clock.

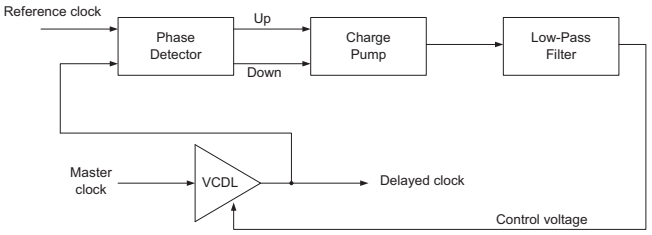

Fig. 2. Block diagram of the Delay Locked Loop.

The DLL, as shown in Fig. 2, works in a similar way to a Phase Locked Loop (PLL), except that the input frequency value is always the same as the output frequency value. The loop compares the phase (delay) of the reference clock with the phase of the delayed clock using a phase detector (PD). The output of the charge pump (CP), goes through a low-pass filter to attenuate the excess jitter noise from the clock signals, and the resulting voltage is used to control the delay value in the voltage controlled delay line (VCDL) until the rising (or the falling) edges of both clocks coincide. The minimum order of the DLL is related to the order of the $\Sigma\Delta$, the DLL will be a second-order system because of closed loop stability problems. The order of the $\Sigma\Delta$ modulator can be determined calculating

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the *rms* value of the jitter noise at the output of the DLL for different orders of the $\Sigma\Delta$ modulators [2]. According to the graph in Fig. 3, a second order modulator produces the best resolution for a given closed loop pole frequency (f_p) value in the case of a second order DLL.

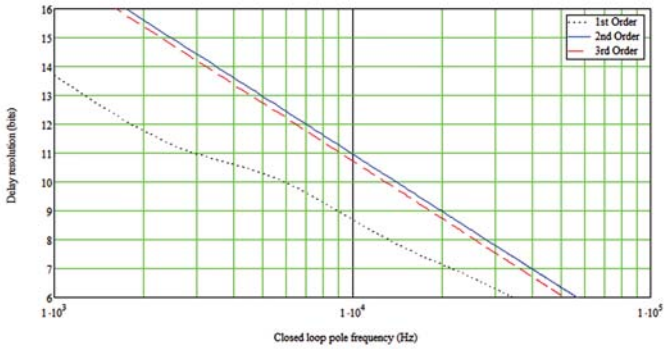

Fig. 3. System resolution (in bits) of the DLL for different closed loop frequencies and a $\Sigma\Delta$ modulator of 1, 2 and 3.

The closed loop pole quality factor Q_p does not affect this graph as long its value is between 0.5 and 1.5 as the Fig. 4 shows:

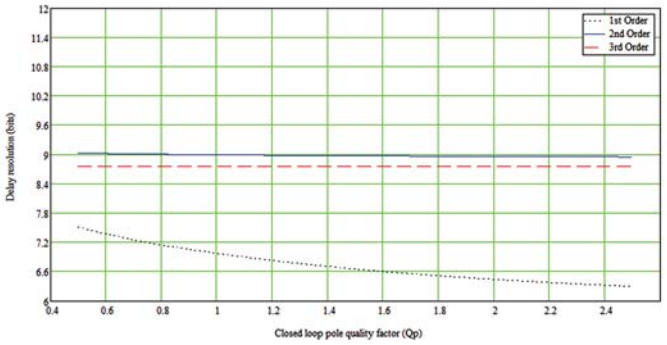

Fig. 4. System resolution (in bits) of the DLL for different closed loop quality factor and a $\Sigma\Delta$ modulator of 1, 2 and 3.

Since the phase detector measures the phase delay only in the rising edge of the clock signals, the loop behaves as a discrete time system. The DLL closed loop transfer function is obtained by a discrete time analysis resulting in [3]:

$$H_{DLL}(z) = \frac{G \cdot I_p \cdot K_{PD} \cdot K_{VCDL} \cdot T_{CLK} \cdot z}{G \cdot I_p \cdot K_{PD} \cdot K_{VCDL} \cdot T_{CLK} + C_1 \cdot \tau_{RC} \cdot (z-1) \cdot (z-1+\frac{T_{CLK}}{\tau_{RC}})} \quad (1)$$

where G is a gain in the filter, I_p is the charge pump current, K_{PD} is the phase detector gain, K_{VCDL} is the gain of the VCDL, C_1 is the output capacitance of the charge pump, τ_{RC} is the time constant of a first order filter introduced in the loop in order to obtain a second order transfer function. Evaluating this equation using $z = e^{j \cdot 2 \cdot \pi \cdot f} \approx 1 + j \cdot 2 \cdot \pi \cdot f$ it is possible to obtain an approximated continuous time transfer function. From this transfer function it is possible to obtain expressions for the closed loop pole frequency and quality factor:

$$f_p = \frac{1}{2\pi} \sqrt{K_{PD} \cdot K_{VCDL} \cdot \frac{I_P}{C_1} \cdot \frac{1}{\tau_{RC}} \cdot F_{clk}} \quad (2)$$

$$Q_p = \frac{\sqrt{K_{PD} \cdot K_{VCDL} \cdot \frac{I_P}{C_1} \cdot \frac{1}{\tau_{RC}} \cdot F_{clk}}}{\frac{1}{\tau_{RC}} + K_{PD} \cdot K_{VCDL} \cdot \frac{I_P}{C_1} \cdot \frac{1}{\tau_{RC}}} \quad (3)$$

These expressions are used to design the DLL loop in order to have a closed loop frequency of 16 kHz and a pole quality factor of 0.7. The main circuit parameters used in this design are $\frac{I_P}{C_1}$ and τ_{RC}. The other parameters in the circuit do not allow for much design freedom since they are dependent on the technology and on power dissipation constraints. The final design of the DLL loop must take into account the electrical design of the DLL sub-blocks, this will be discussed next.

III. Constituting Circuits of the DLL

A. Phase Detector (PD)

The PD is a digital state machine with 3 states, whose states correspond to the reference clock being "ahead", being the same or being "behind" of the delayed clock. Initially the PD is in inactive state, both UP and DOWN signal are OFF, if the rising edges of the reference clock occur before the delayed clock, then the PD will activate the UP signal until a rising edge of the delayed clock occurs, resulting in the activation of the DOWN signal that will activate the RESET signals, returning to the inactive state. The time interval when the UP signals is ON measures the phase difference between the two input clock signals. The third state is the other way around, when the rising edge of the delayed clock occurs first and the DOWN signal is activated. The maximum amount of delay between the two clock signals with the same period (T_{clk}) is $\pm T_{clk}$. When the PD "awakes" it can be in any of the 3 states, which can be a problem. Because the loop gain of the DLL can be positive or negative for the same delay between the two input clock signals. The solution for this problem is to reset the PD to the inactive state at start-up, this is implemented with an OR gate and a new reset signal (generated at start-up), as shown in Fig. 5.

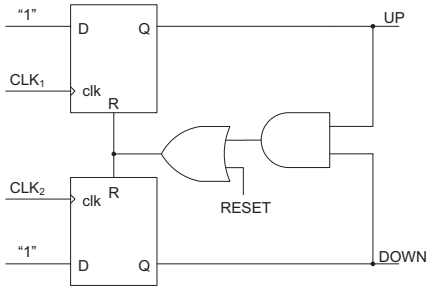

Fig. 5. Schematic of the phase detector.

The clock signals in the circuit are differential signals, because this type of signals generates much less noise than CMOS signals. The flip-flop circuits are implemented using NOR gates [4] and the gates are implemented using differential logic based on differential pairs, such as the circuit shown in Fig. 6.

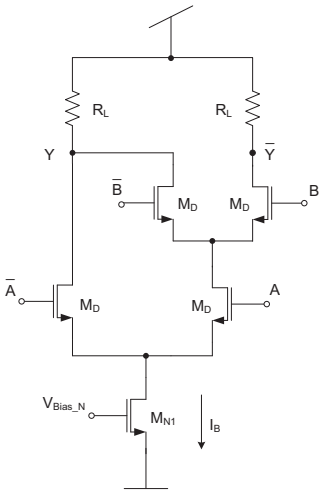

Fig. 6. Schematic of a differential AND gate.

This circuit can realize the four basic logic operations AND, NAND, OR and NOR, depending on how the input and output signals are connected.

B. Charge Pump

The CP uses a folded cascode topology to increase the output resistance and maintain a large output voltage swing for a low power supply. Since the CP is completely differential the output resistance should be maximized through a careful design of the current source circuits inside the CP. This circuit is depicted in Fig. 7.

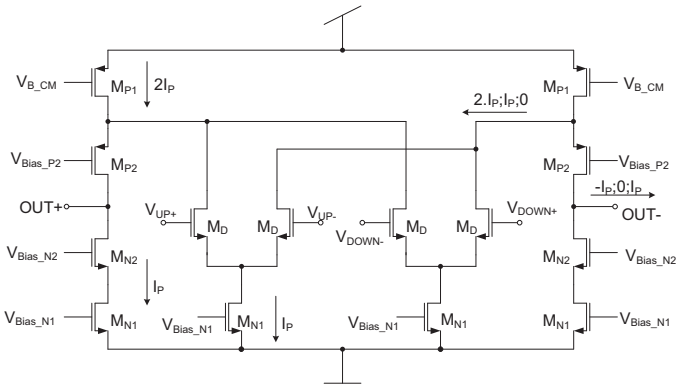

Fig. 7. Folded cascode charge pump circuit schematic.

The transistors M_{P1} produce a current equal to $2.I_P$ and the transistors M_{N1} produce a current equal to I_P. This current will charge a capacitor (C_1) increasing or decreasing its voltage depending on which current source is on. The output current is determined by the two differential pairs that act as switches steering the current produced by the M_{P1} transistors from the output branch. Transistors M_{P2} and M_{N2} act as cascode devices and increase the output resistance of the current source transistors. Since the CP is designed to have a high output resistance, any mismatch between the current values of the NMOS and PMOS current sources would result in the common mode output voltage saturating in either V_{DD} or GND [2]. To avoid this situation it is necessary to adjust the current level of the PMOS to match the NMOS current sources. The common mode comparator circuit is depicted in Fig. 8:

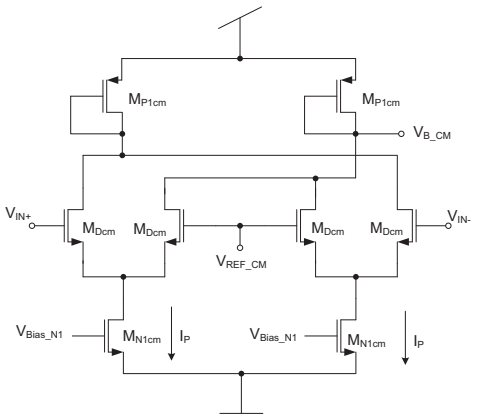

Fig. 8. Common mode comparator circuit.

The differential pairs have a output current proportional to the difference between the positive or negative output voltage and the desired common mode voltage level. The currents produced by this differential pairs are summed in the transistor M_{P1}, generating a bias voltage for the transistor M_{P1} inside the CP circuit.

C. Low-Pass Filter

The output of the CP is connected to a capacitor, resulting in the creation of a pole close to DC. The voltage across this capacitor increases or decreases according to the phase detector activity. An extra pole is needed in the loop in order to obtain a second order system, this pole is created in the differential to single ended converter circuit, shown in Fig. 9, by adding an extra capacitor to the output resistor. This circuit converts the differential output voltage of the charge pump into a single ended voltage used to control the VCDL, it is implemented as a differential pair with a current mirror load, that drives the output resistor, thus producing a single-ended voltage.

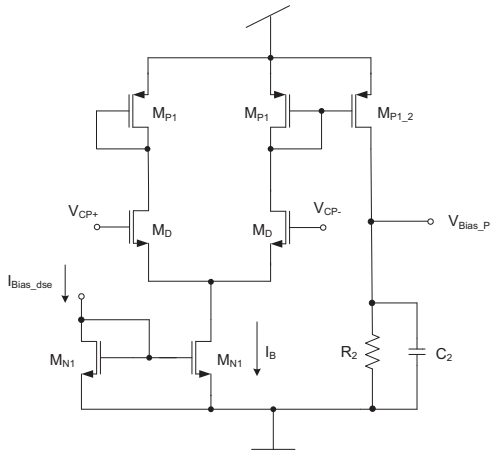

Fig. 9. Differential to single ended conversion circuit and second pole.

D. Voltage Controlled Delay Line

The VCDL is implemented as a cascade of differential buffers with symmetrical loads [8], such as the one depicted in Fig. 10. If both PMOS transistors, in the symmetrical load, have the same size, this type of load exhibits an almost constant conductance, when the output voltage changes. The delay of each differential stage varies with the value of the load conductance, which can be adjusted using the control voltage V_{Bias_P}. The delay of the differential buffer is proportional to the RC time constant of the output node and it can calculated using:

$$T_D(V_{Bias\_P}) \approx \frac{0.7 \times C}{\beta \cdot [(V_{DD} - V_{Bias\_P} + 2 \cdot V_T)]} \quad (4)$$

where β is the transconductance parameter of the load transistors, C is the capacitance value in the output nodes of the circuit and V_{Bias_P} is the control voltage.

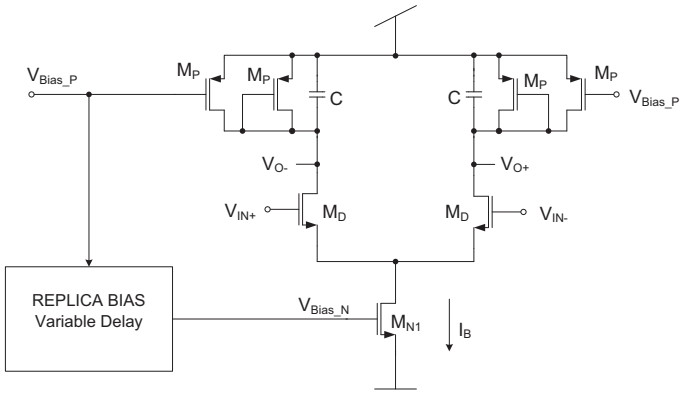

Fig. 10. Variable delay buffer schematic.

When the control voltage V_{Bias_P} changes (in order to adjust the delay of the buffer) the amplitude of the signal in the buffer also changes (because the load conductance changes). Since the power supply voltage is only 1.2 V, the signal amplitude can not change significantly otherwise the differential pair would not work properly. The VCDL is supposed to produce a delay that can change approximately 100 ns, this would result in large voltage swing variation, therefore it is necessary to adjust the bias current of the inverter in order to obtain a constant voltage swing. A negative feedback circuit determines the bias current in a replica circuit of the delay element as shown next in Fig. 11. The replica bias circuit is designed to have a bandwidth larger than the clock frequency of the circuit (in order not to introduce any extra poles into the circuit) and in order to be stable for all the possible values of the control voltage V_{Bias_P}.

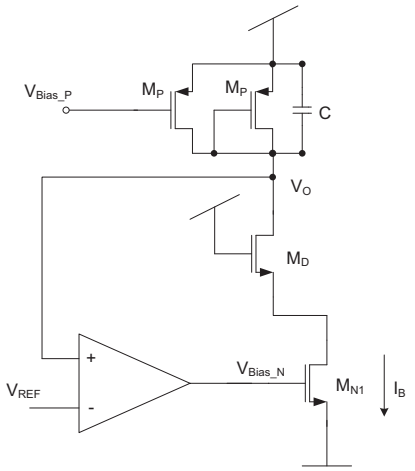

Fig. 11. Replica Bias circuit.

The maximum delay a single buffer can add is limited to $T_{Dmax} = T_{CLK}/4$ because a larger delay would result in an output signal with an amplitude smaller than the input signal amplitude. Therefore if a larger delay value is required it is necessary to use more than one delay element in cascade. The specifications of the programmable delay require that the VCDL must be able to produce a variable delay with a maximum value of 100 ns, which in this case, means that the VCDL circuit is composed of three variable delay differential buffers, followed by three fast differential buffers. The fast buffer are used to reduce the rise and fall time of the output signals. These circuits use resistive loads in order to obtain a small rise and fall times and are controlled by a separate replica bias circuit (in order to eliminate the influence of process and temperature variations in the signal amplitude). The complete VCDL circuit is show in Fig. 12.

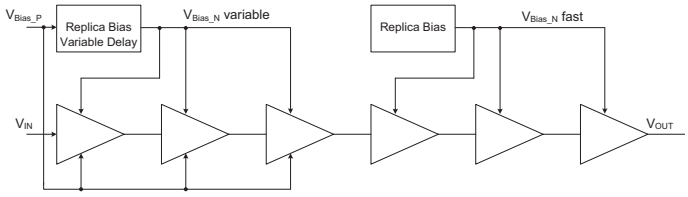

Fig. 12. Block diagram of the Voltage Controlled Delay Line.

IV. Design and Simulation Results

The programmable delay circuit proposed here was designed in a 130 nm HS (high-speed) 1.2 V CMOS technology. Only standard NMOS and PMOS devices were used without special options (e.g. low-V_T or high-V_T devices). The mobility and threshold parameters (Level 2), K_N, K_P, V_{TN} and V_{TP} parameters of the devices are, respectively, 525 μAV^{-2}, 145 μAV^{-2}, 0.38 V and -0.33 V.

The digital $\Sigma\Delta$ modulator controls the switching sequence that produces the reference clock, as shown in Fig. 1. The reference clock is created by selecting between the input clock and a delayed version of the input clock. The switches used to do this selection can add jitter and extra delay to the clock signals,

due to the ON resistance and the parasitic capacitance. These switches are implemented as CMOS switches, the transistors in these switches must be carefully designed in order to reduce the unwanted effects in the clock signals.

A. Charge Pump common mode loop stability

The correct operation of the CP depends on the common mode comparator, these circuits must be designed together in order to guaranty that the common mode feedback loop is stable. This loop must have a bandwidth larger than the DLL reference frequency (2.5 MHz), to assure that any common mode voltage wander is corrected within a clock cycle. A value of 5 MHz is set as the design goal. The common mode loop gain must also be larger than 40 dB to guaranty that the error between the desired common mode voltage and the actual value is inferior to 1% and the phase margin of the loop must be larger than 60° to guaranty stability.

TABLE I
CHARGE PUMP COMMON MODE LOOP SIMULATION RESULTS.

	Design Goals	Typical Simulation Results
Gain (dB)	40	74.87
GBW (MHz)	5	6.89
Phase (°)	60	82.90
Rout (MΩ)	∞	63.18

Since the circuit behavior can vary with temperature, supply voltage values, a corners analysis was made to assure that the loop is unconditionally stable. The results of these simulations results are shown in Table II.

TABLE II
CORNERS SIMULATION RESULTS OF THE COMMON MODE CP LOOP.

Supply Voltage (V)	Section	Temp. (°C)	Gain (dB)	GWB (MHz)	PM (°)	Rout (MΩ)
Vdd = 1.2	Slow	0	74.70	7.70	81.9	64.77
		80	69.60	6.92	82.0	39.88
	Fast	0	76.28	6.58	83.74	68.12
		80	72.50	5.79	83.88	49.77
Vdd = 1.08	Slow	0	74.70	7.70	81.93	54.42
		80	69.60	6.92	82.06	32.06
	Fast	0	76.28	6.58	83.74	61.60
		80	72.50	5.79	83.88	44.07
Vdd = 1.3	Slow	0	74.70	7.70	81.93	67.26
		80	69.60	6.92	82.06	39.25
	Fast	0	76.28	6.58	83.74	70.47
		80	72.50	5.79	83.88	49.79

B. Replica Bias loop stability

The feedback loop of the replica bias circuit adjusts the voltage swing of the delay elements inside the VCDL. Since these process digital signals a tolerance of around 1% in the signal amplitude is aceptable. This means that the open loop gain of the feedback loop should be larger than 40 dB. The bandwidth of the loop should also be larger than the clock frequency of the DLL and the loop should have a phase margin larger than 60°. The design goals and the typical simulation results are shown in Table III. The result of the corner simulations of the circuit are shown in Table IV, these corners include the variation of the V_{Bias_P} for maximum and mininum delay.

TABLE III
REPLICA BIAS FOR THE VARIABLE DELAY BUFFER SIMULATION RESULTS.

	Design Goals	Simulation Results (V_{Bias_P} = 0 V)	Simulation Results (V_{Bias_P} = 650 mV)
Gain(dB)	32	48.28	43.76
GBW(MHz)	8	17.2	18.1
Phase(°)	60	69.7	81.6

TABLE IV
CORNERS ANALYSIS SIMULATION RESULTS CONFIRMING THE STABILITY OF THE LOOP.

Supply Voltage (V)	Section	Temp. (°C)	Gain (dB)	GWB (MHz)	PM (°)
Vdd = 1.2	Slow	0	50.76	22.6	66.6
		80	48.19	18	76.5
V_{Bias_P} = 0	Fast	0	47.95	16.0	65.2
		80	45.69	12.7	75.6
Vdd = 1.2	Slow	0	49.18	21.6	69
		80	45.54	17.3	79.3
V_{Bias_P} = 0	Fast	0	47.01	15.7	67.7
		80	42.06	12.3	79.4
Vdd = 1.2	Slow	0	50.42	22.3	65.9
		80	48.72	17.8	75.1
V_{Bias_P} = 0	Fast	0	48.14	16.1	63.8
		80	46.94	12.9	73.6
Vdd = 1.2	Slow	0	50.17	23.6	81.3
		80	38.18	16.8	93.2
V_{Bias_P} = 0.65	Fast	0	46.38	17.5	69.3
		80	36.74	13.1	84.4
Vdd = 1.08	Slow	0	62.33	25.7	61.5
		80	44.62	17.3	77.1
V_{Bias_P} = 0.53	Fast	0	51.19	19.1	70.4
		80	35.28	12.5	93.1
Vdd = 1.3	Slow	0	46.13	21.6	83.8
		80	38.18	16.9	93.3
V_{Bias_P} = 0.75	Fast	0	46.19	16.9	67.7
		80	39.25	13.6	79.7

C. VCDL simulation results

The delay of the the VCDL is essentially determined by the delay of the differential buffer with variable delay (Fig. 10). The signal amplitude in this circuit must be large enough in order to guaranty that the differential pair saturates and that it is larger than the V_T of the load transistors for all the corners. The bias current of this circuit is given by:

$$I_B \approx \frac{\beta}{2} \cdot (V_{DD} - V_{Bias\_P} - V_T)^2 + \frac{\beta}{2} \cdot (V_{Swing} - V_T)^2 \quad (5)$$

where β is the transconductance parameter of the load transistors, V_{Bias_P} is the VCDL control voltage and V_{Swing} is the clock signal amplitude. This equation shows that the current in the buffer changes quadratically with both the control voltage and the clock signal amplitude. The circuit is designed in order to have a voltage swing of 400 mV and a bias current (for the minimum delay case) of 100 μA. The load PMOS transistors

are designed to have minimum channel length and a small W/L ratio. The value of the output capacitor is determined by electrical simulations, in order to obtain the desired delay variation in the complete VCDL. The delay of the VCDL as a function of the control voltage, was simulated for different process corners, the result is shown in Fig. 13.

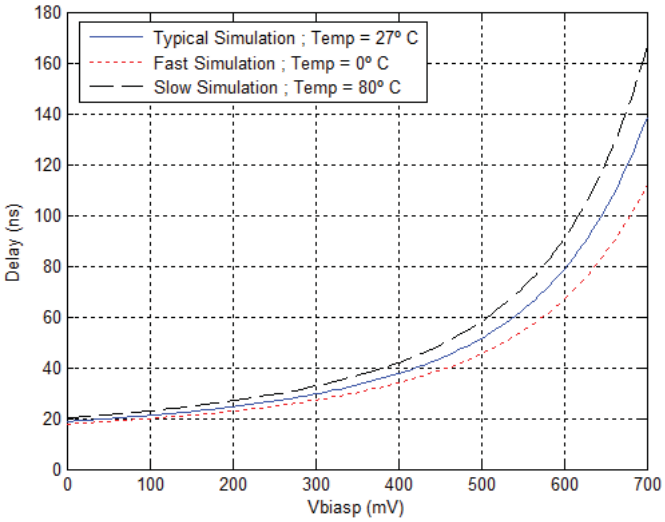

Fig. 13. Simulated delay of the VCDL as a function of the control voltage.

The gain factor of the VCDL (K_{VCDL}) is given by the derivative of the delay to the control voltage (V_{Bias_P}), this is inversely proportional to the square of the control voltage:

$$K_{VCDL} = \left(\frac{dT_D}{dV_{Bias\_P}}\right) \propto \frac{1}{V_{Bias\_P}^2} \tag{6}$$

This gain can be obtained by numerically calculating the derivative of the delay of VCDL (obtained by electrical simulation Fig. 13). The value of (K_{VCDL}) as a function of the control voltage is shown next in Fig. 14.

As expected, this graph shows that (K_{VCDL}) increases quadratically with the control voltage. This means that the loop gain of the DLL will increase quadratically with the desired delay. This is a problem, because it means that the DLL closed loop frequency and quality factor will change significantly with the delay (as shown by expressions 2 and 3). The end result is that for larger delays, the K_{VCDL} value is very large which means that the closed loop pole frequency increases (the quality factor also) and therefore the jitter noise at the output of the DLL will also increase. In order to maintain a small jitter noise at the output of the DLL it would be necessary to use a charge pump current (I_P) value that can produce a compromise between the jitter power for large delays and the DLL response time for small delays. This results in a value of I_P equal to 5 μA. In order to obtain a better performance it would be necessary to adjust the charge pump current, in order to compensate for the the variation of the K_{VCDL}. Noting that the bias current of the variable delay (given by expression 5) increases with the square of the control voltage

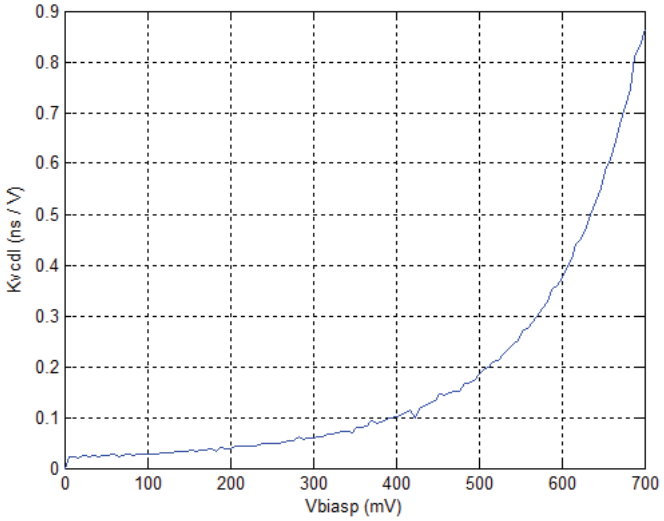

Fig. 14. Simulated gain curve of the VCDL.

value (V_{Bias_P}) and that the K_{VCDL} value decreases with the square of the control voltage (expression 6), it is clear that the product of these two variables can be independent of the control voltage (in a first order approach). Therefore the charge pump current value is determined according to the value of the bias current of the variable delay buffer. This is achieved by adjusting the bias current of the charge-pump circuit using the following circuit:

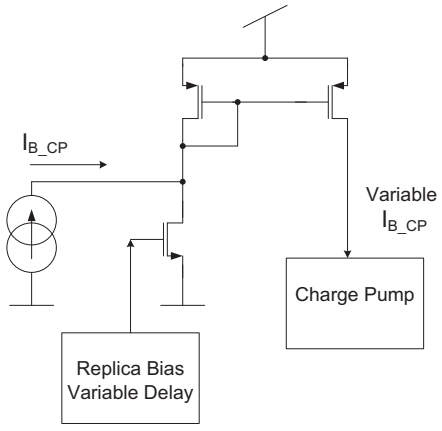

Fig. 15. Architecture of variable charge pump current.

The previous circuit has a fixed bias current (I_{B_CP} value of 1.67 μA, the variable bias current changes between 6.5 μA (for a delay of 20 ns) and 0.185 μA (for a delay of 100 ns).

D. DLL simulation results

In order to simulate the complete programmable delay, the $\Sigma\Delta$ modulator was simulated at high level for different input values and the resulting output bit stream was imported into the electrical simulator to control a voltage source. This voltage source was used to implement the clock signal that controls the switching between the input clock and the delayed clock signal, the master clock frequency is 2.5 MHz,

corresponding to a clock period of 400 ns. These signals were used to run electrical simulations of the circuit with different delays, the resulting step responses of the programmable delay are shown next in Fig. 16. These simulation results shown that DLL loop is stable for the different delays.

The delay produced by the circuit as a function of the programming delay is shown in Fig. 17, for the case of the variable charge pump current ($I_{B_CP} = 1.67\ \mu$A) and for the case of the fixed charge pump current ($I_{B_CP} = 5\ \mu$A). From this graph it is clear that using a variable current results in an improved programming linearity.

The relative error of the programmed delay are shown in Fig. 18.

The simulated output jitter noise of the circuit for different delays is shown in Fig. 19. These simulation results show that the programmable delay, using the variable charge pump current, has an output jitter noise smaller than 106 ps rms, even for the case of the maximum delay.

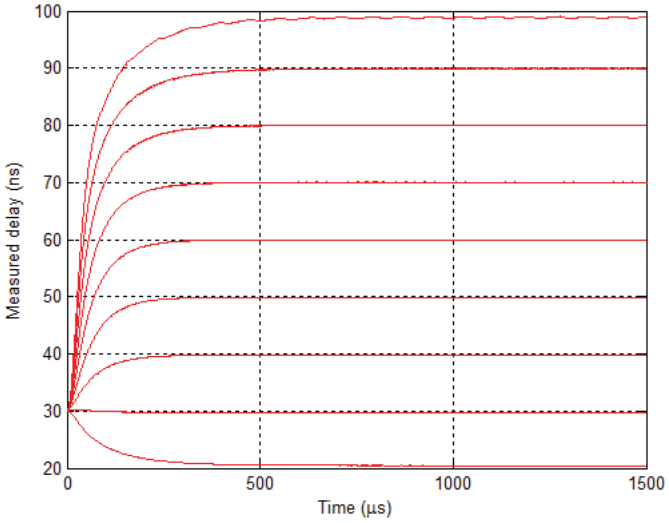

Fig. 16. Step response of the programmable DLL. Programmable delay from 20 ns to 99 ns.

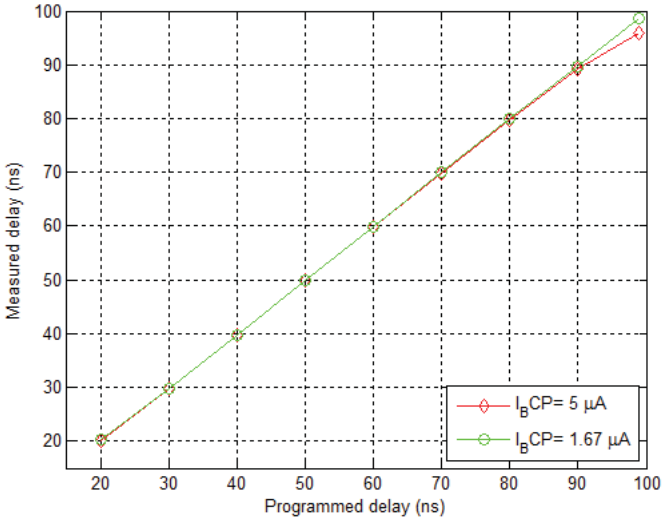

Fig. 17. Simulated output delay as a function of the desired delay.

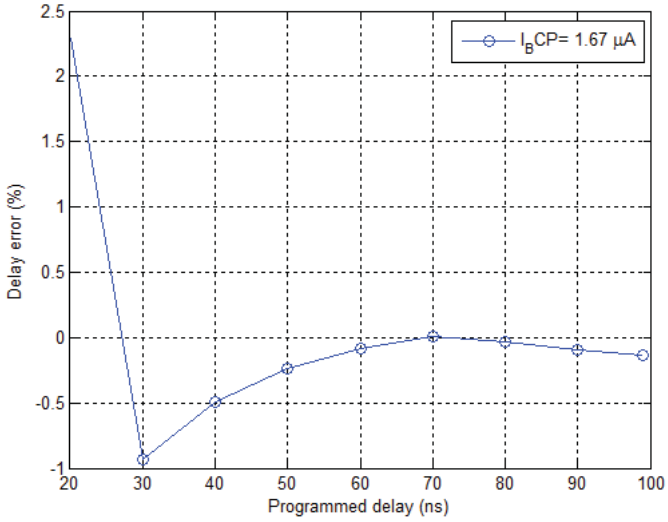

Fig. 18. Delay error simulation results of the programmable DLL.

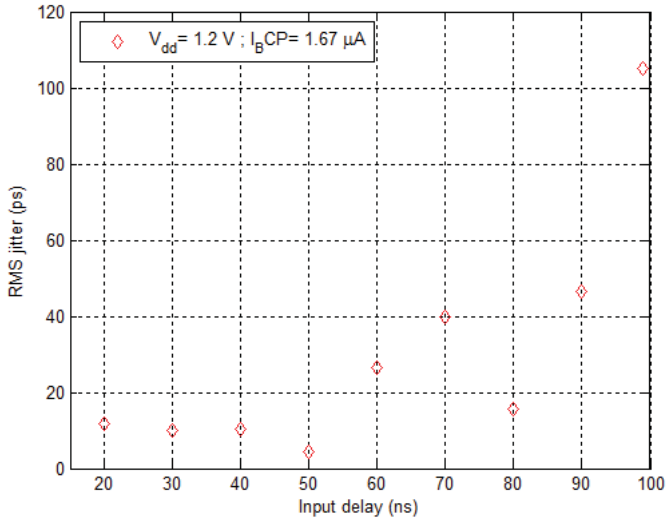

Fig. 19. Jitter noise simulation results of the programmable DLL.

TABLE V
PROGRAMMABLE DELAY SUMMARY.

Delay (ns)	Power dissipation (mW)	Jitter noise rms (ps)	Delay error (%)
20	2.05	11.6	2.29
99	2.31	105.1	-0.14

V. CONCLUSION

This paper presents a digitally programmable delay line intended for use as timing generator in a RADAR ranging system. The architecture presented uses a $\Sigma\Delta$ modulator to generate a delay unaffected by matching and a delay lock loop (DLL) to filter the excess jitter noise from the output clock. Inside the DLL we presented design and simulations results showing that by making the current of the charge pump variable results in a improved jitter noise and delay error.

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