# A sub-μW Conductance Converter for Bioimplantable Devices

Nuno Miranda and Raul Morais

***Abstract*—This article describes a new electrical conductance converter method suitable for very low power applications, where energy constraints prevail over speed and measurement accuracy. This method gathers voltage integration and shopper stabilization techniques to process noisy low level signals and overcome severe limitations of weak inversion channel CMOS circuitry. Main features, tradeoffs and upgrades are exploited. Besides that, the paper presents the circuit schematics for a standard 0.35μm CMOS implementation. Post-layout simulations show a total current consumption lower than 750nA, including current source excitation inherent to the conductance measurement. Such low power consumption allows measuring several physical parameters using self-powered wireless sensors networks.**

***Index Terms*—Conductance measurement, biologic tissue micro-power, ASIC**

## I. Introduction

ELECTRICAL conductance reflects many physical or physiologic proprieties directly or through a resistive transducer. In some applications, reduced power consumption and miniaturization prevail over accuracy and precision. Agricultural field is demanding new automation technologies including self-powered wireless sensor networks to meet economic criteria. Soil water content for automatic irrigation management is one example of such use. Herd management is another application where an implantable bio-impedance sensor can predict the correct time to successfully perform artificial insemination [1][2]. In the aforementioned examples there is no need for high accuracy or speed performance, but very low power consumption is crucial to comply with energy harvesting techniques and reduce the final application cost.

From the wide range of conductance or impedance measurement applications, bio-technology field have motivated the development of electric bio-impedance (EBI) variations measurement approaches aiming low-power and single chip implementation [3]. Most of them apply a bipolar pulsed current source into a biological tissue, the unit under test (UUT), and uses synchronous demodulation to extract real and imaginary components of impedance [4]. Both components are separately filtered or sampled and converted to digital domain. These approaches may be effective, but they do not minimize power consumption. This paper describes a new electrical conductance converter technique, suitable to be implemented using CMOS technology. In addition, it allows the implementation of a simplified measurement device with minimized power consumption for the targeted application.

Measurement approach and blocks diagram are presented in section II. Features tradeoffs, design choices and possible improvements from the simplest approach are also exploited. In the section III, a 0.35μm standard CMOS technology ASIC schematic implementation is described. Section IV presents circuit layout and post-layout simulations. The last section presents the final remarks.

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## II. Conductance Measurement Method

Here we present a very low power electrical conductance measurement method where energy constraint prevails over speed, linearity resolution and accuracy. Similarly that lock-in amplifiers can detect or measure a very low amplitude AC signal, the goal is to measure a very low voltage on the UUT caused by a very low current excitation. When speed is not mandatory, voltage integration can be used to increase a SNR measurement, allowing the developed voltage across UUT to be even dipped on noise. All circuitry can work at low speed, allowing the use of low levels of MOSFET channel inversion.

### *A. Measurement Technique*

A three level bipolar step current source is applied to the UUT and the resulting voltage is amplified before a chopper rectifies the signal. At this stage, signal average is inversely to UUT conductance. This signal is integrated and compared to a threshold reference. When the integration voltage reaches this reference, comparator output ends the process and switches off all analog circuitry. The result is an output count proportional to UUT conductance. System block diagram is presented in Fig. 1. A temporal diagram of relevant signals on the conversion process is presented on Fig. 2.

### *B. Features*

An important requirement to the most impedance sensor is to apply no DC current or voltage to UUT. This characteristic balance electrons or ions flow preventing damage on contact electrodes or on UUT itself.

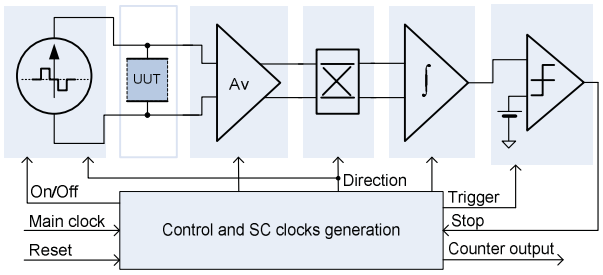


Fig. 1. Electric conductance converter block diagram.

System simplicity can benefit from this requirement. First, pulsed current source is switched using a H bridge. As a consequence, medium current is null and independent on any offset from the current source. Second, the chopper placed at the amplifier output to rectify the amplified voltage allows the cancellation of any amplifier offset and also reduces pink noise from signal. White noise is reduced during integration time depending on the size of integrator capacitors. At cost of time conversion, the presented measurement technique waives the usual conversion sample-and-hold and constitutes an alternative technique for low voltage and low power applications.

### C. Design Choices

A characteristic inherent to this topology is design flexibility to meet application requirements of resolution, power consumption and speed. Resolution depends on current excitation amplitude applied on UUT, total gain, from amplifier and integrator factor, threshold voltage and on UUT measurement range. If the UUT reactance component matters, power depends on circuitry speed to process signal at a desired frequency on UUT. Otherwise, power and speed are a compromise for a specified measurement range and resolution. With very little adjustment on biasing and input clock frequency division it may be possible to perform impedance measurements at wide range of frequency with the same circuit. In the last case, and to reduce energy consumption, it is possible to increase frequency for specified power consumption or reduce power for a specified frequency at the cost of linearity loss due to settling time error on amplifier on the integrator.

Minimum voltage is dictated by amplifier cells and process technology. Weak or moderate channel inversion provides small transistor source-drain saturation voltage allowing operational amplifiers to work down to 1.2V on actual CMOS technologies.

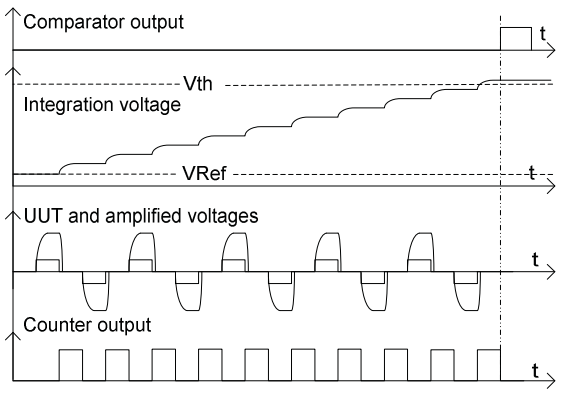


Fig. 2. Temporal representation of determinant signals involved on conductance conversion process.

### D. Circuitry Design Issues

The measurement approach allows a simple yet effective circuitry implementation. Measurement performance is strongly dependent on how care is taken about noise, limited gain on amplifier cells and charge injection errors on switched capacitor circuits. These aspects become more significant in low voltage and low current circuitry design.

The integration voltage threshold and voltage noise dictate maximum effective resolution. In this simple approach and low voltage design, high resolution can only be achieved by reduction the noise of integrator output and reference signals and improving comparator accuracy.

If UUT is biased by a very low amplitude current, amplifier and chopper process very low amplitude signals and so they should be fully differential to cancel charge injection errors.

### E. Approach Improvements

The proposed measurement approach allows very simple circuitry implementation that may provide modest performance and very low power consumption. Despite of design choices for some specific application, these are always shrieked for low voltage and low currents.

#### 1) Resolution improvement and comparator input offset error cancelation

To significantly improve resolution without need to reduce noise levels and increase biasing currents, digital control block can be modified to allow the integrator to repeat integration *N* times. To this effect, another comparator is added and chopper control signals needs to be changed after integration voltage reaches threshold voltage toggling integration way. Fig. 3 presents temporal diagram of the main signals involved. This technique improves resolution *N* times, however the comparators input offset errors remains unchanged.

Another possible implementation is adding another chopper at the comparator input instead of another comparator. This solution waives to increase power consumption from the second comparator and allows the reduction the input offset error from the comparator. If *N* is even the input offset error is cancelled.

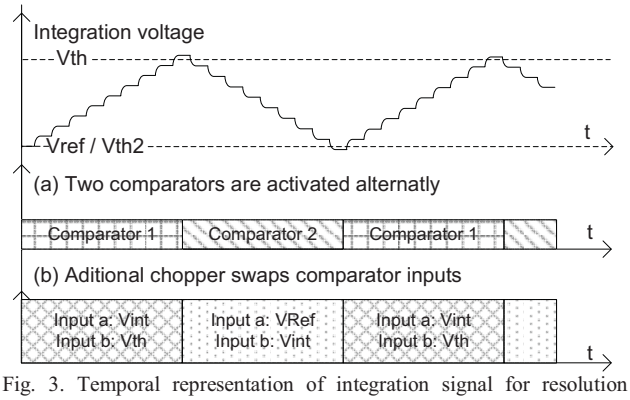


Fig. 3. Temporal representation of integration signal for resolution improvement. Solution requires a second comparator (a), or a second chopper to swap the comparator inputs (b).

If the threshold voltage is close to reference voltage, conversion method resembles to the first order *Delta-Sigma* modulator without the concept of oversampling. Resolution is achieved at the cost of conversion time instead.

*2) Admittance measurement*

The presented approach can also be designed to extract the complex components of conductance. First, the amplifier block must act as a mixer by amplifying synchronously with the pulsed current source, just as occurs in the approach described previously in this section. To extract the imaginary component, a quarter of period delay must be introduced from the current source to the amplification phase, corresponding to 90º shift for a sinusoidal current source. Pulsed signals demodulation introduces measurement errors due to their harmonic content. By changing the current source duty-cycle from 50% to 80% and the amplification phase time from 50% to 66.7% it is possible to reduce these errors from 10% to 0.3% [5]. However, digital circuitry complexity is increased to generate control signals to the current source and amplifier timely accurate. Moreover, amplifier settling time is significantly reduced for the same measurement frequency, leading to increasing power consumption.

## III. ASIC Implementation

A 1.2V ASIC implementation on standard 0.35μm CMOS technology has been designed. The aim of this implementation is to evaluate total power consumption for conductance measurement range from 2.5mS to 14mS with a resolution of 5%. These specifications where defined according to previously studies of bio-conductance from reproductive tissues of farm mammals for artificial insemination purpose, were measurements shows a relative bio-conductance variation above 40% during the estrus cycle at several frequencies [1]. Frequency of 25kHz was chosen for design purpose because it allows circuitry to be biased at weak and moderate inversion providing high energy efficiency.

Despite of the objective purpose for this ASIC, all circuit performance depends on two external factors that are concurrent: First, all internal circuit clocks derive from a single clock input. Second, all analog circuitry biasing is dependent on an external resistance. This turns possible to test the prototype on several different conditions and find best compromise for some purpose.

ASIC block diagram is presented on Fig. 1. Only analog bias and voltage reference block was not included. Next topics describe each block individually.

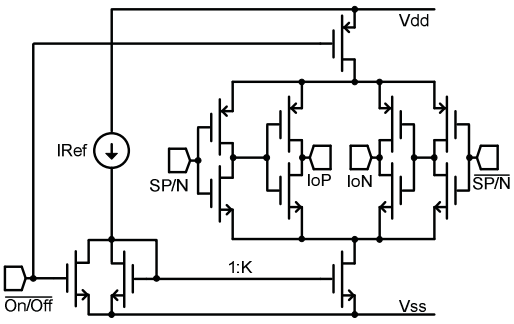


Fig. 4. Current source circuit schematic.

### A. Current Source

Circuit consists on an H bridge biased by NMOS current mirror. One control signal input blocks output current by stealing all the reference current from the mirror. Another two complementary signals define current direction on the bridge.

Two inverters were added to reduce transition glitches on step current output transitions by reducing the gate voltages on bridge transistors. Output terminals are connected to UUT and voltage amplifier input.

### B. Fully Differential Amplifier

Amplifier interfaces the UUT to the integrator input. It allows isolation needed for correct integration of voltage proportional to the real component of UUT. This application requires a relative small gain and it was chosen to be 60. An open loop single transconductance gain stage constituted by a differential pair input and terminated with a differential common drain output stage proved to be effective.

The gain of a single differential pair biased on weak inversion is relatively small and can it be adjusted by transistors lengths. Fig. 4 presents the amplifier schematic.

Despite of inherent chopper stabilization from the presented topology that provides a medium integration slope independent on the amplifier offset input error, very little input offset on this amplifier can cause a jagged slope integration signal. This problem is justified due to the very low input signal levels and may affect measurement resolution. Fortunately, with no power increment, it is possible to cancel amplifier offset with an auto-zero switched-capacitor circuit [6]. Two capacitors at the amplifier input stores the amplifier total offset during the phase were no current is applied on UUT. During the amplification phase, capacitors voltages are added to the input signal canceling amplifier offset.

Common mode output control is archived with a switched-capacitor circuit. Amplifier output signals are compared to the reference and the differential par load transistors biasing are adjusted to maintain outputs signals centered on reference. This circuit produces very high transitions spikes compared to the signal levels. However this causes no influence on circuitry performance once they are equal at both outputs and are canceled on integrator.

### C. Differential Input Integrator

Integrator is the key element to this measurement technique. It integrates a noisy and small differential amplitude signal proportional to the UUT. The chopper rectifier constitutes the

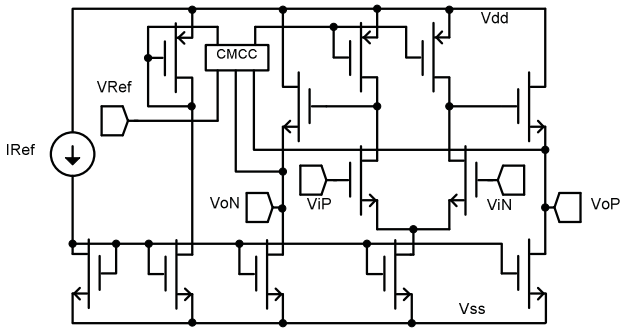


Fig. 5. Fully differential amplifier circuit schematic.

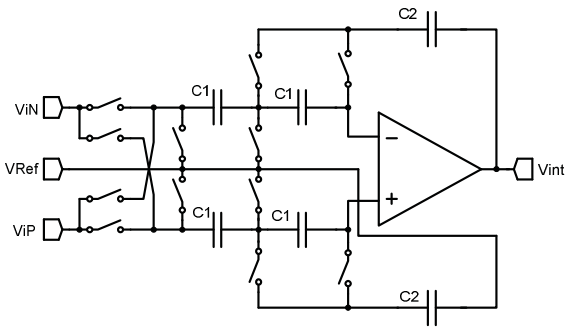


Fig. 6. Double sample technique integrator schematic.

integrator input switches.

In the presented topology, a small input offset on integrator can produce large measurement error because it would be integrated during all conversion time and chopper at the input does not cancel it. Fortunately the step signal characteristic to integrate allows using a double sample technique with little power consumption increase. This solution ease the integrator operational amplifier requirements of gain witch is decisive in very low power applications. It cancels op-amp DC input offset and reduces the finite-gain errors. This integrator is differential input version of single input double sample technique integrator [7]. A symmetric input was added, doubling capacitor and switch number and requires a modified connection to the reference.

In the Fig. 6, C2 stores integration voltage to be processed by comparator being an important element for the converter performance. Also most circuit elements sizing and biasing depends on C2 capacitance. Miller op-amp was chosen due to good power dissipation to gain-bandwidth compromise and the possibility to work at 1.2V.

### D. Comparator

Comparator consists of a differential pair loaded by a negative resistance to provide positive feedback [8]. Two transistors switch were added forcing both outputs to be zero. When switch are released one output becomes Vdd and another output becomes Vss depending on the input voltages.

Threshold voltage was chosen to be lower than reference to increase differential pair gate-source voltages and increase gain. This aspect is quite meaningful for this low voltage application. For this reason, integration voltage is decreasing during measurement.

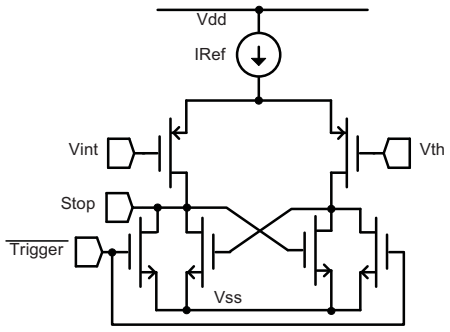


Fig. 7. Comparator circuit schematic.

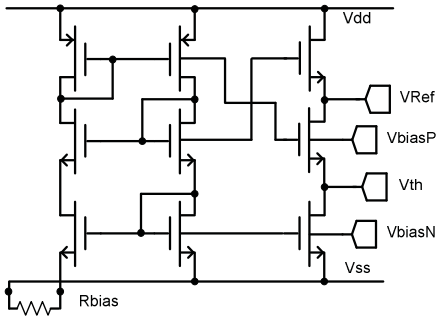


Fig. 8. Bias and reference voltage circuit chematics.

### E. Bias and Voltage References Circuits

Bias circuitry consists in simple constant transconductance circuit through an external resistor [9]. Voltages reference circuit consist in only two biased N-type large transistors connected in series acting as a source follower from two different voltages.

Circuitry was designed to be biased at 60nA with external resistance (Rbias) of 1MΩ and to create a reference voltage (VRef) about 480mV and a threshold voltage (Vth) of 250mv.

### F. Control Block

Control block generates all necessary control signals for switched-capacitor amplifier and integrator, current source and comparator. All these signals directly depend on the clock input allowing performing measurements at different frequencies. Process is initiated with the Reset input and ends through the comparator output. Serial Counter output is incremented during the process each semi-cycle of the current source signal corresponding to each integration cycle.

## IV. Layout and Simulation Results

The described circuitry requires an area of 85nm$^2$ to layout on a 0.35µm CMOS technology. Careful was taken to dispose digital control block as far as possible from the output integrator capacitors and the references block (Fig. 9).

Presented results were obtained though post-layout simulations using BSIM3v3 MOSFET model. Fig. 10 shows time response of reference, threshold voltage the integration signals from four different UUTs.

Fig. 11 presents three UUT measurement sweeps at different conditions. For the designed biasing conditions of 60nA and normal frequency of 25kHz is notable some linearity error. The step characteristic slope denotes the limited resolution. Increasing all analog circuitry bias current with a exterior

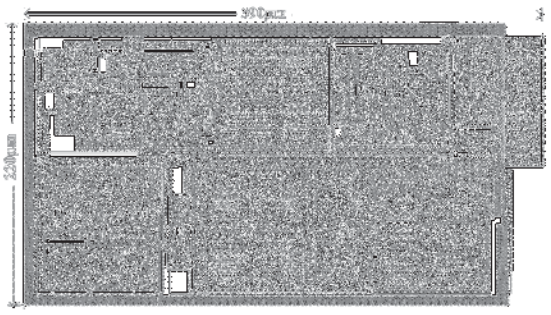

Fig. 9. Circuit layout in 0.35µm CMOS technology.

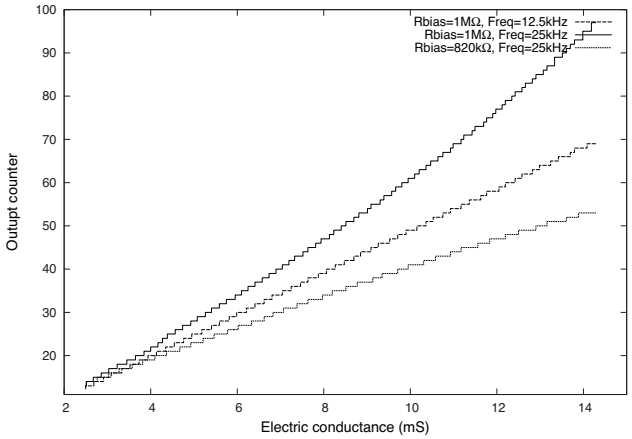


Fig. 10. UUT measurement sweeps at the different biasing and frequency conditions.

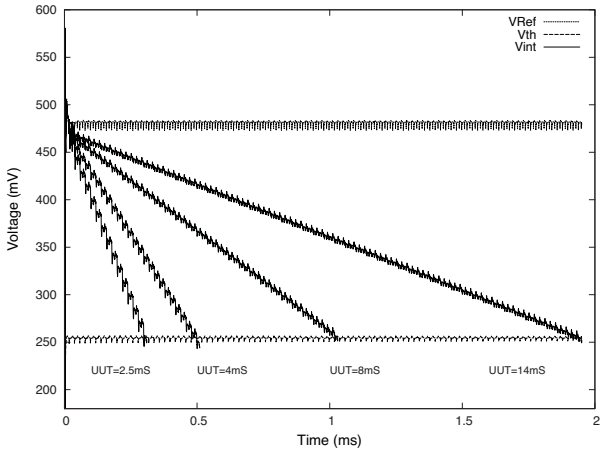


Fig. 11. Time response of reference, threshold voltage and integration signals for UUT=10kS, 14mS, 8mS, 4mS and 2.5mS.

resistance of 820kΩ shows a linearity improvement but a severe resolution decrease once the current source amplitude applied on UUT increase at the same proportion.

The reduction of measurement frequency to 12.5kHz also shows a linearity improvement and may lead to conclude that 60nA of bias condition may not be adequate to measure at 25kHz. Measurement range and resolution are certainly limited but power consumption is even more limited. With external biasing resistor of 1MΩ the total power is under 900nW. Energy is proportional to time conversion but is under 2nJ within tested range at 25kHz. With 820kΩ the total power is under 1.2μW.

## V. Conclusion

The present work describes a new electric conductance measurement approach suitable for applications providing power minimization. The approach simplicity allows designing circuitry to achieve desired accuracy and resolution. Self-powered devices can therefore include several physical parameters measurement through resistive transducers with meaningless power consumption addition. Post-layout simulations from a ASIC design shows a current consumption as low as 750nA that can be provided from a small 1.2V accumulator cell.

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